

FEATURES:

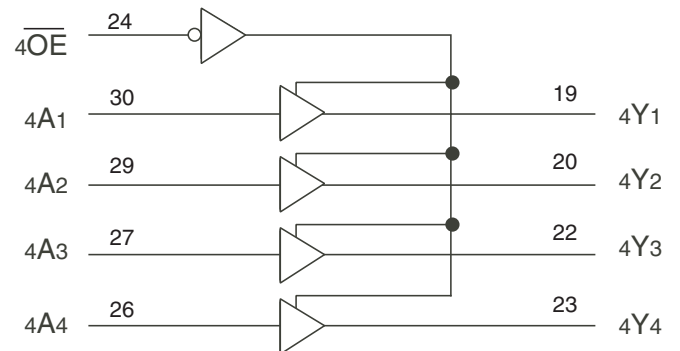
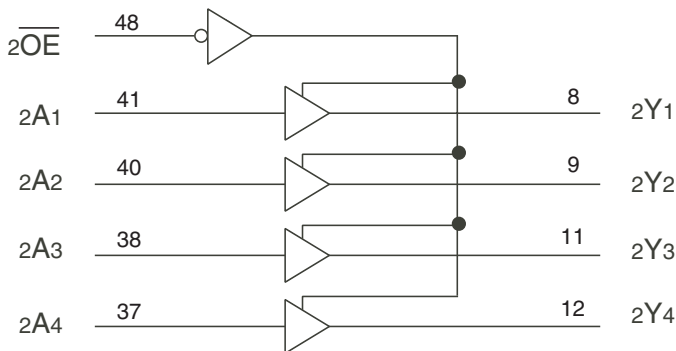
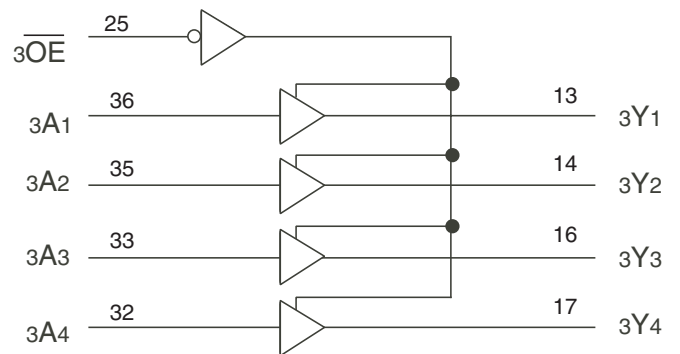
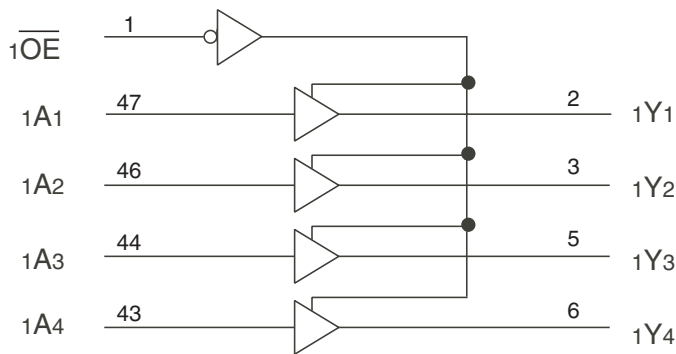
- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range, or $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- Rail-to-rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components
- Available in SSOP, TSSOP, and TVSOP packages

DESCRIPTION:

The FCT163244 16-bit buffer/line drivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices offer bus/backplane interface capability with improved packing density. These devices have a flow-through organization for simplifying board layout. The three-state controls operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

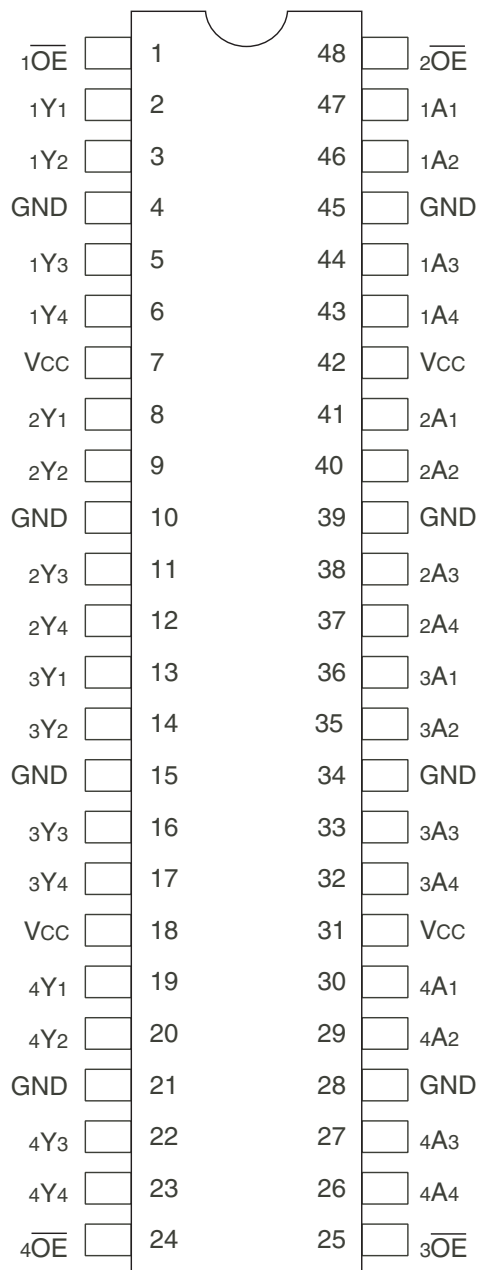
The inputs of the FCT163244 can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system. Thus, the FCT163244 can be used as buffers to connect 5V components to a 3.3V bus.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to 7	V
VTERM ⁽⁴⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +60	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- Input terminals.
- Outputs and I/O terminals.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COU	Output Capacitance	VOU = 0V	3.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xOE	3-State Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
xOE	xAx	xYx
L	L	L
L	H	H
H	X	Z

NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V _{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2	—	5.5	V	
	Input HIGH Level (I/O pins)		2	—	V _{CC} +0.5		
V _{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V	
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max.	V _I = 5.5V	—	—	±1	
	Input HIGH Current (I/O pins)						V _I = V _{CC}
I _{IL}	Input LOW Current (Input pins)		V _I = GND	—	—	±1	
	Input LOW Current (I/O pins)						V _I = GND
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = Max.	V _O = V _{CC}	—	—	±1	
I _{OZL}			V _O = GND	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V	
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	-36	-60	-110	mA	
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	50	90	200	mA	
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -0.1mA	V _{CC} -0.2	—	—	
		V _{IN} = V _{IH} or V _{IL}					I _{OH} = -3mA
		V _{CC} = 3V	I _{OH} = -8mA	2.4 ⁽⁵⁾	3	—	
V _{OL}	Output LOW Voltage	V _{CC} = Min.	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1mA	—	—	0.2
				I _{OL} = 16mA	—	0.2	0.4
				I _{OL} = 24mA	—	0.3	0.55
		V _{CC} = 3V	I _{OL} = 24mA	—	0.3	0.5	
V _{IN} = V _{IH} or V _{IL}							
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max., V _O = GND ⁽³⁾	-60	-135	-240	mA	
V _H	Input Hysteresis	—	—	150	—	mV	
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}	—	0.1	10	μA	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC}-0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V^{(3)}$		—	2	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	50	75	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.5	0.8	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.5	0.8	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2	3 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	2	3.3 ⁽⁵⁾	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input. All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} \text{ DHNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (ICCL, ICCH and ICCZ)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $DH = \text{Duty Cycle for TTL Inputs High}$
 $NT = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

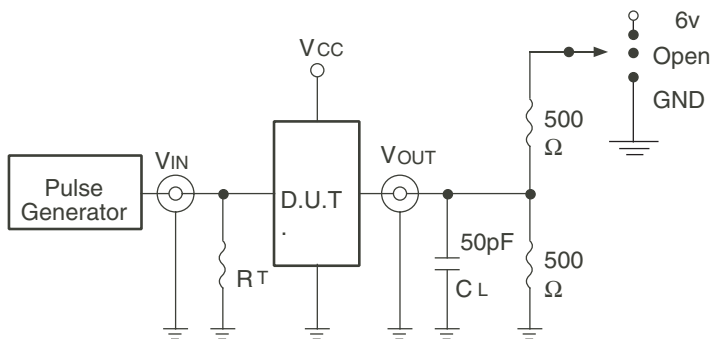
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Symbol	Parameter	Condition ⁽²⁾	FCT163244A		FCT163224C		Unit				
			Min. ⁽³⁾	Max.	Min. ⁽³⁾	Max.					
t_{PLH}	Propagation Delay	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	4.8	1.5	4.1	ns				
t_{PHL}	xAx to xYx										
t_{PZH}	Output Enable Time							1.5	6.2	1.5	5.8
t_{PZL}											
t_{PHZ}	Output Disable Time							1.5	5.6	1.5	5.2
t_{PLZ}											
$t_{SK(o)}$	Output Skew ⁽⁴⁾	—	0.5	—	0.5	ns					

NOTES:

- Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$ (normal range). For $V_{CC} = 2.7$ to $3.6V$ (extended range), all Propagation Delays and Enable/Disable times should be degraded by 20%.
- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS



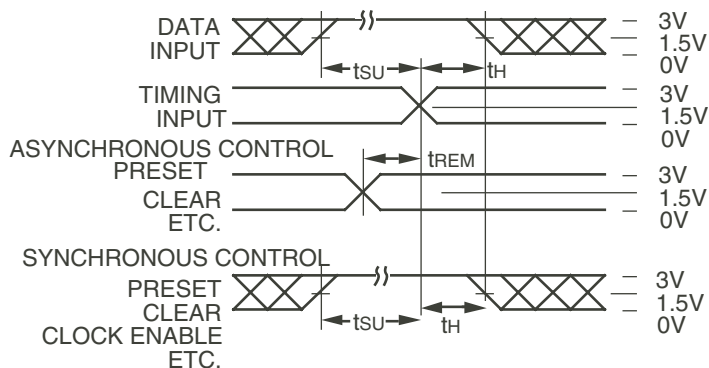
Test Circuits for All Outputs

SWITCH POSITION

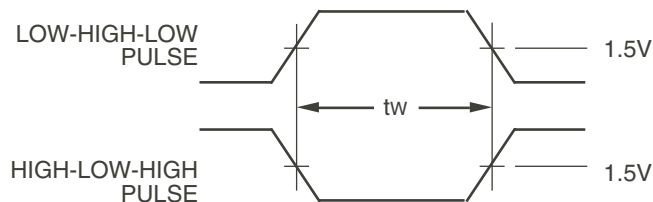
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

DEFINITIONS:

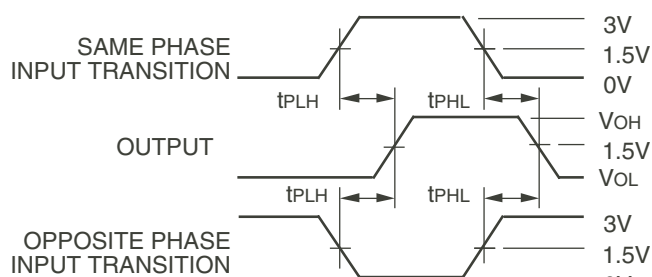
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



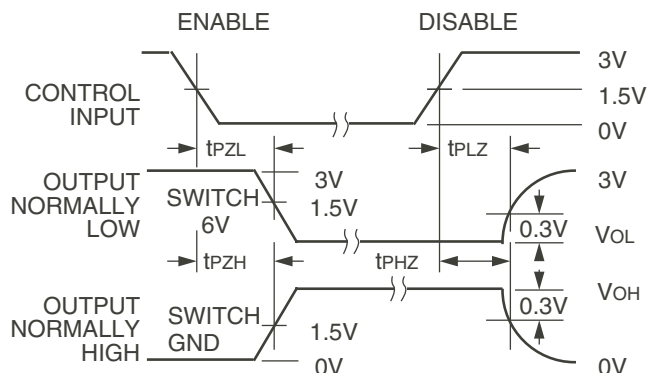
Set-up, Hold, and Release Times



Pulse Width



Propagation Delay

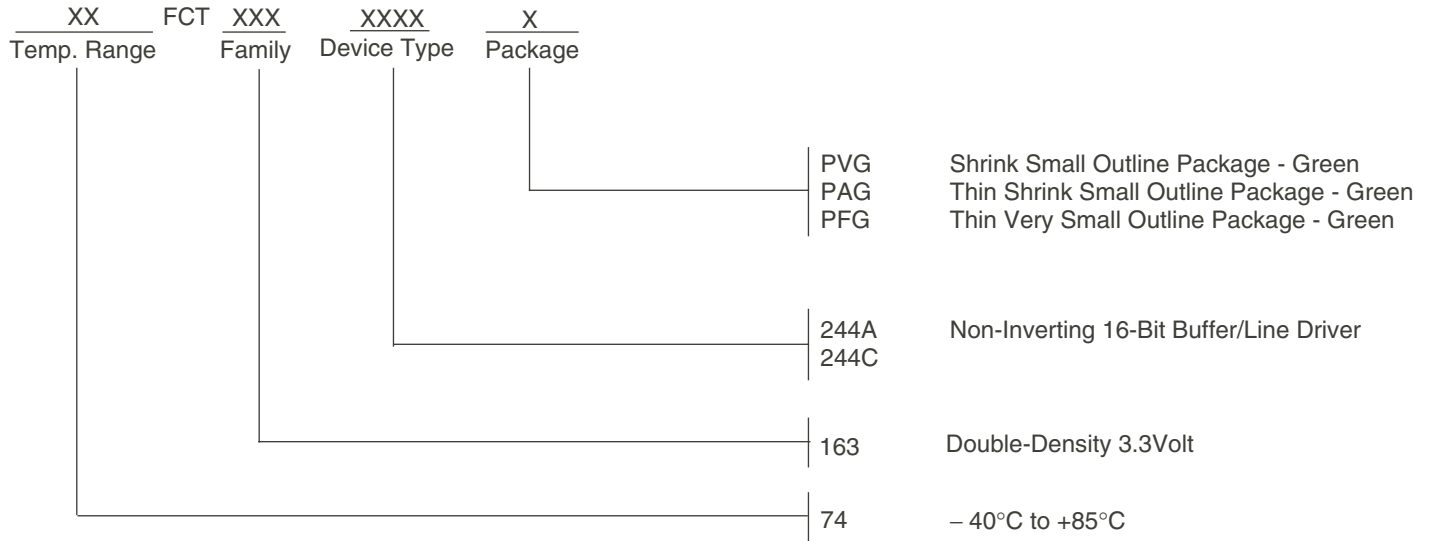


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.
3. If Vcc is below 3V, input voltage swings should be adjusted not to exceed Vcc.

ORDERING INFORMATION



Datasheet Document History

09/10/09 Pg.6 Updated the ordering information by removing the "IDT" notation and non RoHS part.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.