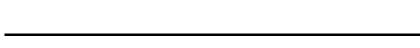
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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR NP60N04HLF, NP60N04ILF

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP60N04HLF and NP60N04ILF are N-channel MOS Field Effect Transistors designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP60N04HLF	TO-251 (MP-3)
NP60N04ILF	TO-252 (MP-3Z)

FEATURES

• Super low on-state resistance

 $R_{DS(on)1}$ = 6.5 m Ω MAX. (Vgs = 10 V, ID = 30 A)

 $R_{DS(on)2}$ = 9.1 m Ω MAX. (Vgs = 4.5 V, ID = 30 A)

- Low Ciss: Ciss = 2600 pF TYP. (VDS = 25 V, VGS = 0 V)
- Built-in gate protection diode

(TO-251)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGS = 0 V)	VDSS	40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C) Note1	ID(DC)	±60	Α
Drain Current (pulse) Note2	I _{D(pulse)}	±240	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	100	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.2	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Repetitive Avalanche Current Note3	Iar	32	Α
Repetitive Avalanche Energy Note3	Ear	100	mJ

Notes 1. Calculated contact current according to MAX. allowable channel temperature.

- **2.** PW \leq 10 μ s, Duty Cycle \leq 1%
- 3. V_{DD} = 20 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, T_{ch(peak)} \leq 150°C

(TO-252)

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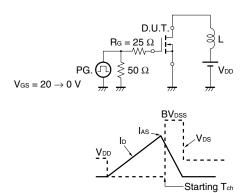


ELECTRICAL CHARACTERISTICS (TA = 25°C)

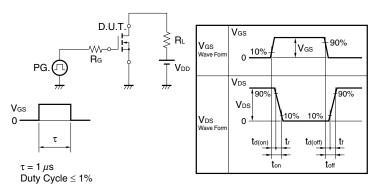
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 40 V, V _{GS} = 0 V			10	μА
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μА
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 30 A	22	43		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = 10 V, I _D = 30 A		5.2	6.5	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 30 A		6.6	9.1	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V		2600	3900	pF
Output Capacitance	Coss	V _{GS} = 0 V		480	720	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		180	330	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 30 A		11	23	ns
Rise Time	tr	V _{GS} = 10 V		13	32	ns
Turn-off Delay Time	td(off)	$R_G = 0 \Omega$		69	138	ns
Fall Time	tf			14	34	ns
Total Gate Charge	Q _G	V _{DD} = 32 V		50	75	nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		9		nC
Gate to Drain Charge	Q _{GD}	I _D = 60 A		13		nC
Body Diode Forward Voltage Note	V _F (S-D)	IF = 60 A, V _{GS} = 0 V		0.94	1.5	V
Reverse Recovery Time	trr	IF = 60 A, V _{GS} = 0 V		40		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		42		nC

Note Pulsed

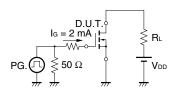
TEST CIRCUIT 1 AVALANCHE CAPABILITY



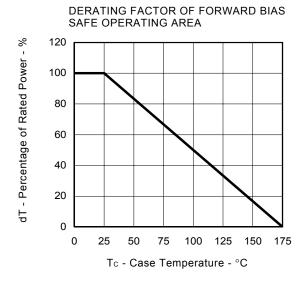
TEST CIRCUIT 2 SWITCHING TIME

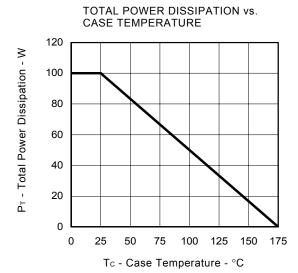


TEST CIRCUIT 3 GATE CHARGE

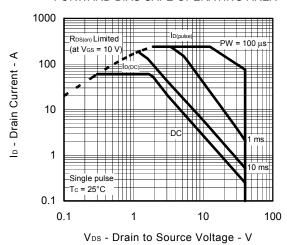


TYPICAL CHARACTERISTICS (TA = 25°C)

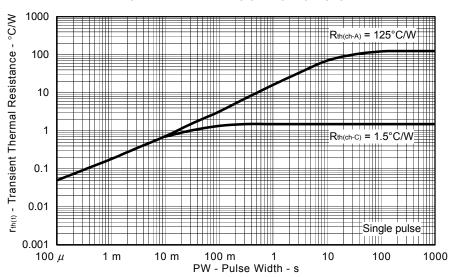




FORWARD BIAS SAFE OPERATING AREA

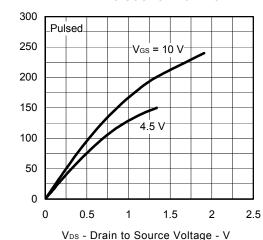


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

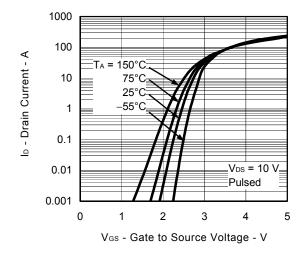


lo - Drain Current - A

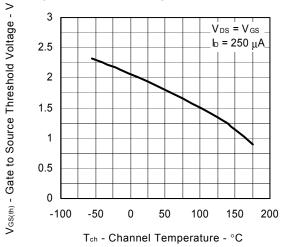
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



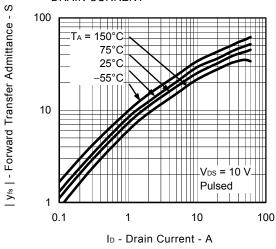
FORWARD TRANSFER CHARACTERISTICS



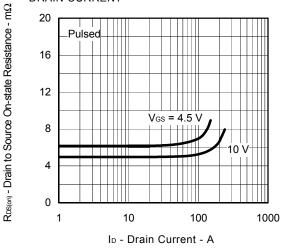
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



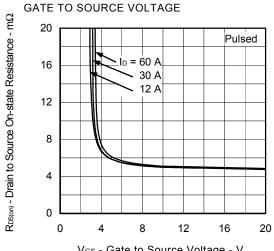
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**

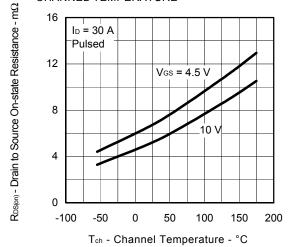


DRAIN TO SOURCE ON-STATE RESISTANCE vs.

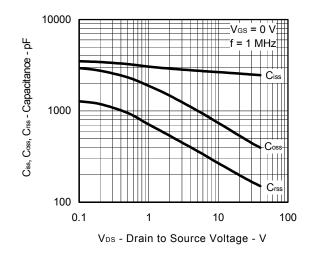


V_{GS} - Gate to Source Voltage - V

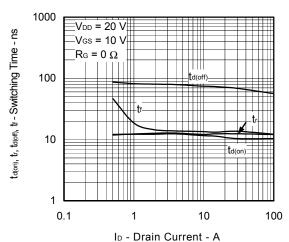
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



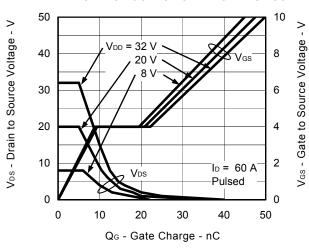
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



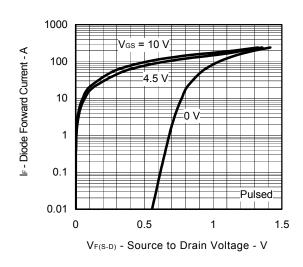
SWITCHING CHARACTERISTICS



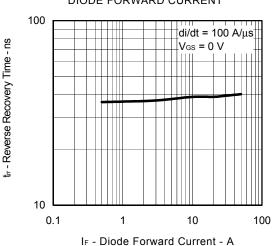
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



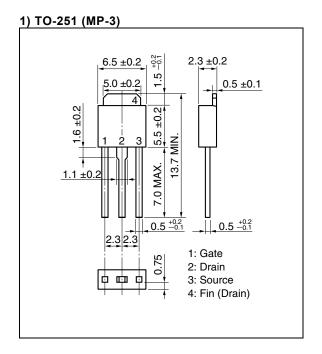
SOURCE TO DRAIN DIODE FORWARD VOLTAGE

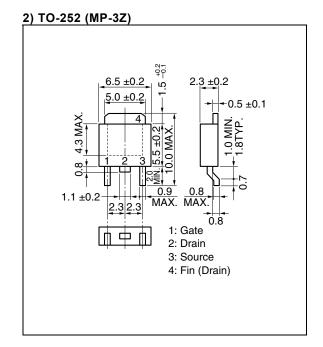


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

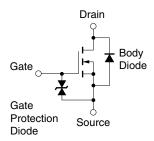


PACKAGE DRAWINGS (Unit: mm)





EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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