ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4512B
Integrated Circuit
CMOS, 8–Channel Data Selector

Description:

The NTE4512B is an 8–channel data selector in a 16–Lead DIP type package constructed with MOS P–channel and N–channel enhancement mode devices is a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequencing generation.

Features:

- Noise Immunity = 45% of V_{DD} (Typ)
- Diode Protection on All Inputs
- High Fanout > 50
- Single Supply Operation – Positive or Negative
- 3–State Output (Logic “1”, Logic “0”, High Impedance)
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 4) “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 3, Note 5)	I_T	5.0	I_T = (0.8µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.6µA/kHz) f + I_{DD}							µAdc
		15	I_T = (2.4µA/kHz) f + I_{DD}							µAdc
Three State Leakage Current	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both “1” and “0” = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (3.0ns/pF) C_L + 25ns	t_{TLH}	5.0	–	225	360	ns
t_{TLH} = (1.5ns/pF) C_L + 12ns		10	–	110	180	ns
t_{TLH} = (1.1ns/pF) C_L + 8ns		15	–	80	130	ns
Output Fall Time t_{THL} = (1.5ns/pF) C_L + 47ns	t_{THL}	5.0	–	130	200	ns
t_{THL} = (0.75ns/pF) C_L + 24ns		10	–	65	100	ns
t_{THL} = (0.55ns/pF) C_L + 17ns		15	–	50	80	ns
Turn−Off Delay Time t_{PLH} = (0.9ns/pF) C_L + 211ns	t_{PLH}	5.0	–	330	650	ns
t_{PLH} = (0.3ns/pF) C_L + 70ns		10	–	125	250	ns
t_{PLH} = (0.23ns/pF) C_L + 54ns		15	–	85	170	ns
Turn−On Delay Time t_{PHL} = (2.7ns/pF) C_L + 184ns	t_{PHL}	5.0	–	330	650	ns
t_{PHL} = (0.9ns/pF) C_L + 61ns		10	–	125	250	ns
t_{PHL} = (0.68ns/pF) C_L + 47ns		15	–	85	170	ns
3−State Output Delay Time “1” or “0” to High Impedance, and High Impedance to “1” or “0”	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	5.0	–	60	150	ns
		10	–	35	100	ns
		15	–	30	75	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

C	B	A	Inhibit	Disable	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
DC	DC	DC	1	0	0
DC	DC	DC	DC	1	High Impedance

DC = Don’t Care

Pin Connection Diagram