

MOSFETs Silicon N-channel MOS (U-MOS<sup>VI</sup>-H)

# XPW4R10ANB

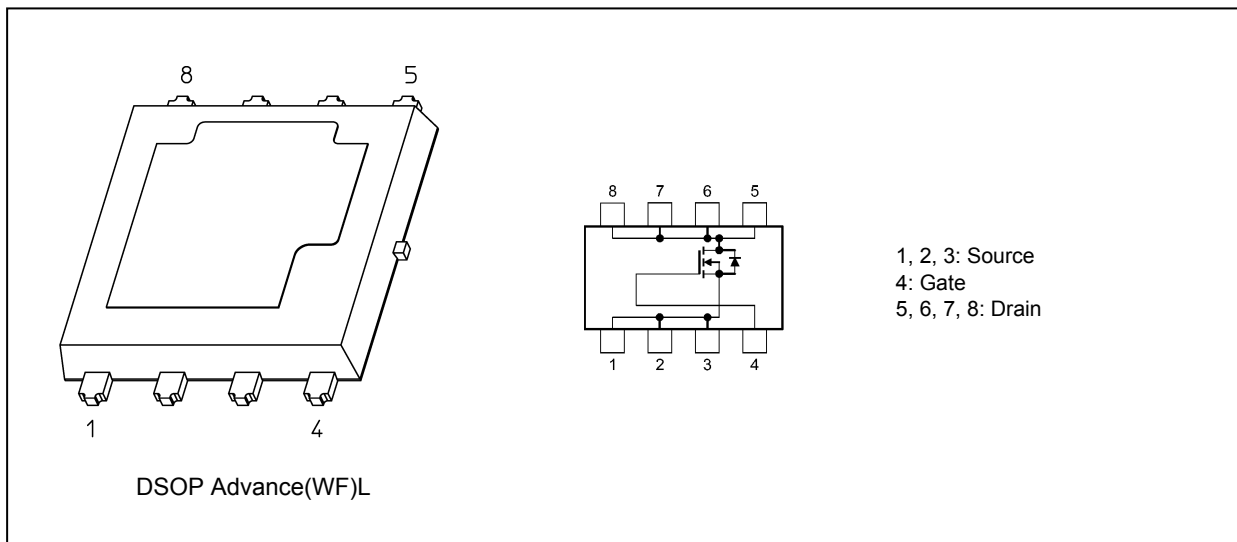
## 1. Applications

- Automotive
- Motor Drivers
- Switching Voltage Regulators

## 2. Features

- (1) AEC-Q101 qualified
- (2) Small, thin package
- (3) Low drain-source on-resistance:  $R_{DS(ON)} = 3.4 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (4) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 100 \text{ V}$ )
- (5) Enhancement mode:  $V_{th} = 2.5 \text{ to } 3.5 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1.0 \text{ mA}$ )

## 3. Packaging and Internal Circuit



Start of commercial production

2020-09

### 4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ °C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	100	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	
Drain current (DC) (Note 1)	$I_D$	70	A
Drain current (pulsed) (Note 1)	$I_{DP}$	210	
Power dissipation ( $T_c = 25\text{ °C}$ ) (Note 6)	$P_D$	170	W
Power dissipation ( $t = 10\text{ s}$ ) (Note 2)		3.0	
Power dissipation ( $t = 10\text{ s}$ ) (Note 3)		0.96	
Single-pulse avalanche energy (Note 4)	$E_{AS}$	241	mJ
Single-pulse avalanche current	$I_{AS}$	70	A
Channel temperature (Note 5)	$T_{ch}$	175	°C
Storage temperature (Note 5)	$T_{stg}$	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: When the body or a connecting part of a semiconductor product is subjected to vibration, impact or stress in actual equipment, bonding fault or device destruction may result.

Therefore, be sure to keep this in mind at the time of structural design.

If a semiconductor product is subject to especially strong vibration, impact or stress, the package or chip may crack. If stress is applied to a semiconductor chip through the package, changes in the resistance of the chip may result due to piezoelectric effects, resulting in fluctuation in element characteristics.

Furthermore, if a stress that does not instantly result in damage is applied continually for a long period of time, product deformation may result, causing defects such as disconnection or element failure.

Thus, at the time of structural design, carefully consider vibration, impact and stress.

### 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal impedance ( $T_c = 25\text{ }^\circ\text{C}$ )	$Z_{th(ch-c)}$	0.88	$^\circ\text{C/W}$
Channel-to-top-plate thermal impedance (Note 7)	$Z_{th(ch-tp)}$	0.93	$^\circ\text{C/W}$
Channel-to-ambient thermal impedance ( $t = 10\text{ s}$ ) (Note 2)	$Z_{th(ch-a)}$	50	$^\circ\text{C/W}$
Channel-to-ambient thermal impedance ( $t = 10\text{ s}$ ) (Note 3)	$Z_{th(ch-a)}$	156	$^\circ\text{C/W}$

Note 1: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

Note 2: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 3: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 4:  $V_{DD} = 80\text{ V}$ ,  $T_{ch} = 25\text{ }^\circ\text{C}$  (initial),  $L = 37.9\text{ }\mu\text{H}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 70\text{ A}$

Note 5: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

Note 6:  $T_c$  is defined as a temperature of the drain electrode.

Note 7: A maximum of the  $Z_{th(ch-tp)}$  measured at Toshiba's test environment is only used for reference.

An area of the top-plate is shown in Figure 5.3.

Be aware that the top-plate has the same electric potential as the sources; however, not intended for an electrode.

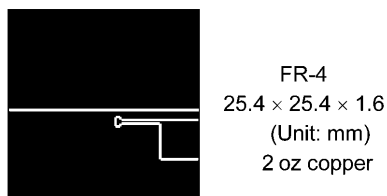


Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

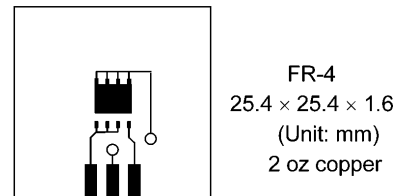
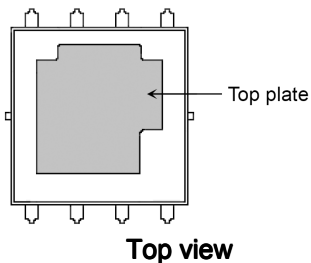


Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)



Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

### 6. Electrical Characteristics

#### 6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	100	—	—	V
	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	80	—	—	
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 1.0\text{ mA}$	2.5	—	3.5	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 6\text{ V}, I_D = 35\text{ A}$	—	4.1	6.2	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 35\text{ A}$	—	3.4	4.1	

#### 6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 300\text{ kHz}$	—	4970	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	300	—	
Output capacitance	$C_{oss}$		—	1940	—	
Gate resistance	$r_g$		—	2.1	4.2	
Switching time (rise time)	$t_r$	See Fig. 6.2.1	—	21	—	ns
Switching time (turn-on time)	$t_{on}$		—	52	—	
Switching time (fall time)	$t_f$		—	22	—	
Switching time (turn-off time)	$t_{off}$		—	89	—	

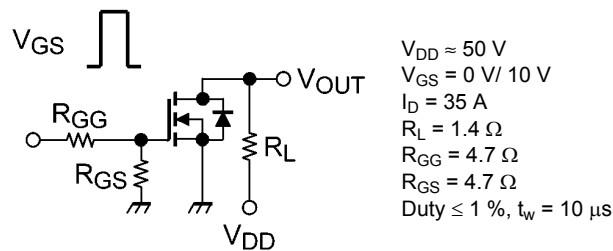


Fig. 6.2.1 Switching Time Test Circuit

#### 6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 80\text{ V}, V_{GS} = 10\text{ V}, I_D = 70\text{ A}$	—	75	—	nC
Gate-source charge 1	$Q_{gs1}$		—	22	—	
Gate-drain charge	$Q_{gd}$		—	16	—	

#### 6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 8)	$I_{DRP}$	—	—	—	210	A
Diode forward voltage	$V_{DSF}$	$I_{DR} = 70\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	V

Note 8: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

## 7. Marking

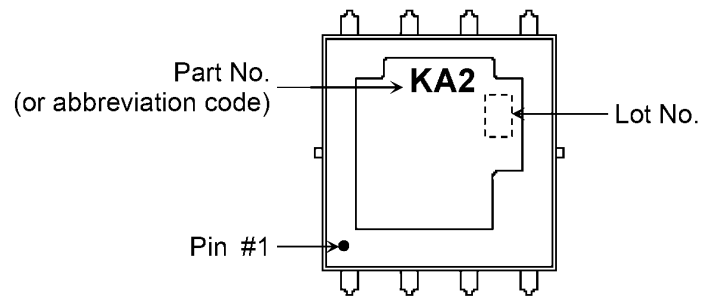
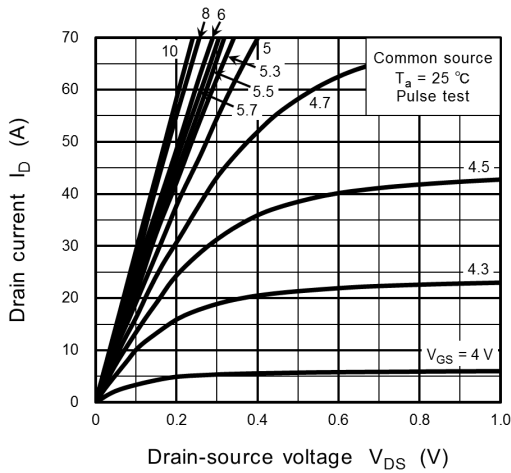
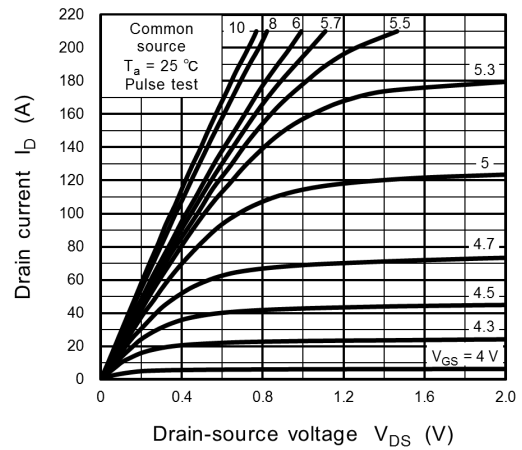


Fig. 7.1 Marking

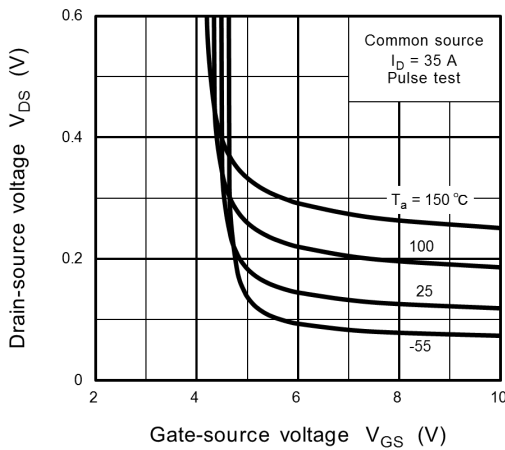
### 8. Characteristics Curves (Note)



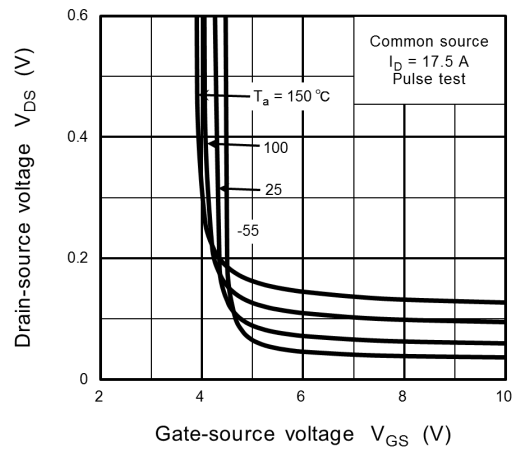
**Fig. 8.1  $I_D - V_{DS}$**



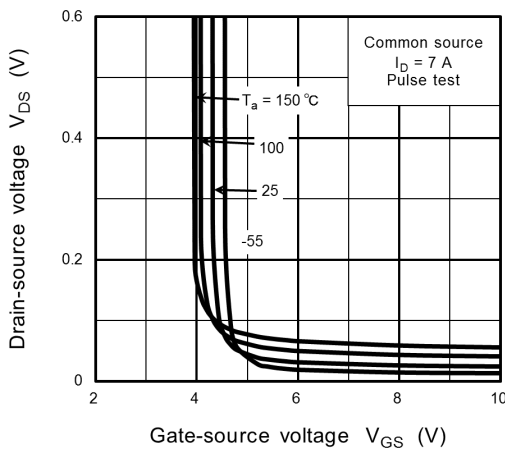
**Fig. 8.2  $I_D - V_{DS}$**



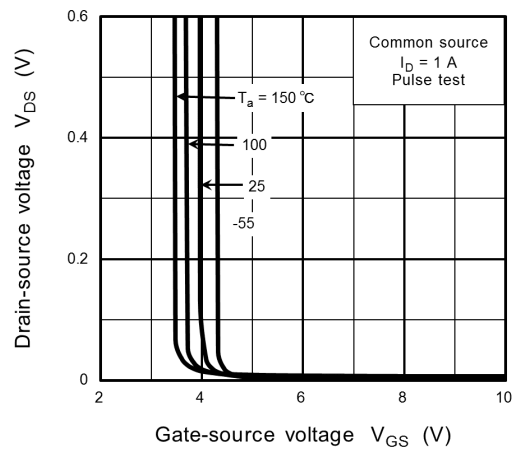
**Fig. 8.3  $V_{DS} - V_{GS}$**



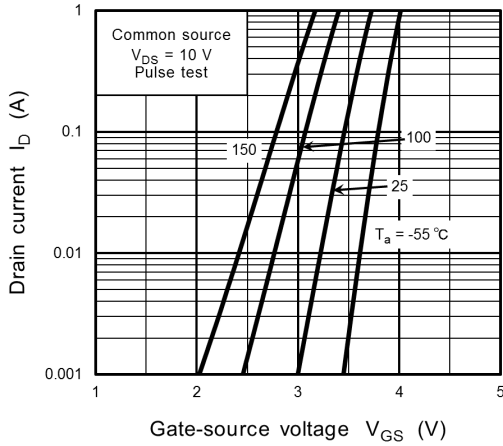
**Fig. 8.4  $V_{DS} - V_{GS}$**



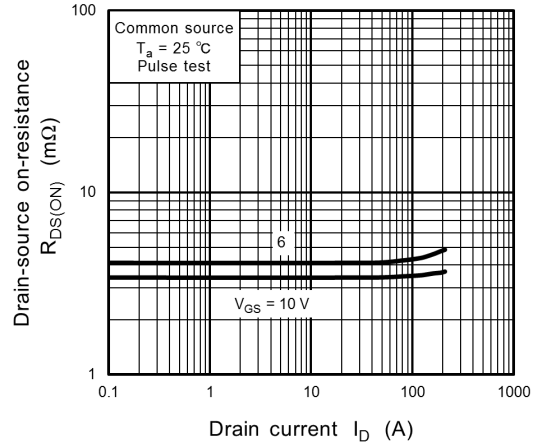
**Fig. 8.5  $V_{DS} - V_{GS}$**



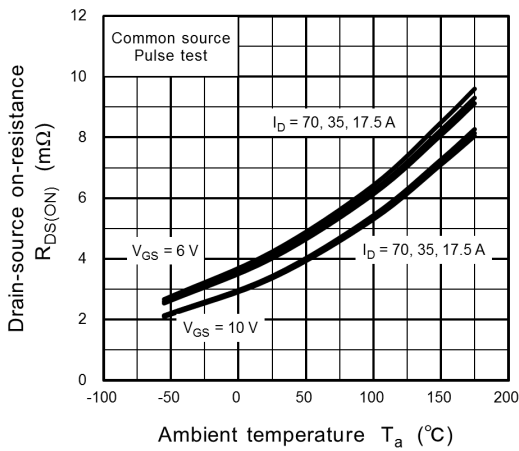
**Fig. 8.6  $V_{DS} - V_{GS}$**



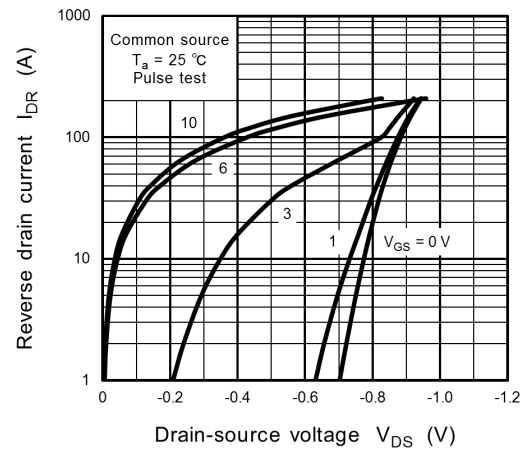
**Fig. 8.7  $I_D - V_{GS}$**



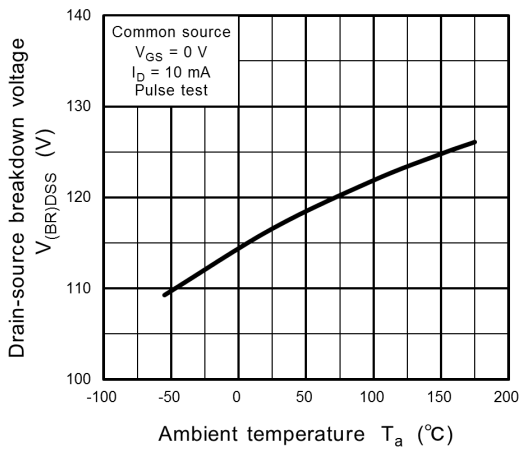
**Fig. 8.8  $R_{DS(ON)} - I_D$**



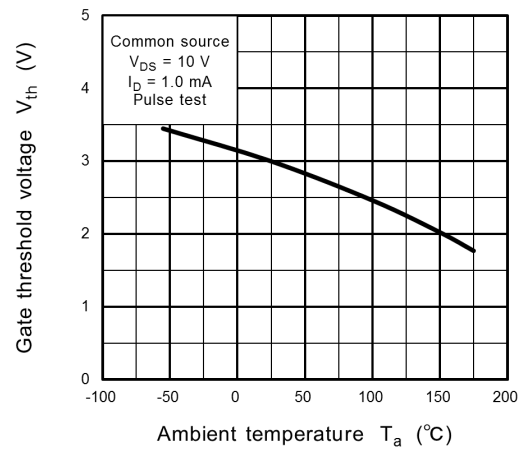
**Fig. 8.9  $R_{DS(ON)} - T_a$**



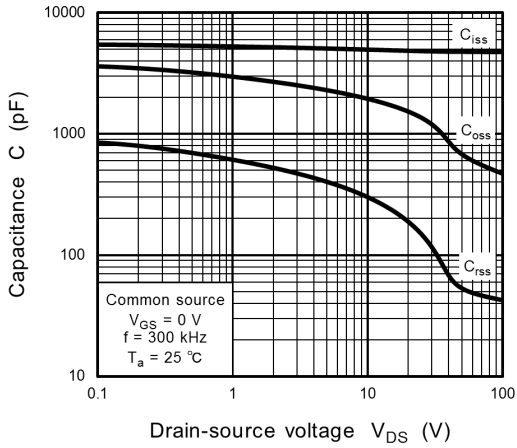
**Fig. 8.10  $I_{DR} - V_{DS}$**



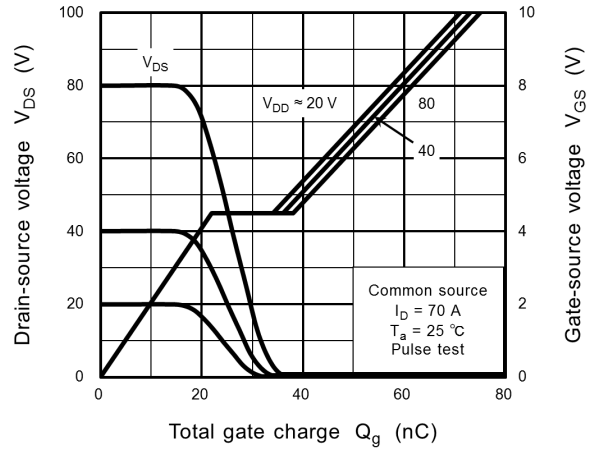
**Fig. 8.11  $V_{(BR)DSS} - T_a$**



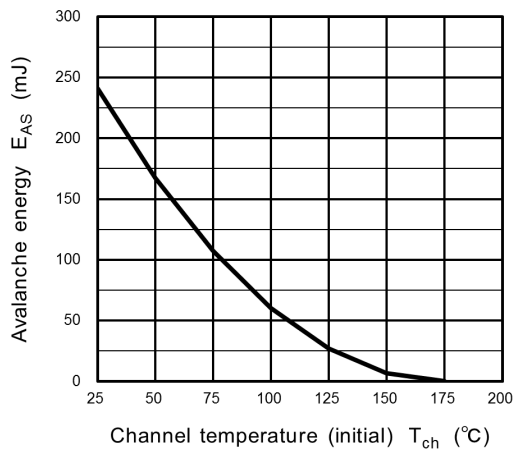
**Fig. 8.12  $V_{th} - T_a$**



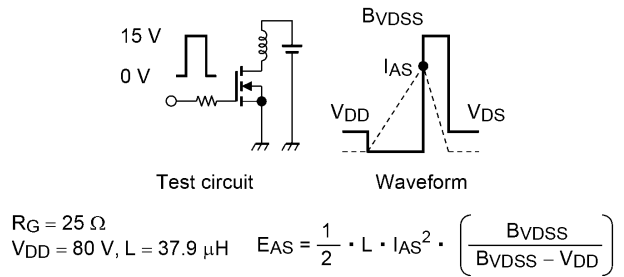
**Fig. 8.13 Capacitance -  $V_{DS}$**



**Fig. 8.14 Dynamic Input/Output Characteristics**

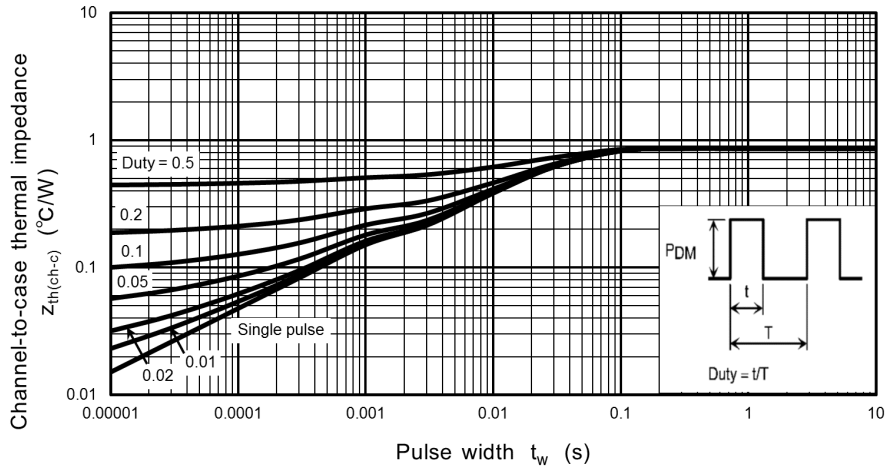


**Fig. 8.15  $E_{AS}$  -  $T_{ch}$ (Guaranteed Maximum)**

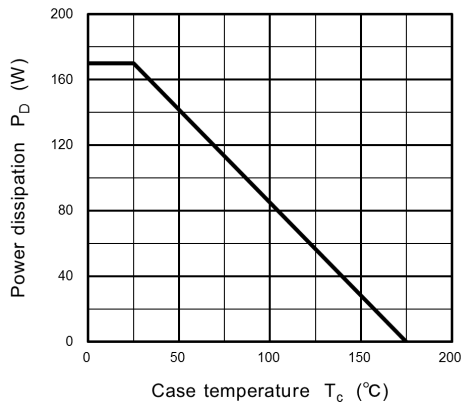


**Fig. 8.16 Test Circuit/Waveform**

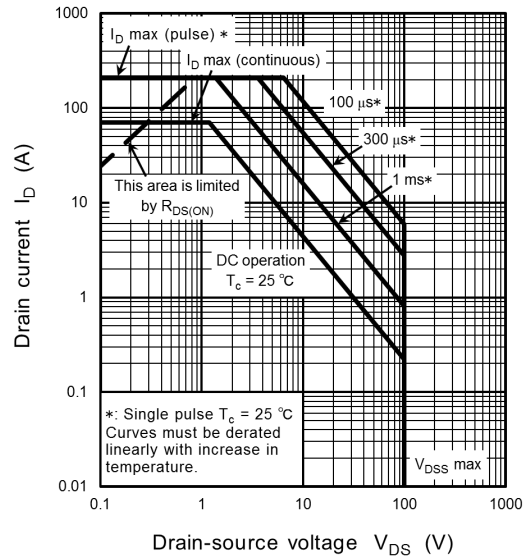




**Fig. 8.17  $Z_{th(ch-c)} - t_w$**   
(Guaranteed Maximum)



**Fig. 8.18  $P_D - T_c$**   
(Guaranteed Maximum)



**Fig. 8.19 Safe Operating Area**  
(Guaranteed Maximum)

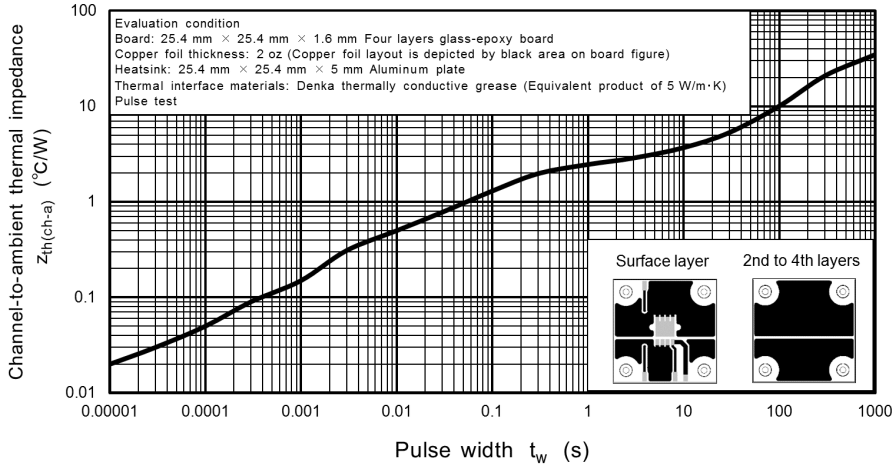


Fig. 8.20  $Z_{th(ch-a)} - t_w$   
(Reference Values)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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