UNITRODE

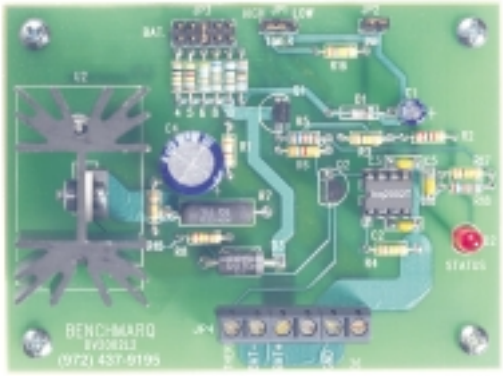
DV2002L2/TL2

Fast Charge Development System

Control of LM317 Linear Regulator

Features

- bq2002/T fast-charge control evaluation and development
- Charge current sourced from an on-board linear regulator (up to 1.5A)
- Fast charge of 4, 5, 6, 8, and 10 NiCd or NiMH cells (contact Benchmarq for other cell counts)
- Fast-charge termination by negative delta voltage (-ΔV) or peak voltage detect (bq2002) or ΔT/Δt (bq2002T)
- Maximum temperature and maximum time safety terminations
- -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Inhibit fast charge by a logic-level input



General Description

The DV2002L2/TL2 Development System provides a development environment for the bq2002 and bq2002T Fast-Charge ICs. The DV2002L2/TL2 incorporates a bq2002/T and a linear regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: ΔT/Δt, maximum temperature, maximum time, or an inhibit command for the bq2002T; or -ΔV/peak voltage, maximum temperature, maximum time, and inhibit command for the bq2002. Jumper settings select the top-off and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2002L2/TL2 for the number of cells and maximum charge time (with or without top-off).

Please review the bq2002T or bq2002 data sheet before using the DV2002L2/TL2 board.

Connection Descriptions

JP4		
	THERM	Thermistor connection
	BAT–	Battery ground
	BAT+	Positive battery terminal
	GND	Ground from charger supply
	DC	DC input from charger supply
JP3	NOC	Select number of cells
JP2	INH	Inhibit input
JP1	TM	Timer, etc. Setting

Fixed Configuration

The DV2002L2/TL2 board has the following fixed characteristics:

V_{CC} (4.75–5.25V) is regulated on-board from the supply at connector JP4 (DC:GND).

$\overline{LED}$ indicates charge status.

Charge initiates on the later application of the battery or DC, which provides V_{CC} to the bq2002/T.

Table 1. Lookup Table for R7 Selection

Input Voltage	Current	Resistance	Wattage
to 25V	1A	1.25Ω	2W
	1.5A	0.83Ω	2W

As shipped from Benchmarq, the DV2002L2/TL2 linear regulator is configured to a charging current of 1.25A. This current level is controlled by the value of sense resistor R_7 by the relationship:

$$I_{CHG} = \frac{1.25V}{R_7}$$

The value of R_7 at shipment is 1Ω. This resistor can be changed depending on the application.

The suggested maximum I_{CHG} for the DV2002L2/TL2 board is 1.5A. ***U2 must be mounted to an appropriate heat sink.***

The maximum cell voltage (MCV) is scaled to 2V/cell.

With the provided NTC thermistor connected between THERM and BAT–, TCO = 50°C.

The thermistor is identified by the serial number suffix as follows:

Identifier	Thermistor
K1	Keystone RL0703-5744-103-S1
(blank)	Philips 2322-640-63103
F1	Fenwal Type 16, 197-103LA6-A01
O1	Ozhumi 150-108-00(4)
S1	Semetic 103AT-2

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Jumper-Selectable Configuration

The DV2002L2/TL2 must be configured as described below.

INH (JP2): Enables/disables charge inhibit (see bq2002/T data sheet).

Jumper Setting	Pin State
[1 2] 3	Disabled (high)
1 [2 3]	Enabled (low)

TM (JP1): Selects fast charge safety time/top-off (see bq2002/T data sheet).

Jumper Setting	Pin State
[1 2] 3	High
1 [2 3]	Low
1 2 3	Float

Number of Cells (JP3): A resistor-divider network is provided to select 4 to 10 cells (the resulting resistor value equals N – 1 cells). RB1 is a 100KΩ resistor, and RB2 (RB20–RB25) is jumper-selected.

Closed Jumper	Number of Cells
R13	10
R12	8
R11	6
R10	5
R9	4

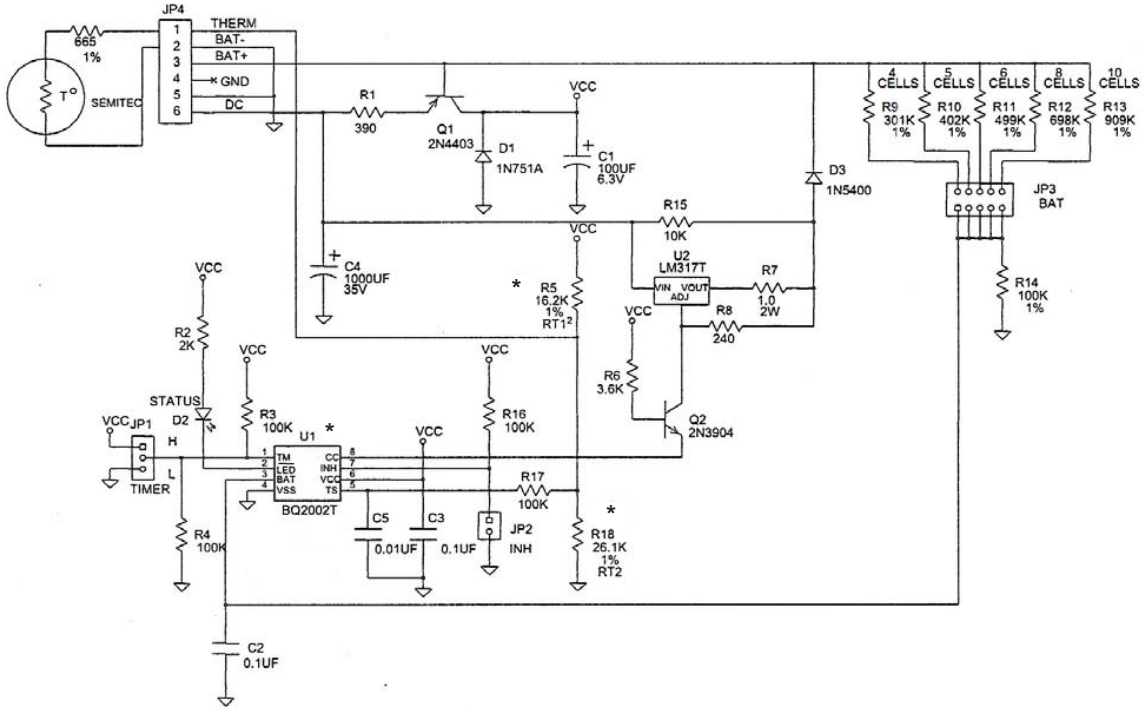
Temperature Disable: Connecting a 10KΩ resistor between THERM and BAT– disables temperature control.

Setup Procedure

1. Configure TM, INH, and number-of-cells (NOC) jumpers.
2. Connect the provided thermistor or a 10KΩ resistor between THERM and BAT–.
3. Attach the battery pack to BAT+ and BAT–. For temperature control, the thermistor must contact the cells.
4. Attach DC current source to DC (+) and GND (–) connections in JP4.

Symbol	Description	Minimum	Typical	Maximum	Unit
I_{DC}	Maximum input current	-	-	1.5	A
V_{DC}	Maximum input voltage	4.0 + V_{BAT} or 10	-	18 + V_{BAT} or 25	V
V_{BAT}	BAT input voltage	-	-	24	V
V_{TH}	THERM input voltage	0.5	-	5	V

DV2002L2/TL2 Board Schematic



* For the DV2002L2, U1 is the bq2002, R5 is 3.57 kΩ, and R18 is open.

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