DATA SHEET

FEATURES

- **SMPTE 292M compliant**
- **fully automatic adjustment free reclocker for HDTV signals**
- **1.485Gb/s and 1.485/1.001Gb/s operation**
- **dual 75Ω co-axial cable driver outputs**
- **reclocker bypass mode**
- **seamless input Interface to the GS1504 HD adaptive equalizer**
- **low power**
- **lock detect**
- **Pb-free and Green**
- **+5V or -5V power supply operation**
- **44 pin MQFP**

APPLICATIONS

SMPTE 292M Serial Digital Routers; SMPTE 292M Serial Digital Distribution Amplifiers.

DESCRIPTION

The GS1515 HDTV Serial Digital Reclocker is designed to automatically recover the embedded clock signal and re-time the data from a SMPTE 292M compliant digital video signal.

An internal low pass filter removes the high frequency jitter components from the bit-serial stream. 100Ω differential input termination is on-chip for seamless matching to 50Ω transmission lines. A dual SMPTE 292M compliant output Cable Driver is also included on-chip. The GS1515 uses the GO1515 external VCO connected to the internal PLL circuitry in order to achieve ultra low noise PLL performance.

Two diagnostic features are included in the GS1515 for robust system design. The Input Jitter Indicator (IJI) indicates excessive input jitter before the Serial Digital outputs are muted and the Jitter Demodulator Function (DM) helps to debug systems and locate the source of jitter.

The GS1515 is packaged in a 44 pin MQFP package and requires a single 5V power supply. The GS1515 typically draws 100mA of current.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	Pb-FREE AND GREEN
GS1515-CQM	44 pin MQFP	0°C to 70°C	No
GS1515-CTM	44 pin MQFP Tape	0°C to 70°C	No
GS1515-CQME3	44 pin MQFP	0°C to 70°C	Yes
GS1515-CTME3	44 pin MQFP Tape	0°C to 70°C	Yes
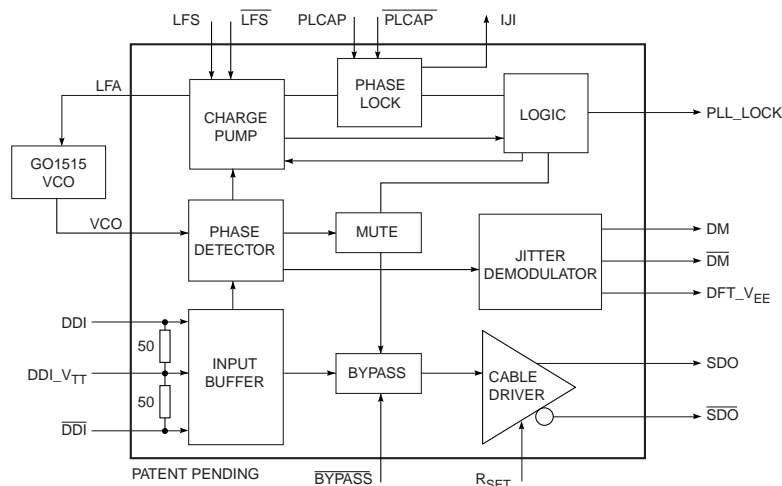
BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.5 V_{DC} to +5.5V_{DC}
Input Voltage Range	-0.3 < V_{IN} < V_{DD} + 0.3V
Input ESD Voltage	2000V
Operating Temperature Range	0°C T_A to 70°C
Storage Temperature Range	-40°C T_S to 125°C
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V, T_A = 0°C to 70°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Positive Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
Power Consumption (without GO1515 VCO) T_A = 25°C	P_D	Cable Driver Output 800mV into 75Ω load, R_{SET} = 52.3Ω, ± 1%	-	500	-	mW	1
		Used as a buffer O/P 200mV into 75Ω load, R_{SET} = 210Ω, ± 1%	-	420	-	mW	3
Supply Current (without GO1515 VCO) T_A = 25°C V_{CC} = 5V	I_C	Cable Driver Output 800mV into 75Ω load, R_{SET} = 52.3Ω, ± 1%	-	100	125	mA	1
		Used as a buffer O/P 200mV into 75Ω load, R_{SET} = 210Ω, ± 1%	-	84	111	mA	3
Logic Input Low	V_{IL}		-0.5	-	0.8	V	1
Logic Input High	V_{IH}		2.0	-	V_{CC} + 0.5	V	1
Logic Output Low	V_{OL}	at 400µA	-	-	0.5	V	1
Logic Output High	V_{OH}	at 150µA	2.4	3.5	-	V	1
Serial Input, common mode	V_{DDI-CM}		2.5 + V_{SID}/2	-	V_{CC} - V_{SID}/2	V	2, 4
Serial Input, differential	V_{SID}		100	-	800	mV	2, 4
Serial Outputs, tuning range	V_{SOD}		0	800	880	mV	4

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5 V, T_A = 0 °C to 70 °C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Serial Input Data Rate			-	1.485 or 1.485/1.001	-	Gb/s	1
Serial Input Jitter Tolerance		Worst case modulation Eg. Square wave or histogram with two peaks	-	0.5	-	UI	3, 4
		Onset of errors with histogram extending tails (outliers) with major (75%) transitions within 0.4UI	-	0.8	-	UI	4
PLL Lock Time - Asynchronous	t_{ALOCK}	Loop Bandwidth approximately 1.41MHz at 0.2UI input jitter modulation	-	60	100	ms	1
		Loop Bandwidth approximately 129kHz at 0.2UI input jitter modulation	-	340	560	ms	3
PLL Lock Time - Synchronous	t_{SLOCK}	Loop Bandwidth approximately 1.41MHz at 0.2UI input jitter modulation	-	1.25	-	µs	3
		Loop Bandwidth approximately 129kHz at 0.2UI input jitter modulation	-	12.5	-	µs	3
Serial Output Data Rate	BR_{SDO}		-	1.485 or 1.485/1.001	-	Gb/s	1, 2
Serial Output - Signal Swing	V_{SDO}	R_{SET} = 52.3Ω, ± 1%	750	800	850	mV	1
Serial Output - Rise Time 20% - 80%	SDO_{tr}	No Compensation for Return Loss	-	150	230	ps	1
		Return Loss Compensation R_{COMP} = 75Ω, 1% L_{COMP} = 10nH C_{COMP} = 1.5pF	-	220	255	ps	4
Serial Output - Fall Time 20% - 80%	SDO_{tf}	No Compensation for Return Loss	-	150	230	ps	1
		Return Loss Compensation R_{COMP} = 75Ω, 1% L_{COMP} = 10nH C_{COMP} = 1.5pF	-	220	255	ps	4
Serial Output - Intrinsic Jitter	t_{IJ}	Loop Bandwidth approximately 1.41MHz at 0.2UI input jitter modulation (jitter for clean PRN23 input and SMPTE pathological)	-	42	90	ps p-p	3
Loop Bandwidth at 0.2UI input jitter modulation	BW_{LOOP}	C_{CP1}, C_{CP2} = 1µF C_{CP3} = Open R_{CP1} = Open	-	1.41	-	MHz	4
		C_{CP1}, C_{CP2} = 5.6µF C_{CP3} =1.0µF R_{CP1} = 50Ω	-	129	-	kHz	4

GS1515

AC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +5 V, T_A = 0 °C to 70 °C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Jitter Peaking		Loop Bandwidth approximately 1.41MHz at 0.2UI input jitter modulation	-	0.05	-	dB	4
		Loop Bandwidth approximately 129kHz at 0.2UI input jitter modulation	-	0.05	-	dB	4
Phaselock Unlock Timer		10nF PLCAP	-	67	-	µs	2, 4

NOTES

1. 100% Tested at 25°C

2. Guaranteed by Design

3. Correlated Value

4. Using EB1515

PIN CONNECTIONS

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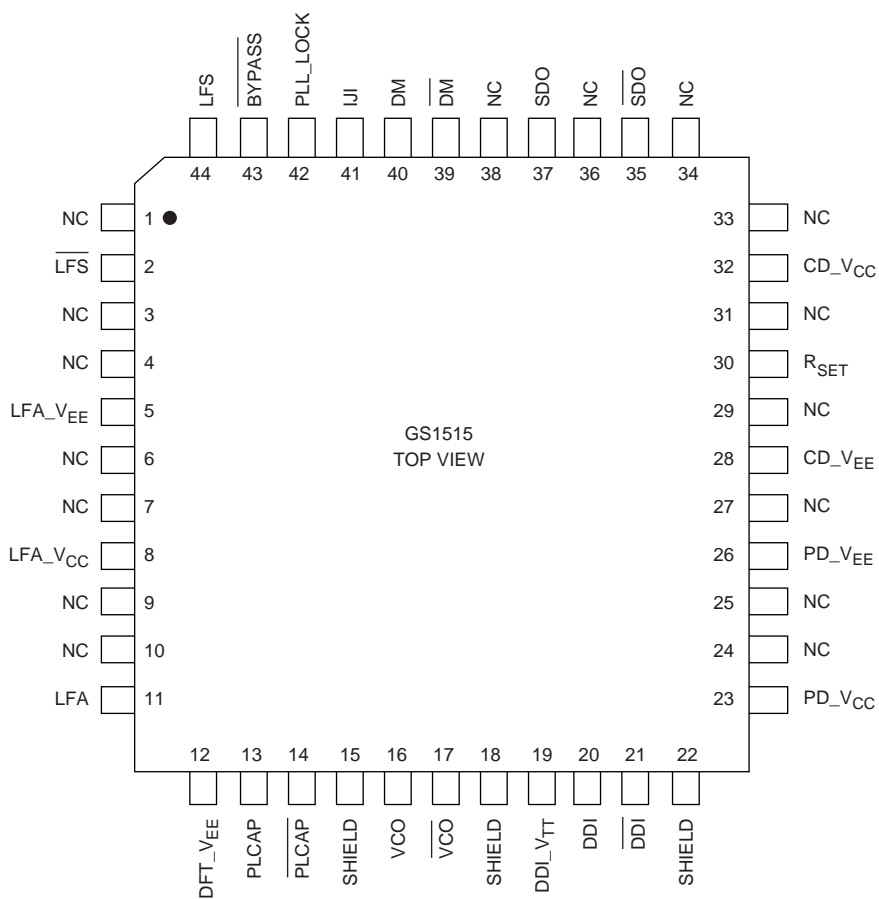
PIN DESCRIPTIONS

| NUMBER	SYMBOL	TYPE	DESCRIPTION
1, 3, 4, 6, 7, 9, 10, 24, 25, 27, 29, 31, 33, 34, 36, 38	NC		No connection. These pins are not bonded to the die.
2	$\overline{\text{LFS}}$	INPUT	Loop filter capacitor connection.
5	LFA_V_{EE}	POWER	Most negative power supply connection - loop filter circuitry.
8	LFA_V_{CC}	POWER	Most positive power supply connection - loop filter circuitry.
11	LFA	OUTPUT	Control signal output: control voltage for the external GO1515 VCO.
12	DFT_V_{EE}	POWER	Most negative power supply connection - that enables the jitter demodulator functionality, this pin should be connected to ground. If left floating, the DM function is disabled resulting in a current saving of 340μA.
13, 14	PLCAP, $\overline{\text{PLCAP}}$	INPUT	Control signal input: PLL lock detect time constant capacitor connection.
15, 18, 22	SHIELD		No connect pins separating the DDI inputs, the VCO inputs and the loop filter components to improve noise performance. Connection to be made to ground in most cases depending upon PCB performance.
16, 17	VCO, $\overline{\text{VCO}}$	INPUT	Control signal inputs: differential inputs for the external VCO. The GO1515 has single ended output. In this case, the $\overline{\text{VCO}}$ input is decoupled to ground.
19	DDI_V_{TT}	INPUT	Centre tap of the two 50Ω on-chip termination resistors between the DDI and the $\overline{\text{DDI}}$ inputs.
20, 21	DDI, $\overline{\text{DDI}}$	INPUT	Differential inputs for the serial digital signals.
23	PD_V_{CC}	POWER	Most positive power supply connection - phase detector circuitry.
26	PD_V_{EE}	POWER	Most negative poser supply connection - phase detector circuitry.
28	CD_V_{EE}	POWER	Most negative power supply connection - cable driver circuitry.
30	R_{SET}	INPUT	Resistor used to set the serial digital output signal swing. It is connected between here and ground with a very short trace length.
32	CD_V_{CC}	POWER	Most positive power supply connection - cable driver circuitry.
35, 37	$\overline{\text{SDO}}$, SDO	OUTPUT	Differential serial digital outputs from the on-chip cable driver. These outputs require 75Ω pull-up resistors.
39, 40	$\overline{\text{DM}}$, DM	OUTPUT	Diagnostic signal: if the jitter demodulator function is not used, these pins must be left floating.
41	IJI	OUTPUT	Status signal output: indicates the amount of excessive jitter on the incoming DDI and $\overline{\text{DDI}}$ signals.
42	PLL_LOCK	OUTPUT	Status signal output: lock detect and carrier detect: PLL lock indicator output used to indicate when the PLL is locked. This output is TTL compatible. When the PLL_LOCK = LOW, the serial digital outputs are muted.
43	$\overline{\text{BYPASS}}$	INPUT	Control signal input: operational TTL compatible input that controls whether the input DDI and $\overline{\text{DDI}}$ signal is reclocked ($\overline{\text{BYPASS}}$ = HIGH) or is passed through the device, unreclocked ($\overline{\text{BYPASS}}$ = LOW). Muting does not affect the bypassed signal.
44	LFS	INPUT	Loop filter capacitor connection.

GS1515

INPUT / OUTPUT CIRCUITS
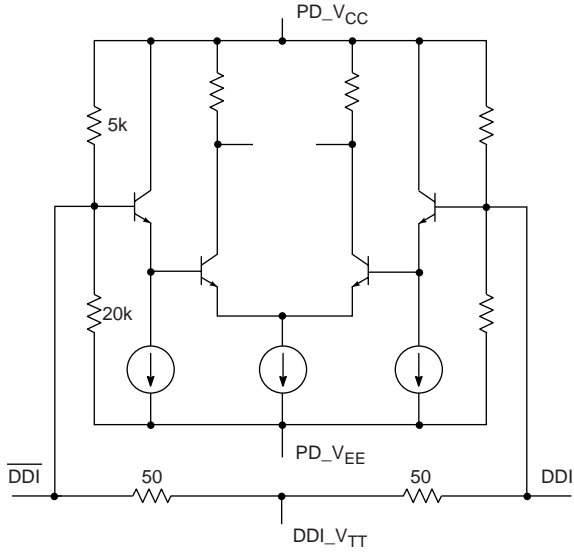
Fig. 1   DDI/$\overline{\text{DDI}}$ Input
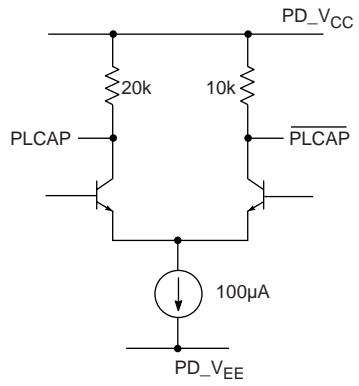
Fig. 4   PLCAP/$\overline{\text{PLCAP}}$ Output
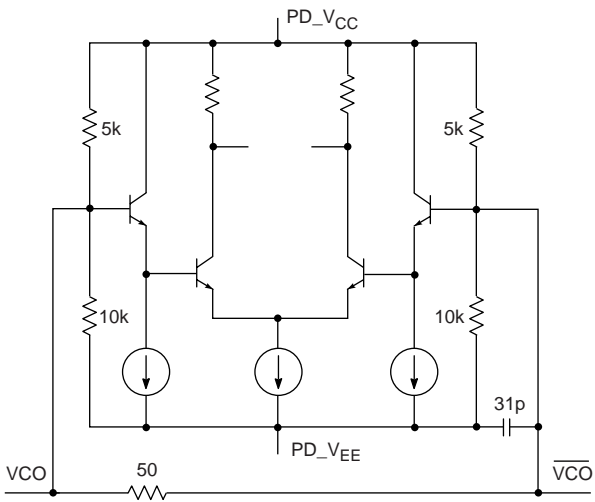
Fig. 2   VCO/$\overline{\text{VCO}}$ Input
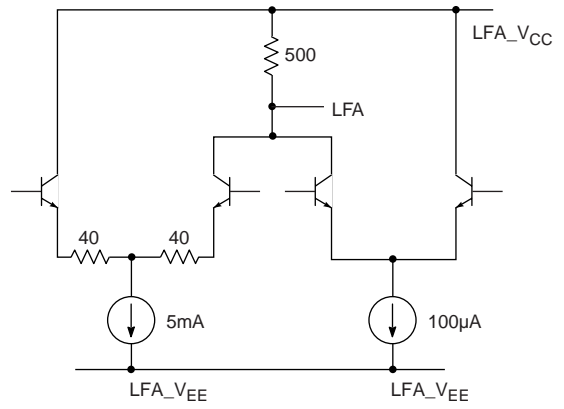
Fig. 5   LFA Circuit
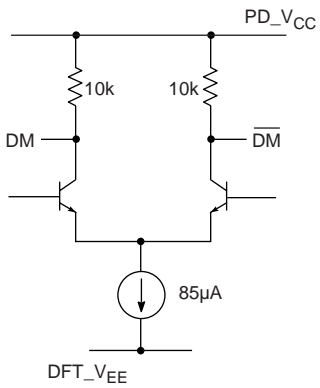
Fig. 3   DM/$\overline{\text{DM}}$ Output

Fig. 6   LFS Output

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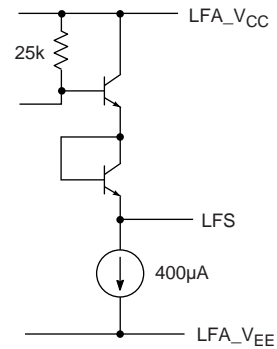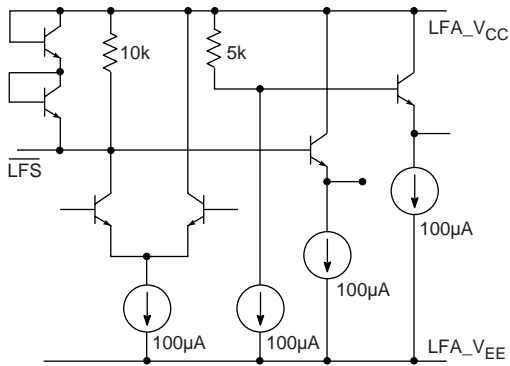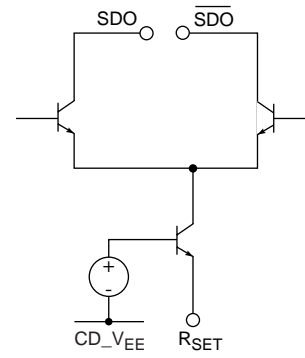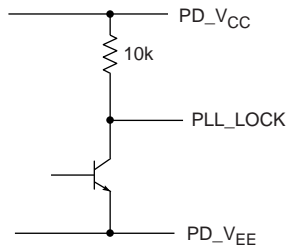
Fig. 7 $\overline{\text{LFS}}$ Input

Fig. 10 SDO/$\overline{\text{SDO}}$ Output

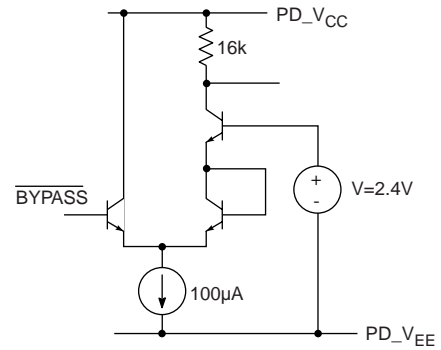All on-chip resistors have ±20% tolerance at room temperature.

Fig. 8 PLL_LOCK Output

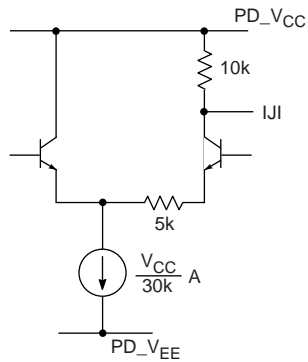Fig. 11 $\overline{\text{BYPASS}}$ Circuit
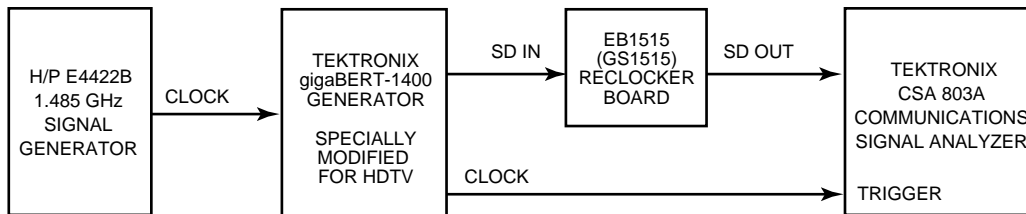
Fig. 9 IJI Output

Fig. 12 Intrinsic Jitter Measurement Set-Up

DETAILED DESCRIPTION

The GS1515 is a single standard re-timer for serial digital HDTV signals at 1.485Gb/s and 1.485/1.001Gb/s.

UNIQUE SLEW PHASE LOCK LOOP (S-PLL):

A unique feature of the GS1515 is the innovative slew phase lock loop (S-PLL). When a step phase change is applied to the PLL, the output phase gains constant rate of change with respect to time. This behavior is termed slew. Figure 13 shows an example of input and output phase variation over time for slew and linear (conventional) PLLs. Since the slewing is a non-linear behavior, the small signal analysis cannot be done in the same way as it is done for the standard PLL. However, it is still possible to plot input jitter transfer characteristics at a constant input jitter modulation.
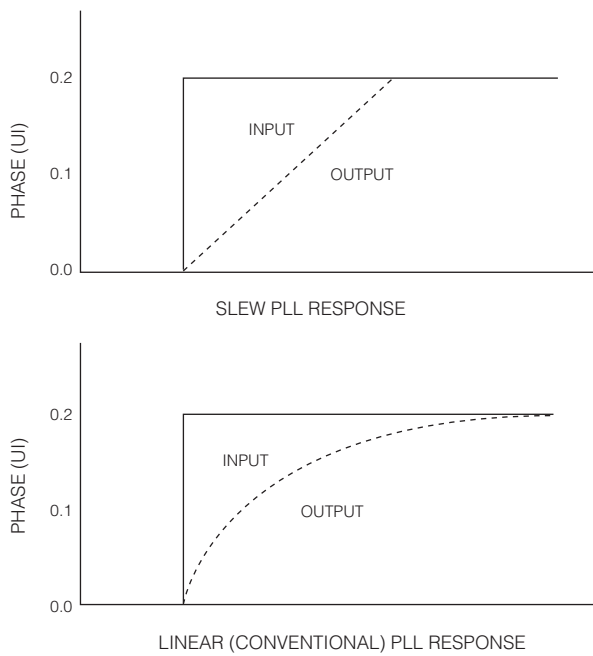
Fig. 13   PLL Characteristics

Slew PLLs offer several advantages such as excellent noise immunity. Because of the infinite bandwidth for an infinitely small input jitter modulation (or jitter introduced by VCO), the loop corrects for that immediately thus the small signal noise of the VCO is cancelled. The GS1515 uses an extremely clean, external VCO called the GO1515 (reference should be made to the GO1515 Data Sheet). In addition, the bi-state digital phase detector provides constant loop bandwidth that is independent of the data transition density. The loop bandwidth of a conventional tri-stable charge pump drops with reducing data transitions. During pathological signals, the data transition density reduces from 0.5 to 0.05, but the slew PLL's performance does not change.

Lastly, because most of the PLL circuitry is digital, it is very robust similar to any other digital systems which are generally more robust than their analog counterparts. Additionally signals like DM/$\overline{DM}$ which represent the internal functionality can be generated without adding additional artifacts. Thus, system debugging is also possible with these features. The complete slew PLL is made up of several blocks including the phase detector, the charge pump and an external Voltage Controlled Oscillator (VCO). For the device descriptions, reference should be made to the Functional Block Diagram on the cover page of the data sheet.

INPUT BUFFER

The input buffer is a self-biased circuit. On-chip 50Ω termination resistors provide a seamless interface for other HD-LINX™ products such as the GS1504 Adaptive Cable Equalizer.

PHASE DETECTOR

The phase detector portion of the slew PLL used in GS1515 is a bi-level digital phase detector. It indicates whether the data transition occurred before or after with respect to the falling edge of the internal clock. When the phase detector is locked, the data transition edges are aligned to the falling edge of the clock. The input data is then sampled by the rising edge of the clock, as shown in Figure 14. In this manner, the allowed input jitter is 1UI p-p in an ideal situation. However, due to setup and hold time, the GS1515 typically achieves 0.8UI p-p input jitter tolerance without causing any errors in this block. When the signal is locked to the internal clock, the control output from the phase detector is refreshed at the transition of each rising edge of the data input. During this time, the phase of the clock drifts in one direction.
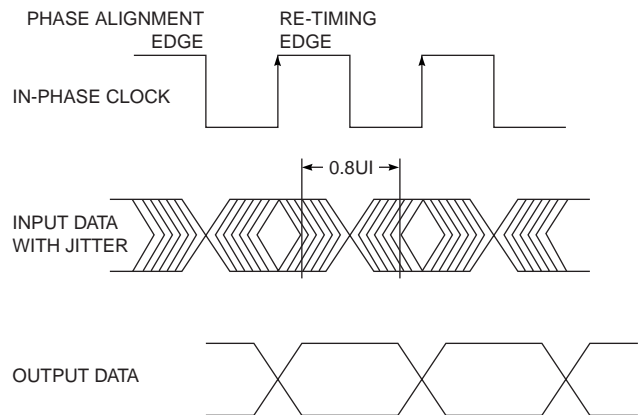

Fig. 14   Phase Detector Characteristics

During pathological signals, the amount of jitter that the phase detector will add can be calculated. By choosing the proper loop bandwidth, the amount of phase detector induced jitter can also be limited. Typically, for a 1.41MHz loop bandwidth at 0.2UI input jitter modulation, the phase detector induced jitter is about 0.015UIp-p. This is not very significant, even for the pathological signals.

CHARGE PUMP

The charge pump in a slew PLL is different from the charge pump in a linear PLL. There are two main functions of the charge pump. One function is to hold the frequency information of the input data. This information is held by C_{CP1}, which is connected between LFS and $\overline{LFS}$. The other capacitor, C_{CP2} between $\overline{LFS}$ and LFA_GND is used to remove common mode noise. Both C_{CP1}, C_{CP2} should be the same value. The second function of the charge pump is to provide a binary control voltage to the VCO depending upon the phase detector output. The output pin, LFA controls the VCO. Internally there is a 500Ω pull-up resistor, which is driven with a 100µA current called I_P. Another analog current I_F, with 5mA maximum drive proportional to the voltage across the C_{CP1} is applied at the same node. The voltage at the LFA node is V_{LFA_VCC} - 500(I_P+I_F) at any time.

Because of the integrator, I_F changes very slowly, whereas I_P could change at the positive edge of the data transition as often as a clock period. In the locked position, the average voltage at the LFA ($V_{LFA\_VCC} - 500(I_P/2+I_F)$) is such that VCO generates frequency f, equal to the data rate clock frequency. Since I_P is changing all the time between 0A and 100µA, there will be two levels generated at the LFA output.

VCO

The GO1515 is an external hybrid VCO, which has a centre frequency of 1.485GHz and is also guaranteed to provide 1.485/1.001GHz within the control voltage (3.1V – 4.65V) of the GS1515 over process, power supply and temperature. The GO1515 is a very clean frequency source and because of the internal high Q resonator, it is an order of magnitude more immune to external noise as compared to on-chip VCOs.

The VCO gain, Kf, is nominally 16MHz/V. The control voltage around the average LFA voltage will be 500 x I_P/2. This will produce two frequencies off from the centre by f=Kf x 500 x I_P/2.

LOOP BANDWIDTH OPTIMIZATION

Since the feed back loop has only digital circuits, the small signal analysis does not apply to the system. The effective loop bandwidth scales with the amount of input jitter modulation index. The following table summarizes the

relationship between input jitter modulation index and bandwidth when R_{CP1} and C_{CP3} are not used. *See the Typical Application Circuit artwork for the location of R_{CP1} and C_{CP3}.*

INPUT JITTER MODULATION INDEX	BANDWIDTH	BW JITTER FACTOR (jitter modulation x BW)
0.05	5.657MHz	282.9kHzUI
0.10	2.828MHz	282.9kHzUI
0.20	1.414MHz	282.9kHzUI
0.50	565.7kHz	282.9kHzUI

The product of the input jitter modulation (IJM) and the bandwidth (BW) is a constant. In this case, it is 282.9kHzUI. The loop bandwidth automatically reduces with increasing input jitter, which helps in cleaning up the signal as much as possible.

Using a series combination of R_{CP1} and C_{CP3} in parallel to an on-chip resistor (as shown in the Typical Application Circuit) can reduce the loop bandwidth of the GS1515. The parallel combination of the resistor is directly proportional to the bandwidth factor. For example, the on-chip 500Ω resistor yields 282.9kHzUI. If a 50Ω resistor is connected in parallel, the effective resistance will be (50 ll 500) 45.45Ω. This resistance yields a bandwidth factor of [282.9 X (45.45/500)] = 25.72kHzUI. The capacitance C_{CP3} in series with the R_{CP1} should be chosen such that the RC factor is 50µF. For example, R_{CP1}=50Ω would require C_{CP3}=1µF.

The synchronous lock time increases with reduced bandwidth. Nominal synchronous lock time is equal to $[0.25 \times \sqrt{2}$ /Bandwidth factor]. That is, the default bandwidth factor (282.9kHzUI) would yield 1.25µs. For 25.72kHzUI, the synchronous lock time is 0.3535/25.72k=13.75µs. Since the C_{CP1}, C_{CP2} and C_{CP3} are also charged, it is measured to be about 11µs which is slightly less than the calculated value of 13.75µs.

The Kf of the VCO (GO1515) is specified with a minimum of 11MHz/V and maximum of 21MHz/V which is about ±32% variation. The 500 x I_P/2 will vary about ±10%. The resulting bandwidth factor would approximately vary by ±45% when no R_{CP1} and C_{CP3} are used. I_P by itself may vary by 30% so the variability for lower bandwidths will increase by an additional ±30%.

The C_{CP1} and C_{CP2} capacitors should be changed with reduced bandwidths. Smaller C_{CP1} and C_{CP2} capacitors would result in jitter peaking, lower stability, less probability of locking but at the same time lowering the asynchronous

lock time. Therefore, there is a trade-off between asynchronous lock time and jitter peaking/stability. These capacitors should be as large as possible for the allowable lock time and should be no smaller than the allowed value. With the recommended values, jitter peaking of less than 0.1dB has been measured at the lower loop bandwidth as shown in Figure 15. At higher loop bandwidths, it is difficult to measure jitter peaking because of the limitation of the measurement unit.
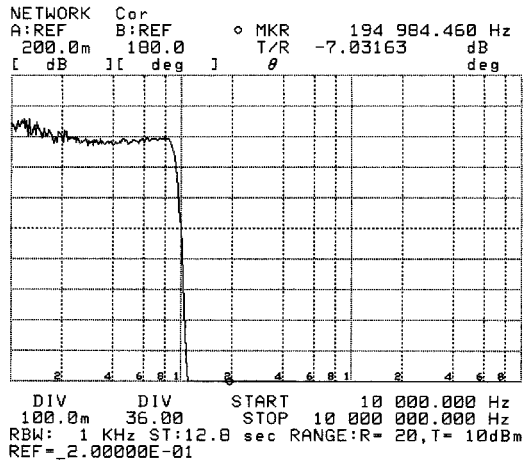

Fig. 15 Typical Jitter Peaking

However, because relatively larger C_{CP1} and C_{CP2} capacitors can be used, over-damping of the loop response occurs. An accurate jitter peaking measurement of 0.1dB for the GS1515 requires the modulation source to have a constant amount of jitter modulation index (within 0.1dB or 1.2%) over the frequency range beyond the loop bandwidth.

It has been determined that for 282.9kHzUI, the minimum value of the C_{CP1} and C_{CP2} capacitors should be no less than 0.5µF. For added margin, 1µF capacitors are recommended. The 1µF value gives a lock time of about 60ms in one attempt. For 25.72kHzUI, these capacitors should be no less than 5.6µF. This would result in 340ms of lock time. If needed, extra margin could be built by increasing these capacitors at the expense of a longer asynchronous lock time.

Bandwidths lower than 129kHz at 0.2UI modulation have not been characterized, but it is believed that the bandwidth could be further lowered. Since a lower bandwidth has less correction for noise, extra care should be taken to minimize board noise. Figures 16 and 17 show the two measured loop bandwidths at these two settings. Table 1 summarizes the two bandwidth settings.
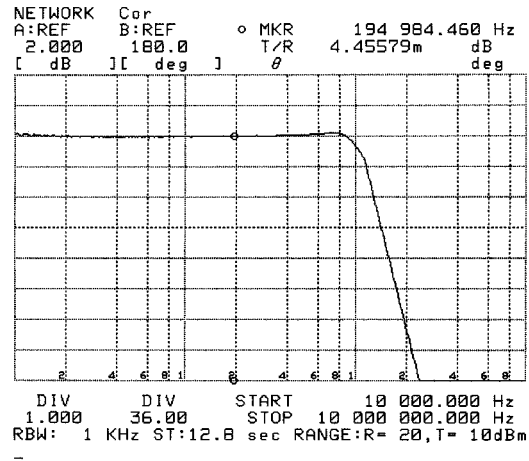

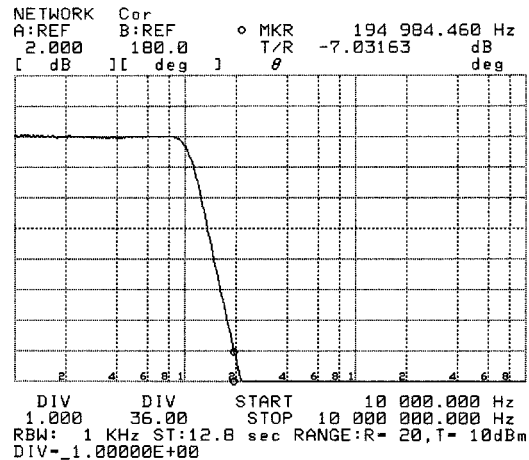Fig. 16 Typical Jitter Transfer Curve
at setting A in Table 1

Fig. 17 Typical Jitter Transfer Curve
at setting B in Table 1

.

TABLE 1: Loop Bandwidth Setting Options

	RCP1	CCP3	CCP1	CCP2	BW FACTOR	BW at 0.2UI JITTER MODULATION INDEX	ASYNCHRONOUS	SYNCHRONOUS
A	Open	Open	1.0	1.0	282.9kHz	1.41MHz	60ms	1.25µs
B	50	1.0	5.6	5.6	25.72kHz	129kHz	340ms	11.0µs

PHASE LOCK

The phase lock circuit is used to determine the phase locked condition. It is done by generating a quadrature clock by delaying the in-phase clock (the clock whose falling edge is aligned to the data transition) by 166ps (0.25UI at 1.5GHz) with the tolerance of 0.05UI. When the PLL is locked, the falling edge of the in-phase clock is aligned with the data edges as shown in Figure 18. The quadrature clock is in a logic high state in the vicinity of input data transitions. The quadrature clock is sampled and latched by positive edges of the data transitions. The generated signal is low pass filtered with an RC network. The R is an on-chip 20kΩ resistor and C_{PL} is an external capacitor (recommended value 10nF). The time constant is about 67µs, or more than a video line.
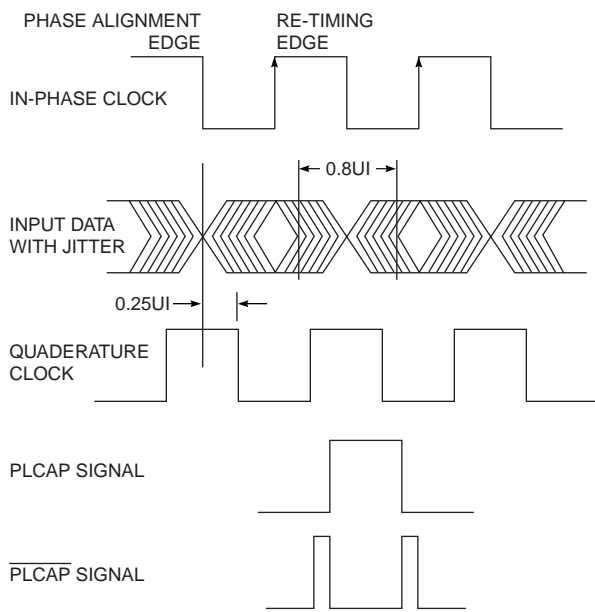

Fig. 18   PLL Circuit Principles

If the signal is not locked, the data transition phase could be anywhere with respect to the internal clock or the quadrature clock. In this case, the normalized filtered sample of the quadrature clock will be 0.5. When VCO is locked to the incoming data, data will only sample the quadrature clock when it is logic high. The normalized filtered sample quadrature clock will be 1.0. We chose a threshold of 0.66 to generate the phase lock signal. Because the threshold is lower than 1, it allows jitter to be bigger than 0.5UI before the phase lock circuit reads it as "not phase locked".

INPUT JITTER INDICATOR (IJI)

This signal indicates the amount of excessive jitter (beyond the quadrature clock window 0.5UI), which occurs beyond the quadrature clock window (see Figure 18). All the input data transitions occurring outside the quadrature clock window, will be captured and filtered by the low pass filter as mentioned in the Phase Lock section. The running time

average of the ratio of the transitions inside the quadrature clock and outside the quadrature is available at the PLCAP/$\overline{PLCAP}$ pins. A signal, IJI, which is the buffered signal available at the PLCAP is provided so that loading does not effect the filter circuit. The signal at IJI is referenced with the power supply such that the factor V_{IJI}/V_{CC} is a constant over process and power supply for a given input jitter modulation. The IJI signal has 10kΩ output impedance. Figure 19 shows the relationship of the IJI signal with respect to the sine wave modulated input jitter.

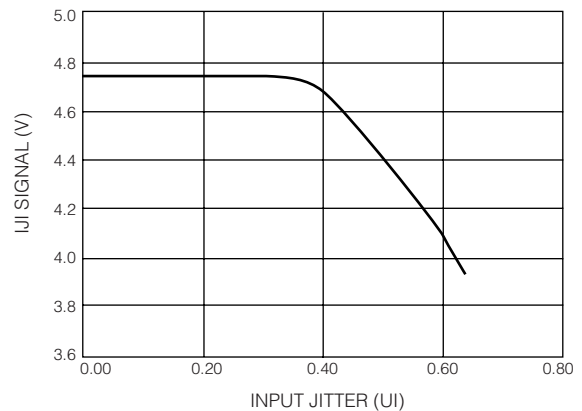| P-P SINE WAVE JITTER IN UI	IJI VOLTAGE
0.00	4.75
0.15	4.75
0.30	4.75
0.39	4.70
0.45	4.60
0.48	4.50
0.52	4.40
0.55	4.30
0.58	4.20
0.60	4.10
0.63	3.95

Fig. 19   Input Jitter Indicator (Typical at T_A = 25°C)

LOCK LOGIC

Logic is used to produce the PLL_LOCK signal which is based on the LFS signal and phase lock signal. When there is not any data input, the integrator will charge and eventually saturate at either end. By sensing the saturation of the integrator, it is determined that no data is present. If either data is not present or phase lock is low, the lock signal is made low. Logic signals are used to acquire the frequency by sweeping the integrator. Injecting a current

into the summing node of the integrator achieves the sweep. The sweep is disabled once phase lock is asserted. The direction of the sweep is also changed once LFS saturates at either end.

MUTE

The logic controls the mute block whenever the PLL_LOCK signal has a LOW logic state. Whenever the mute signal is asserted, previous state of the output is latched.

BYPASS

The BYPASS block bypasses the re-clocked/mute path of the data whenever a logic low input is applied to the BYPASS input. In the bypass mode, the mute does not have any effect on the outputs. Also, in the bypass mode, the internal PLL still locks to a valid HDTV signal and would show PLL_LOCK.

CABLE DRIVER

The output of the GS1515 is a dual/complimentary current mode cable driver stage. The output swing and impedance can be varied. The following table may be used to select the R_{SET} resistor for the desired line impedance. Linear interpolation can be used to determine the specific value of the resistor for a given output swing at the load impedance. For linear interpolation, either Figure 20 or the information in Table 2 should be used. The admittance should be found and then, by inverting the admittance, a resistor value for the R_{SET} can be found. The output can be used as dual 0.8V 75Ω cable drivers. It can also be used as a differential transmission line driver. In this case, the pull-up resistor should match the impedance of the transmission line because the pull-up resistor acts as the source impedance. When it is used in this case, a higher value of R_{SET} resistor could be used in order to reduce the swing and to save power. Other HD-LINX™ products can handle such low input swings. It should be noted that the minimum R_{SET} resistor cannot be less than 50Ω for reliability reasons because of higher current density.
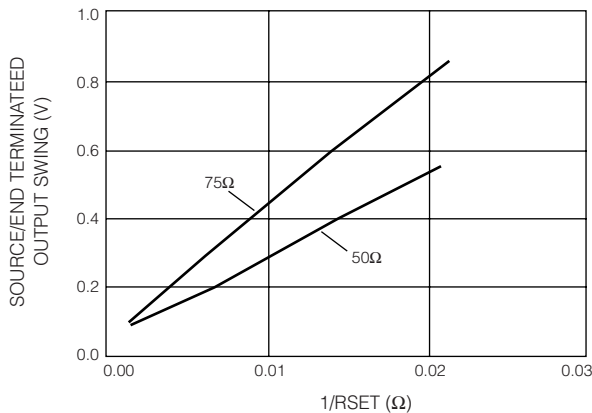

Fig. 20   Signal Swing for Various R_{SET} Admittances

When the outputs are used to differentially drive some other device such as the GS1508, it is recommended to use 50Ω transmission lines with the smallest possible signal swing while allowing 10% variation at the output swing to select the right choice of the R_{SET} resistor. To drive the GS1508, the recommended R_{SET} resistor is 150Ω. There is no need to compensate for the return-loss in this situation. The uncompensated waveform at the output is shown in Figure 21.
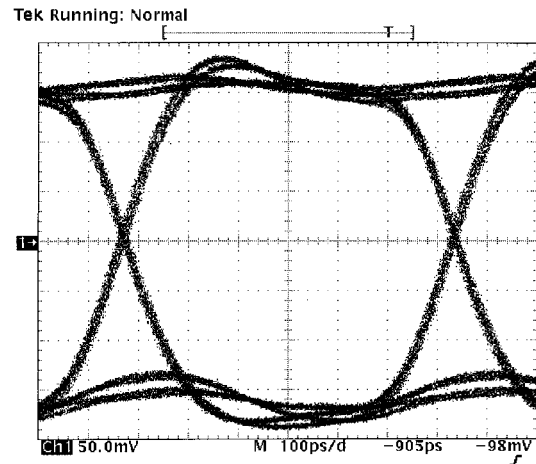

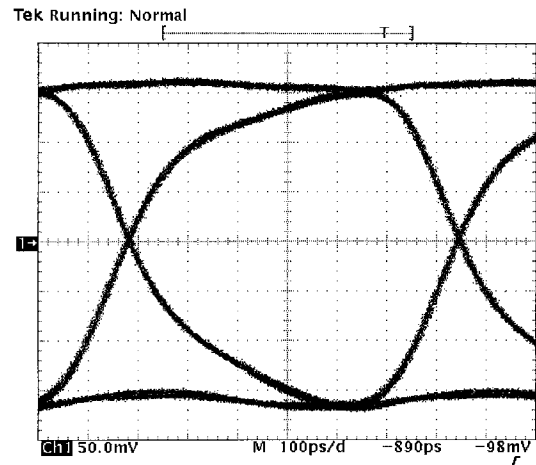Fig. 21   Uncompensated Output Eye Waveform

Fig. 22   Compensated Output Eye Waveform

NOTE: Figures 21 and 22 show the waveforms on an oscilloscope using a 75Ω to 50Ω pad.

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TABLE 2: R$_{SET}$ Values for Various Output Load Conditions

R$_{SET}$ RESISTOR	ADMITTANCE (g) OF THE R$_{SET}$ RESISTOR (= 1/R$_{SET}$ RESISTOR)	OUTPUT CURRENT	TRANSMISSION LINE, TERMINATED AT THE END. (PULL-UP RESISTOR AT THE SOURCE = 75Ω)	TRANSMISSION LINE, TERMINATED AT THE END. (PULL-UP RESISTOR AT THE SOURCE = 50Ω)
500.0Ω	0.0020	2.506mA	0.094V	0.063V
150.0Ω	0.0067	7.896mA	0.296V	0.197V
75.0Ω	0.0133	15.161mA	0.569V	0.379V
53.6Ω	0.0187	20.702mA	0.776V	0.517V
52.3Ω	0.0192	21.216mA	0.796V	0.530V
49.9Ω	0.0200	22.032mA	0.826V	

JITTER DEMODULATION (DM)

The differential jitter demodulation (DM) signal is available at the DM and $\overline{DM}$ pins. This signal is the phase correction signal of the PLL loop, which is amplified and buffered. If the input jitter is modulated, the PLL tracks the jitter if it is within loop bandwidth. To track the input jitter, the VCO has to be adjusted by the phase detector via the charge pump. Thus, the signal which controls the VCO contains the information of the input jitter modulation. The jitter demodulation signal is only valid if the input jitter is less than 0.5UIp-p. The DM/$\overline{DM}$ signals have 10kΩ output impedance, which could be low pass filtered with appropriate capacitors to eliminate high frequency noise. DFT_V$_{EE}$ should be connected to GND to activate DM/$\overline{DM}$ signals.

The DM signals can be used as diagnostic tools. Assume there is an HDTV SDI source, which contains excessive noise during the horizontal blanking because of the transient current flowing in the power supply. In order to discover the source of the noise, one could probe around the source board with a low frequency oscilloscope (Bandwidth < 20MHz) that is triggered with an appropriately filtered DM/$\overline{DM}$ signal. The true cause of the modulation will be synchronous and will appear as a stationary signal with respect to the DM/$\overline{DM}$ signal.

Figure 23 shows an example of such a situation. An HDTV SDI signal is modulated with a modulation signal causing about 0.2UI jitter in Figure 23 (Channel 1). The GS1515 receives this signal and locks to it. Figure 23 (Channel 2) shows the DM signal. Notice the wave shape of the DM signal, which is synchronous to the modulating signal. The DM/$\overline{DM}$ signal could also be used to compare the output jitter of the HDTV signal source.
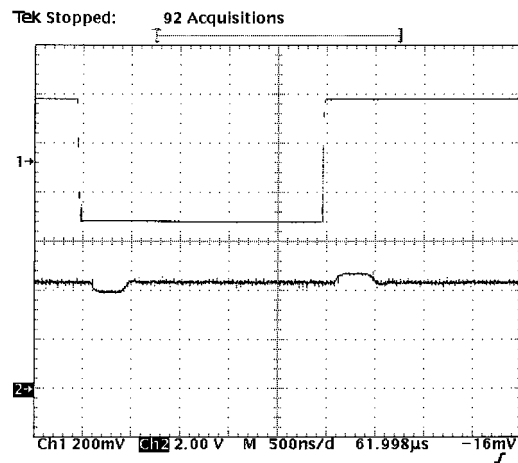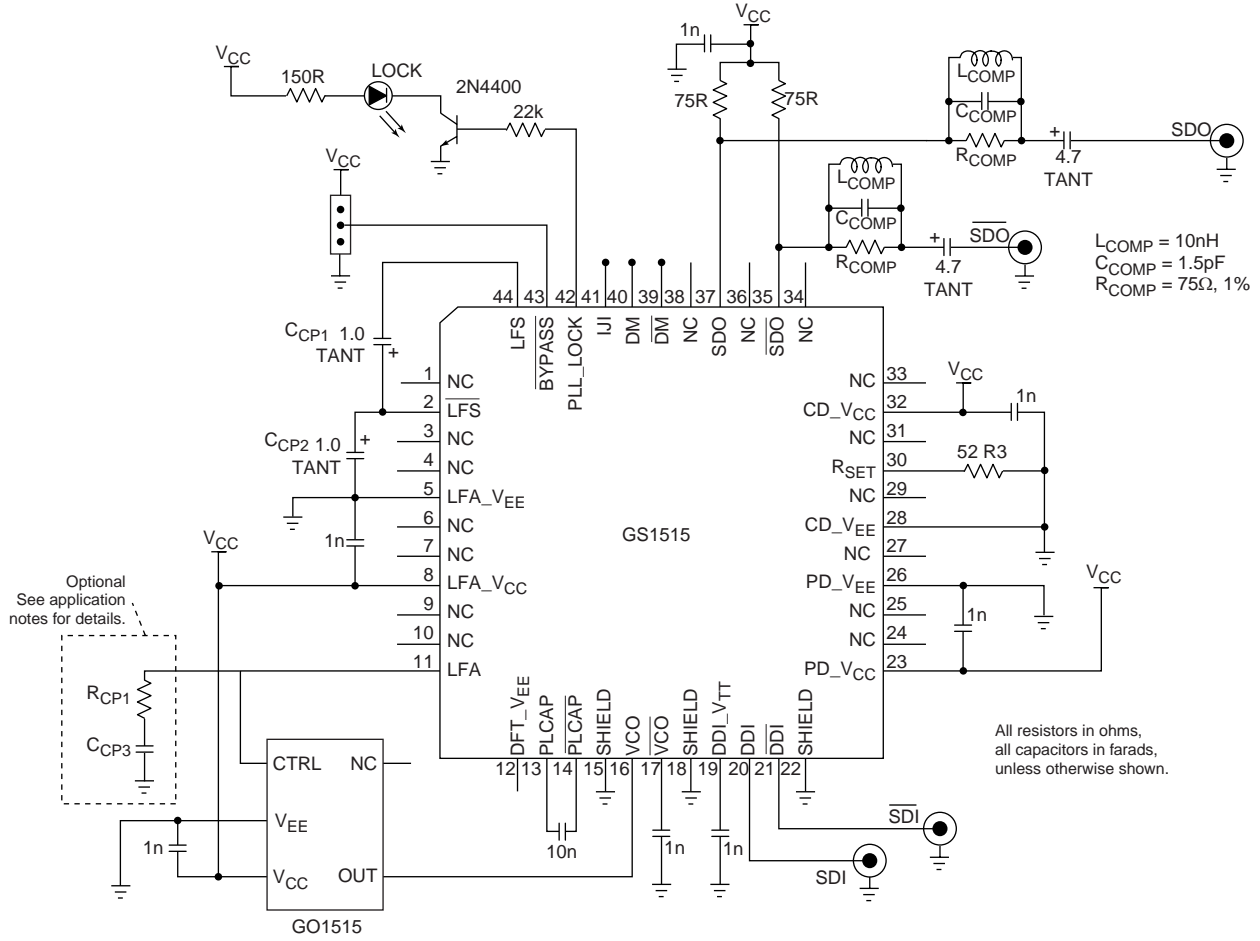

Fig. 23   Jitter Demodulation Signal

POWER SUPPLY NOISE REDUCITON

See Application Note 522-61.

TYPICAL APPLICATION CIRCUIT

L_{COMP} = 10nH
C_{COMP} = 1.5pF
R_{COMP} = 75Ω, 1%

All resistors in ohms, all capacitors in farads, unless otherwise shown.

The figure above shows the recommended application circuit for the GS1515. The external VCO is the GO1515 and is specifically designed to be used with the GS1515. Figures 24 through 28 show an example PC board layout of the GS1515 IC and the GO1515 VCO. This application board layout does not reflect every detail of the typical application circuit but is used as a general guide to the location of the critical parts. *For further circuit and layout details, refer to the EB1504/15 Evaluation Board Application Note.*
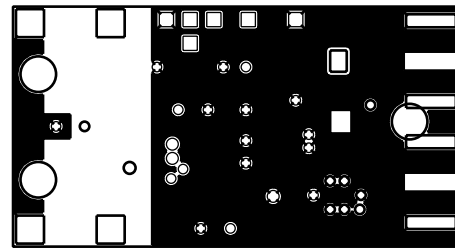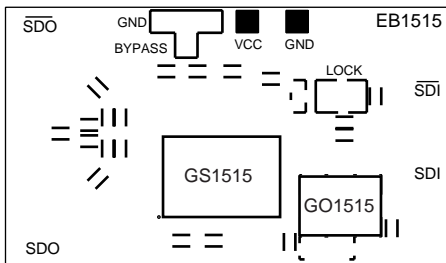

Fig. 25   Ground Layer
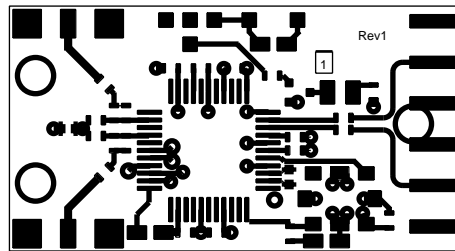

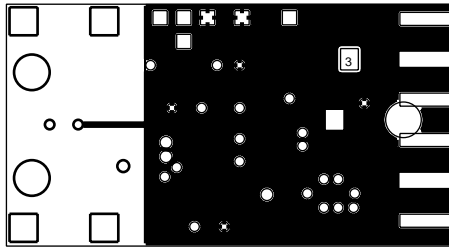Fig. 24   Component Placement

Fig. 26   Top Copper Layer

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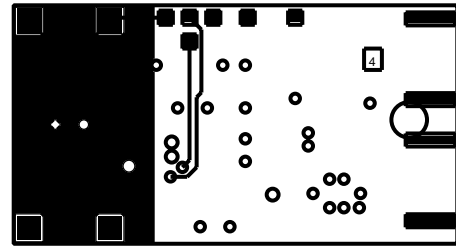
Fig. 27   Power Layer

Fig. 28 Bottom Copper Layer

EXTERNAL PCB AFFECTS

RETURN LOSS

In the application where the GS1515 directly drives a cable, it is possible to achieve an output return loss (ORL) of about 17dB to 1.485GHz. Care should be taken with the PCB layout. It is suggested to use the EB1515 as a reference layout. The use of very small '608' surface mount components and short distances between the components will help in designing high frequency circuits. Openings in the ground plane helps reduce PCB parasitic capacitance. For best matching, a 10nH inductor in parallel with a 75Ω resistor and a 1.5pF capacitor matches the 75Ω cable impedance. The inductor and resistor cancel the parasitic capacitance while the capacitor cancels the inductive effect of the bond wire. In order to verify the performance of any layout, a return loss measurement should be done by shorting the inductor with a piece of wire, without the GS1515 installed.

Unless the artwork is an exact copy of the recommended layout, every design should be verified for output return loss. Changes in the layout should be tweaked until a return loss of 25dB is attained while the GS1515 is not mounted and L_{COMP} is shorted. Once the device is mounted, different inductors should be used to match the parasitic capacitance of the IC. When the right inductor is used, maximum return loss between 5MHz to 800MHz is achievable. Then the shunt capacitor between of 0.5pF to 1.5pF should be tried to increase the return loss between 800MHz and 1.5GHz. The larger inductor causes slower rise/fall time. The larger shunt capacitor causes a kink in the output waveform. Thus, the waveform must be verified to meet SMPTE 292M specifications.

Since there are two levels at the output, depending upon the output state (logic high or low), measurement should be done by latching the outputs in both states. Since the actual output node voltages are different when a stream of data passing as compared to the static situation created to measure return loss, an interpolation is necessary. *See the GS1508 Preliminary Data Sheet for more information.*
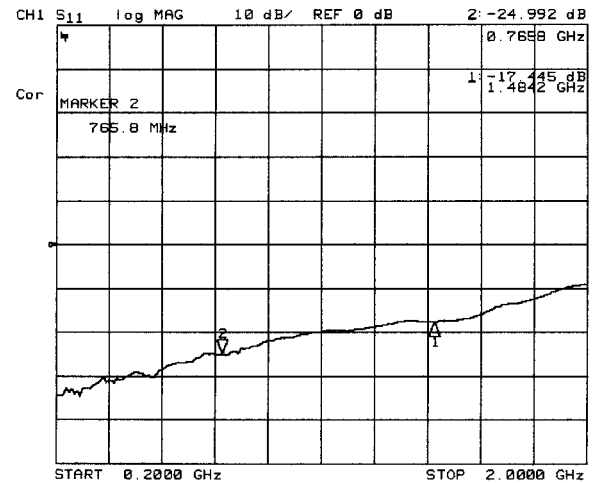

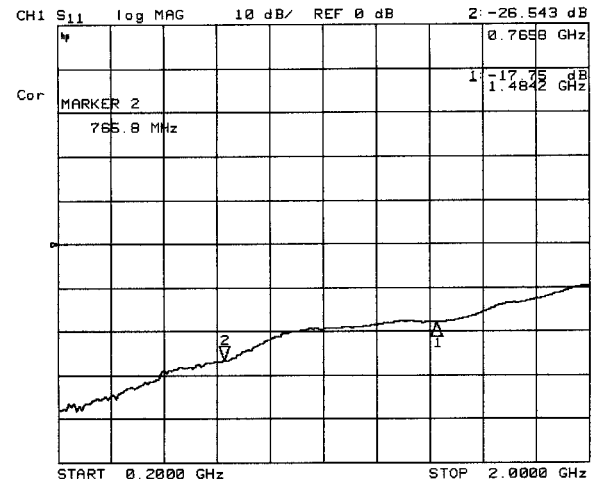Fig. 29   Compensated Output Return Loss at Logic HIGH

Fig. 30   Compensated Output Return Loss at Logic LOW

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OTHER LAYOUT CONSIDERATIONS

The GS1515 is a robust re-timing solution. The layout should be done such that VCO (GO1515) is close to the chip minimizing LFA and VCO traces between GS1515 and GO1515. It is recommended to use the other side of the PCB board whenever possible. The short trace of LFA will reduce noise coupling to the control pin of the VCO. The VCO trace should also be short to reduce EMI radiation from a 1.5GHz clock source. Digital switching noise from CMOS chips should be avoided for best performance. This could be done by providing a moat of at least 50mil wide in all the planes (the GND, V_{CC} and signal layers) (One should be able to see through the moat when the PCB is fabricated). The power supply to the GS1515 Island should be provided through ferrite beads to reject the power supply spikes.

In applications where an adaptive equalizer is used with the GS1515, extra care should be taken to avoid any noise coupling between these two devices. The following recommendations should be followed as layout guides lines. Please refer to the layouts of the EB1515/04 and note the following:

1. The use of power supply islands for GS1504 Adaptive Equalizer.
2. The position of ferrite beads for power supply noise filtering.
3. The ground under the transmission line for GS1504 and GS1515 interface.
4. The transmission line decoupling at the GS1515 end to the transmission line ground.
5. The isolation moat around the transmission line reference ground.

TABLE 3: Application Debugging

PROBLEM	POSSIBLE REASON	SOLUTION
Output Jitter > 80ps	Wrong way of measuring jitter.	Follow jitter measuring procedure as shown in Fig 12.
	Bad source / trigger reference signal.	Follow jitter measuring procedure as shown in Fig 12.
	Power supply noise generated either by on board digital circuit or switch mode DC power supply.	Shut down the digital circuit and power the board from clean voltage regulated supply. The acceptable noise in the V_{CC} is 5mVp-p. If the problem is resolved, filter high frequency noise with ferrite beads and low frequency noise with Inductor and Capacitor. The source of jitter could also be found using diagnostic signal DM as mentioned in the section JITTER DEMODULATION.
	Bypass mode activated.	Apply logic high at the $\overline{\text{BYPASS}}$ pin.
Errors being generated	Bad input jitter.	A. Configure into bypass mode and look for output jitter under infinite persistence for about 5 minutes in a sampling scope, if total jitter including random shots is more than 0.5UI, input jitter is out of specification. Debug circuit, which is driving GS1515.
		B. Probe IJI by a low frequency digital scope to capture any glitch. If glitches are not identified, remove the 10nF PLCAP between PLCAP and $\overline{\text{PLCAP}}$. If glitches are identified, then the sum of jitter of the reclocker and the source is more than 0.5UI. Achieve reclocker jitter around 0.1UI or less and reduce the source jitter less than 0.4UI.

PACKAGE DIMENSIONS
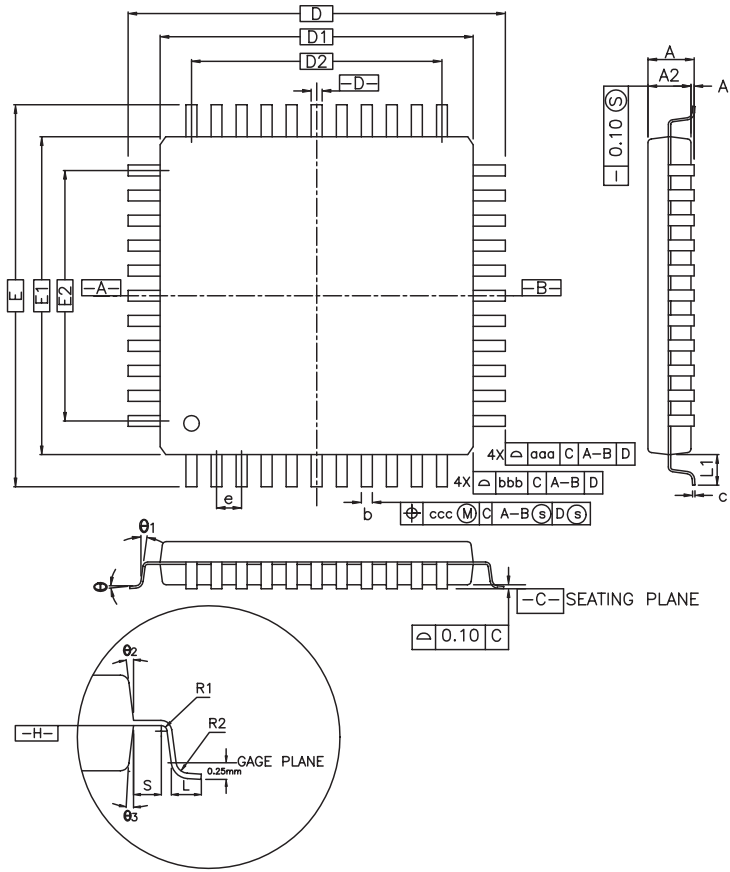
COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	2.55	—	—	0.100
A1	0.15	0.25	0.35	0.006	0.010	0.014
A2	1.80	2.05	2.20	0.071	0.081	0.087
D	13.20 BASIC			0.520 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	13.20 BASIC			0.520 BASIC		
E1	10.00 BASIC			0.394 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2	10° REF			10° REF		
θ3	7° REF			7° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60			0.063		
S	0.20	—	—	0.008	—	—

DOCUMENT IDENTIFICATION

DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:
Added Pb-free and green information.

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