3A, 18V, 500kHz, ACOT™ Step-Down Converter

General Description

The RT6234A/B is a high-efficiency, monolithic synchronous step-down DC-DC converter that can deliver up to 3A output current from a 4.5V to 18V input supply. The RT6234A/B adopts ACOT architecture to allow the transient response to be improved and keep in constant frequency. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. Fault conditions also include output under voltage protection and thermal shutdown.

Ordering Information

RT6234A/B □□□

- Package Type
  QW : WDFN-8L 2x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Option
  H : Hiccup
- A : PSM Mode
  B : PWM Mode

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

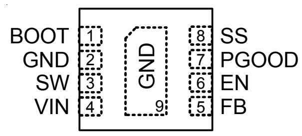
- **Integrated 130mΩ / 70mΩ MOSFETs**
- **4.5V to 18V Supply Voltage Range**
- **500kHz Switching Frequency**
- **ACOT Control**
- **0.8V ± 2% Voltage Reference**
- **Output Adjustable from 0.8V to 6.5V**
- **Monotonic Start-Up into Pre-Biased Outputs**

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

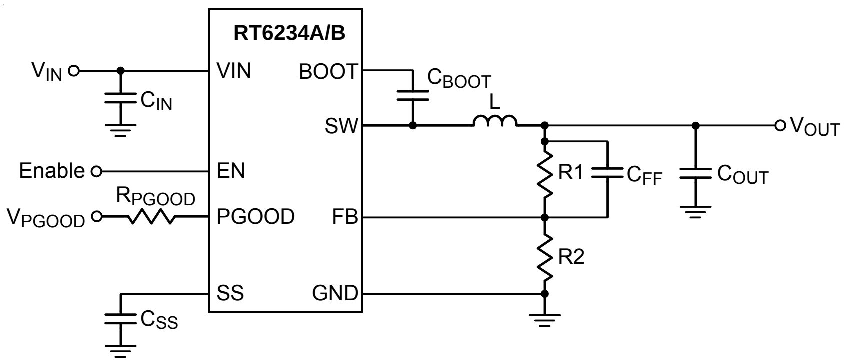
Pin Configuration

(TOP VIEW)



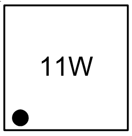
WDFN-8L 2x3

Simplified Application Circuit



Marking Information

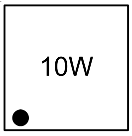
RT6234AHGQW



11 : Product Code

W : Date Code

RT6234BHGQW



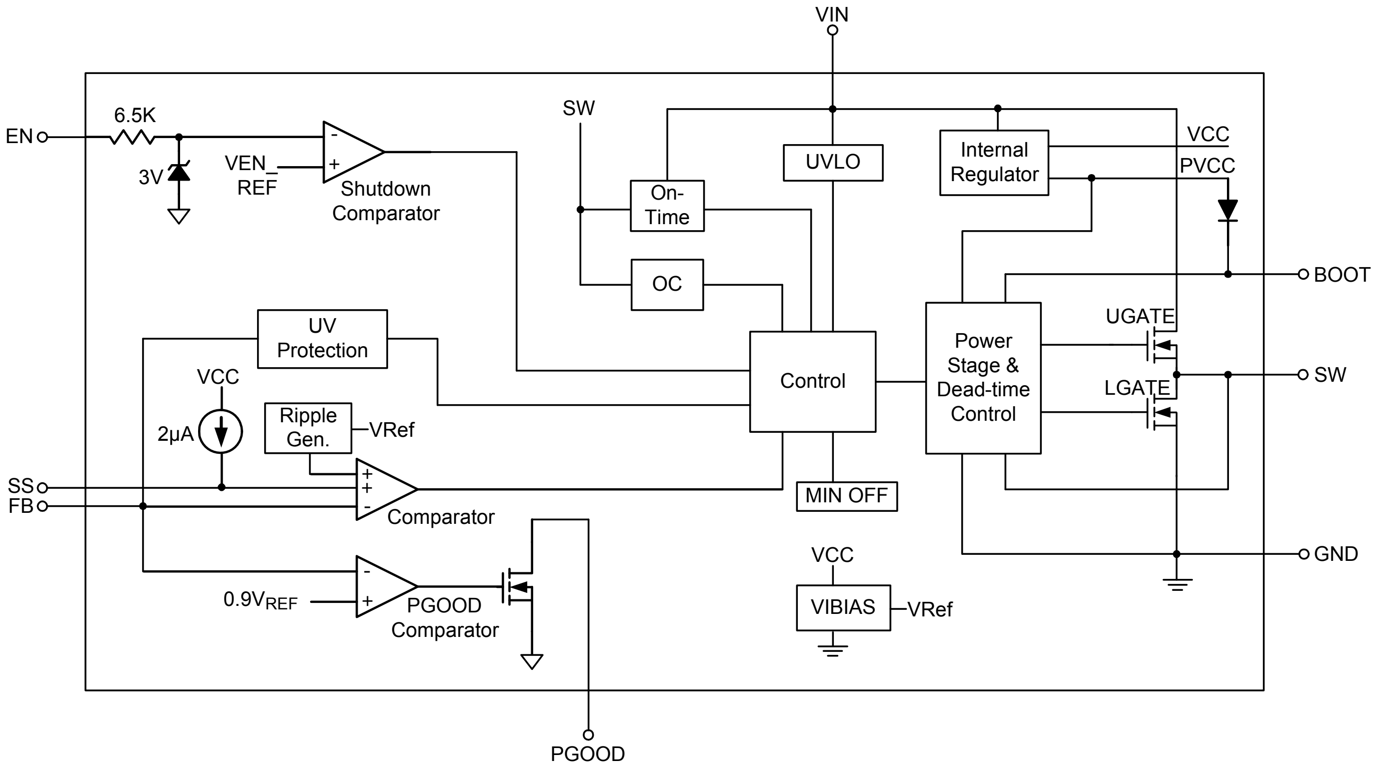
10 : Product Code

W : Date Code

Function Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap, supply for high-side gate driver. Connect a 0.1μF or greater ceramic capacitor between the BOOT pin and SW pin to power the high-side switch.
2, 9 (Exposed Pad)	GND	System ground. Provides the ground return path for the control circuitry and low-side power MOSFET. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	SW	Switch node. SW is the switching node that supplies power to the output and connect the output LC filter from SW pin to the output load.
4	VIN	Power input. Supplies the power switches of the device.
5	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider.
6	EN	Enable control input. Floating this pin or connecting this pin to ground can disable the device and connecting this pin to logic high can enable the device.
7	PGOOD	Power good indicator. This pin is an open-drain logic output that is pulled to ground when the output voltage is lower or higher than its specified threshold under the conditions of OTP, EN shutdown, or during soft-start.
8	SS	Soft-start control input. Connect a capacitor between the SS pin and ground to set the soft-start period.

Functional Block Diagram



Operation

The RT6234A/B is a synchronous step-down converter with advanced constant on-time control mode. Using the ACOT[TM] control mode can reduce the output capacitance and provide fast transient response. It can minimize the component size without additional external compensation network.

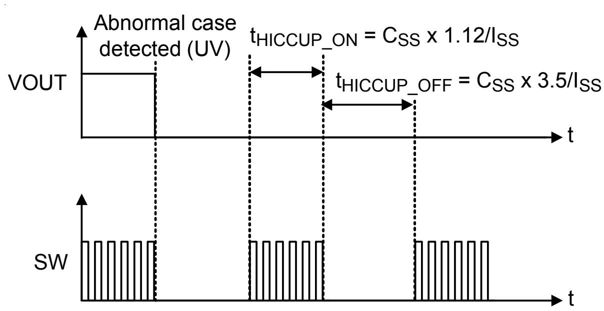
Current Protection

The inductor current is monitored via the internal switches cycle-by-cycle. Once the output voltage drops under UV threshold, the RT6234A/B will enter hiccup mode.

Output Under-Voltage Protection and Hiccup Mode

The RT6234A/B includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 50% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches.

If the output under-voltage condition continues for a period of time, the RT6234A/B will enter output under-voltage protection with hiccup mode. During hiccup mode, the IC will shut down for t_{HICCUP_OFF} (C_{SS} x 3.5/I_{SS}), and then attempt to recover automatically for t_{HICCUP_ON} (C_{SS} x 1.12/I_{SS}). Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.



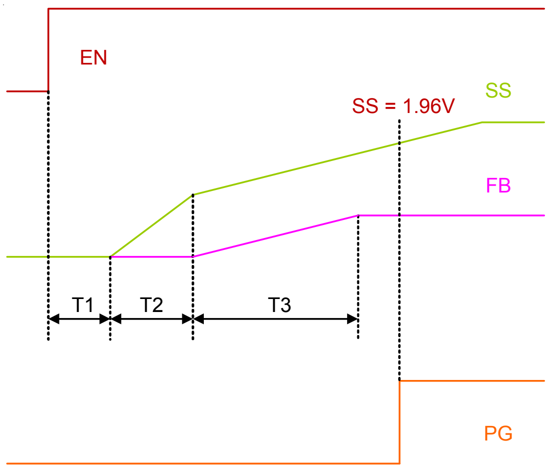
Soft-Start

The RT6234A/B provides adjustable soft-start function. When the EN pin becomes high, the SS charge current (I_{SS}) begins charging the capacitor which is connected from the SS pin to GND (C_{SS}).The soft-start function is used to prevent large inrush current while converter is being powered-up. The soft-start timing can be programmed by the external capacitor C_{SS} between SS and GND. An internal current source I_{SS} (2μA) charges an external capacitor to build a soft-start ramp voltage. The V_{FB} voltage will track the soft-start ramp voltage during soft-start interval. The typical soft-start time is calculated as follows :

Soft-Start time t_{SS} = 50μs + C_{SS} x 0.42 / 8μA + C_{SS} x 1 / I_{SS}

t_{SS} = EN rising to FB settled (T1 + T2 + T3)

Time from EN high to PG signal ready = 50μs + C_{SS} x 0.42/8μA + C_{SS} x 1 / I_{SS} + C_{SS} x 0.54 / I_{SS}.



T1 : EN delay, from EN go high to SS start rising, T1 = 50μs;
T2 : speed up SS, from SS rising to FB start rising, T2 = C_{SS} x 0.42/8μA;
T3 : normal SS, from FB rising to settled, T3 = C_{SS} x 1/ISS;
PG go high after SSOK (SS = 1.96V)

UVLO Protection

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage of VIN is lower than the UVLO falling threshold voltage, the device will be lockout.

Thermal Shutdown

When the junction temperature exceeds the OTP threshold value, the IC will shut down the switching operation. Once the junction temperature cools down and is lower than the OTP lower threshold, the converter will autocratically resume switching.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 20V
- Switch Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
  <50ns ---------- –5V to 25V
- BOOT Voltage, V_{BOOT} ---------- (V_{SW} – 0.3V) to (V_{IN} + 6.3V)
- BOOT to SW, V_{BOOT} – V_{SW} ---------- –0.3V to 6V
- All Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-8L 2x3 ---------- 3.17W
- Package Thermal Resistance (Note 2)
  WDFN-8L 2x3, θ_{JA} ---------- 31.5°C/W
  WDFN-8L 2x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature Range ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Under-Voltage Lockout Threshold-Rising	V_{UVLO}	V_{IN} rising	3.6	3.9	4.2	V
Vin Under-Voltage Lockout Threshold-Hysteresis	ΔV_{UVLO}		--	340	--	mV
Supply Current						
Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0V	--	--	6	μA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V	--	0.8	--	mA
Soft-Start						
Soft-Start Current	I_{SS}		--	2	--	μA
Enable Voltage						
EN Rising Threshold	V_{EN_H}		1.38	1.5	1.62	V
EN Falling Threshold	V_{EN_L}		1.16	1.28	1.4	V
Feedback Voltage						
Feedback Voltage	V_{FB}		784	800	816	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal MOSFET						
High-Side Switch-On Resistance	$R_{DS(ON)\_H}$	$V_{BOOT} - V_{SW} = 4.8V$	--	130	--	mΩ
Low-Side Switch-On Resistance	$R_{DS(ON)\_L}$		--	70	--	mΩ
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}		--	7.5	--	A
Low-Side Switch Valley Current Limit	I_{LIM_L}		4	4.8	--	A
Switching Frequency						
Oscillator Frequency	f_{SW}		--	500	--	kHz
On-Time Timer Control						
Maximum Duty Cycle	D_{MAX}		--	90	--	%
Minimum On Time	$t_{ON(MIN)}$		--	60	--	ns
Thermal Shutdown						
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Hysteresis	ΔT_{SD}		--	20	--	°C
Output Under Voltage Protections						
Output Under Voltage Trip Threshold		UVP detect	45	50	55	%
		Hysteresis	--	10	--	%
Power Good						
Power Good Threshold	V_{PGOOD}	FB rising	--	90	--	%
		FB falling	--	85	--	%

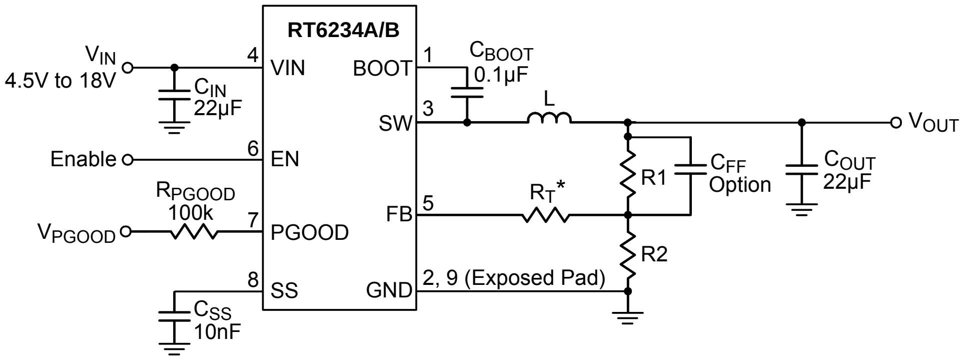
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

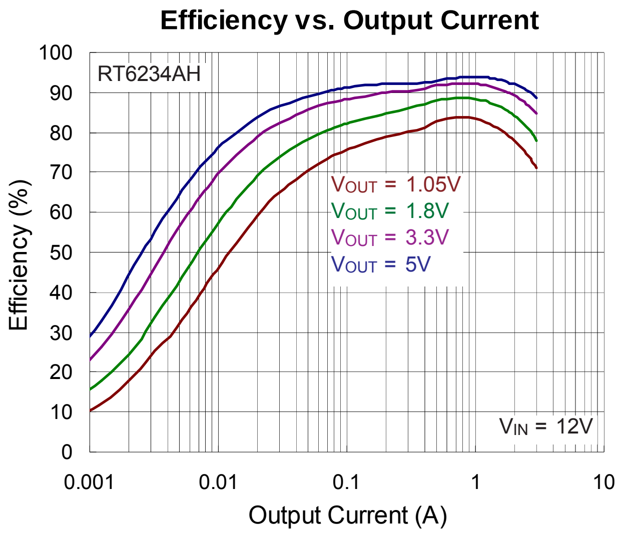


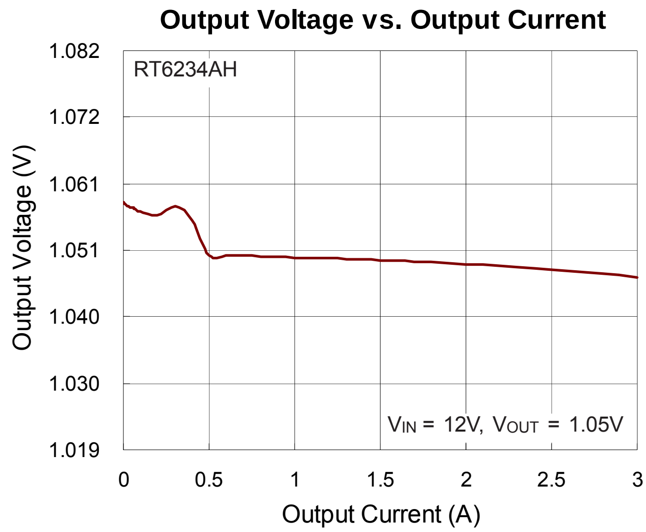
*Note :
When C_{FF} is added, it is necessary to add R_T = 10k between feedback network and chip FB pin.

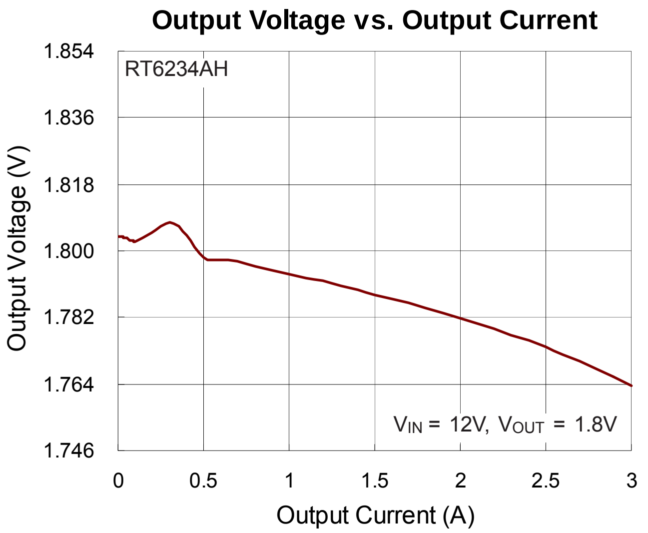
Table 1. Suggested Component Values (V_{IN} = 12V)

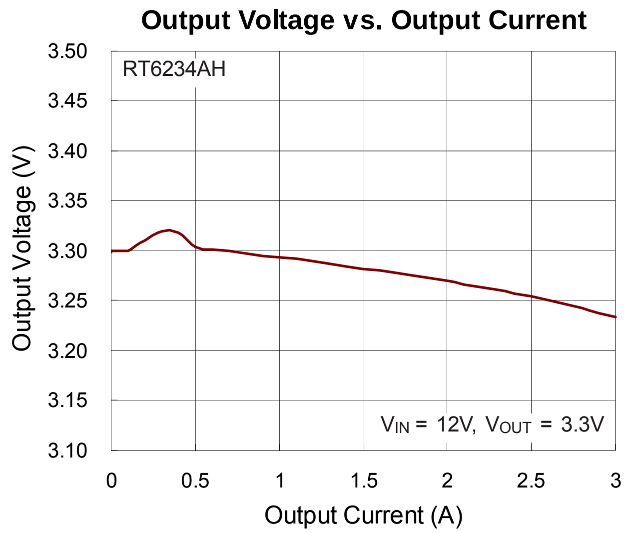
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)	C_{FF} (pF)
1.05	10	32.4	2.2	44	--
1.2	20.5	41.2	2.2	44	--
1.8	40.2	32.4	3.3	44	--
2.5	40.2	19.1	3.3	44	22 to 68
3.3	40.2	13	4.7	44	22 to 68
5	40.2	7.68	4.7	44	22 to 68

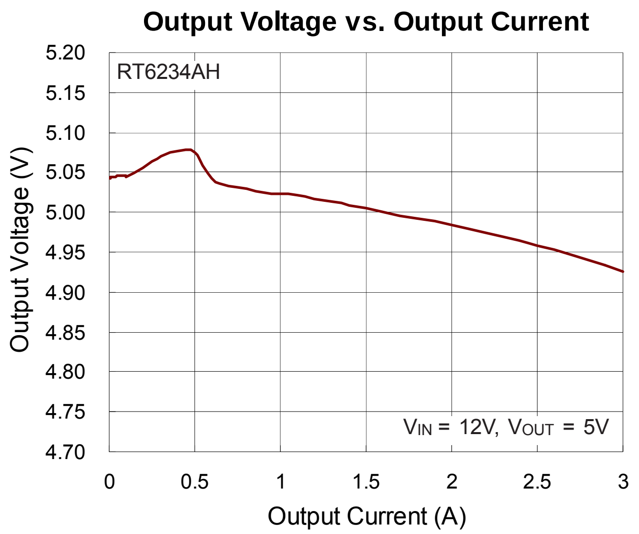
Typical Operating Characteristics

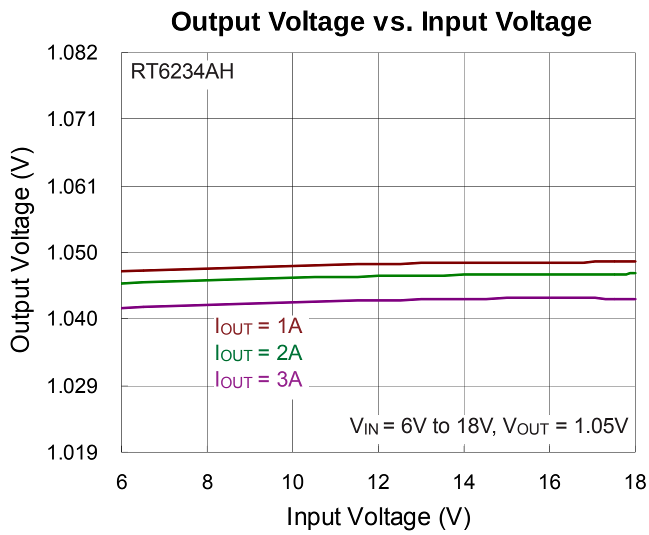




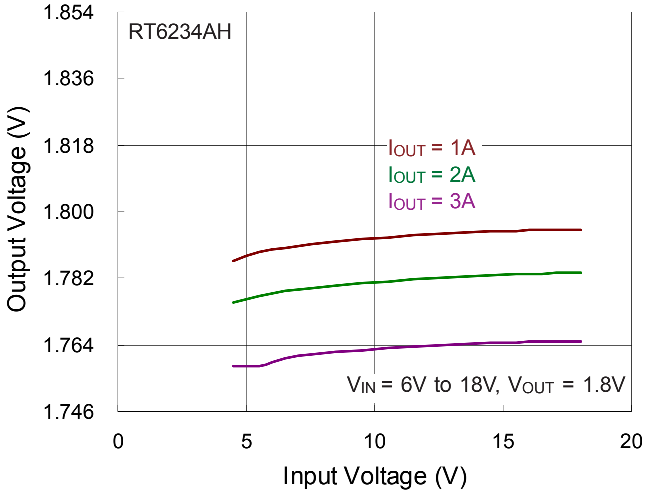




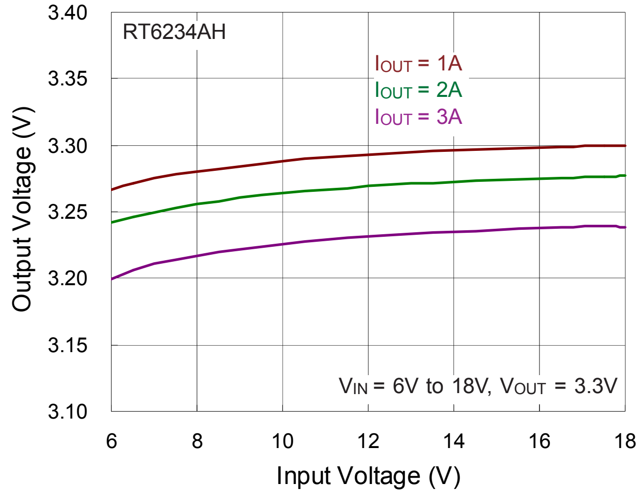




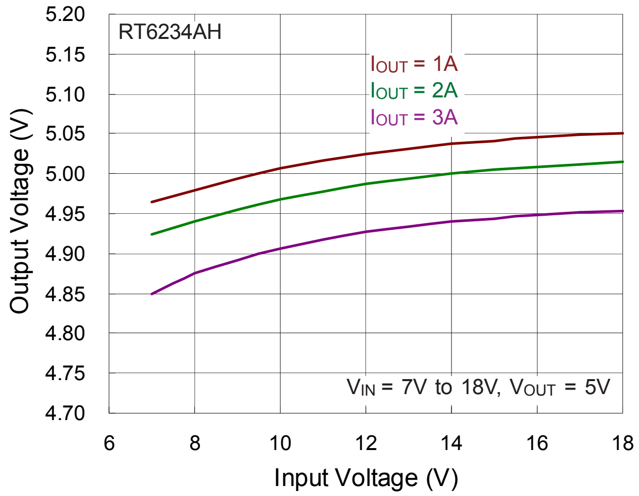
Output Voltage vs. Input Voltage



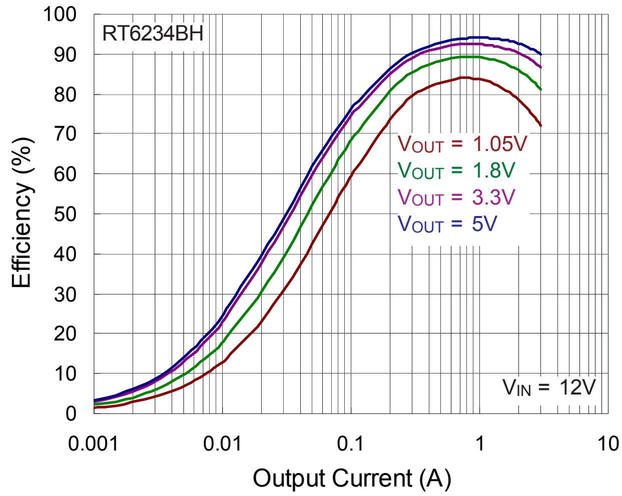
Output Voltage vs. Input Voltage



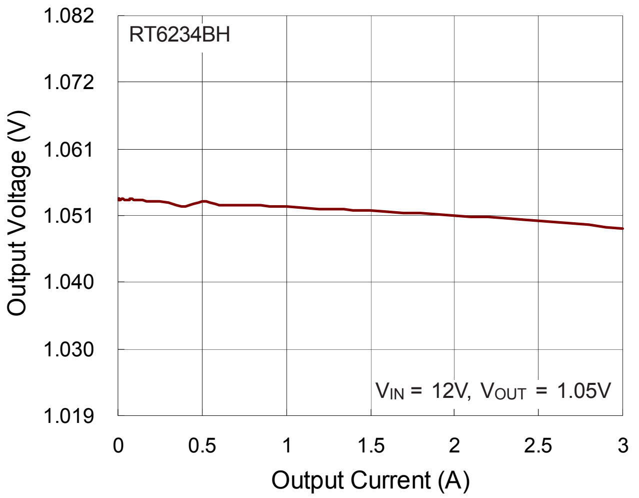
Output Voltage vs. Input Voltage



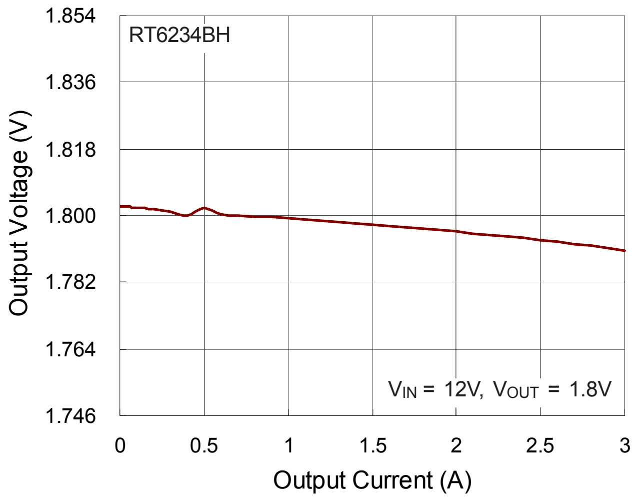
Efficiency vs. Output Current



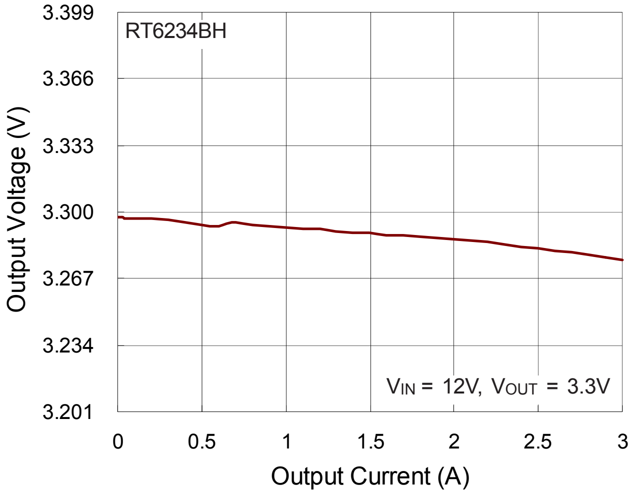
Output Voltage vs. Output Current



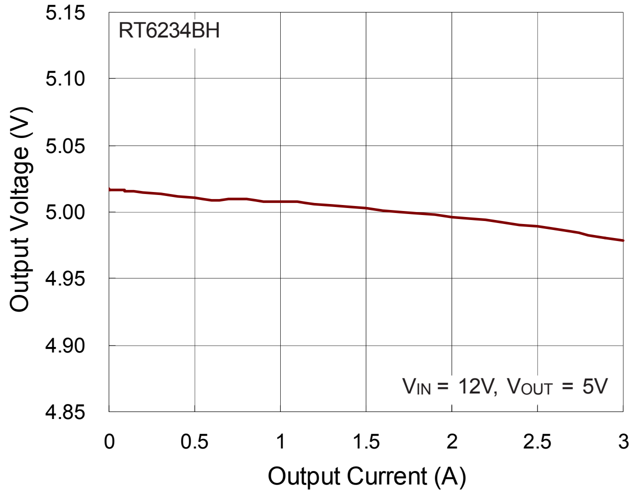
Output Voltage vs. Output Current



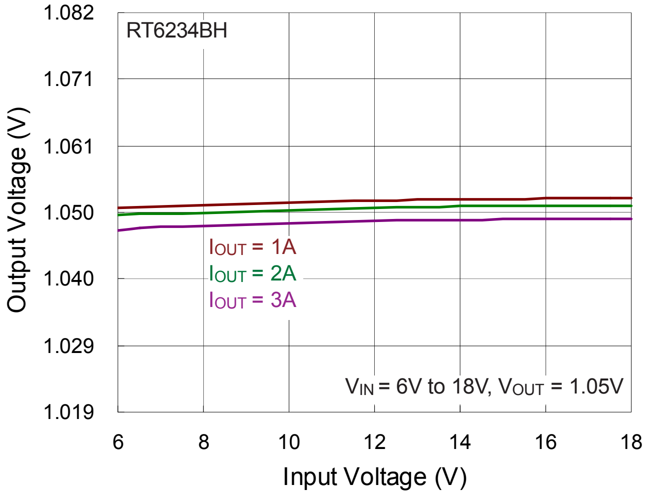
Output Voltage vs. Output Current



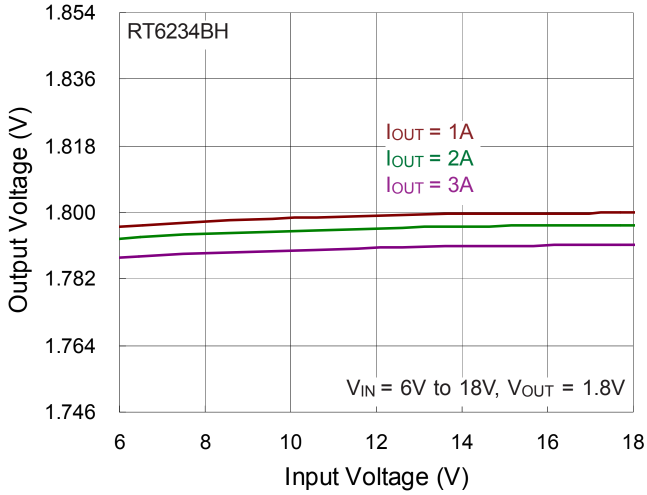
Output Voltage vs. Output Current



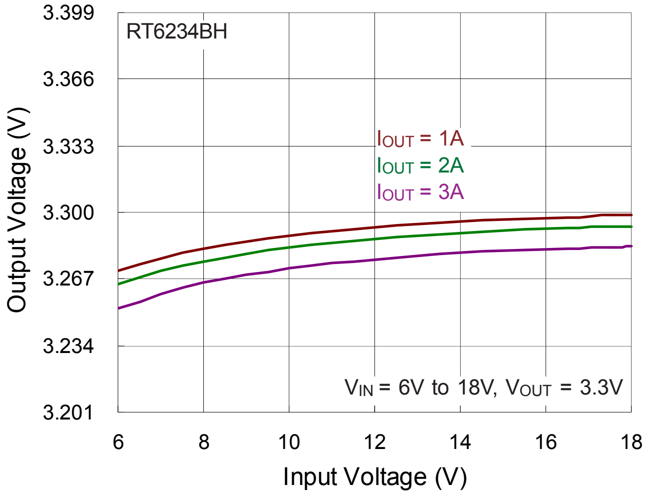
Output Voltage vs. Input Voltage



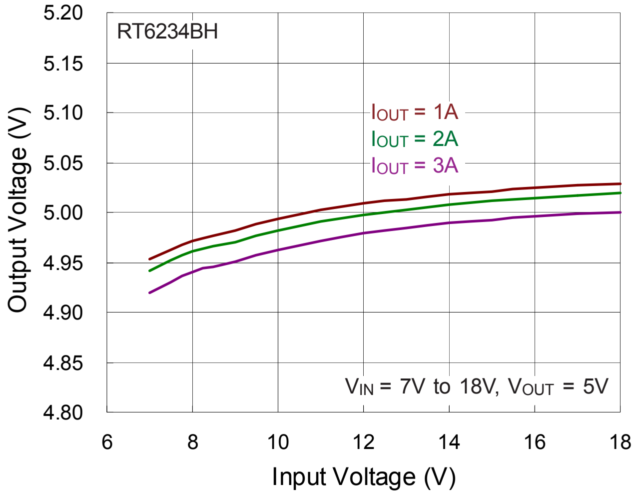
Output Voltage vs. Input Voltage



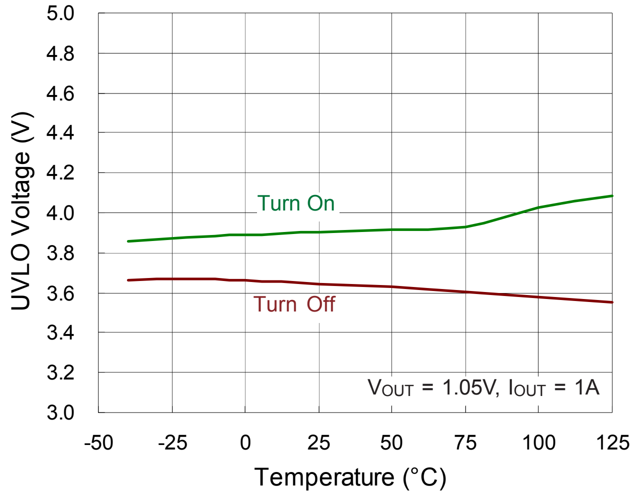
Output Voltage vs. Input Voltage



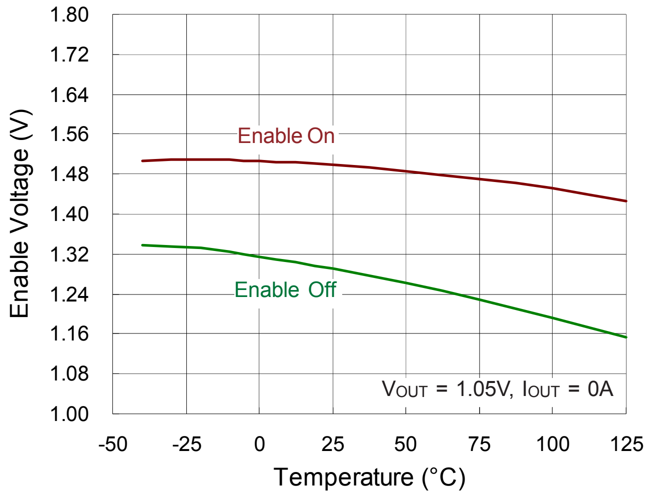
Output Voltage vs. Input Voltage



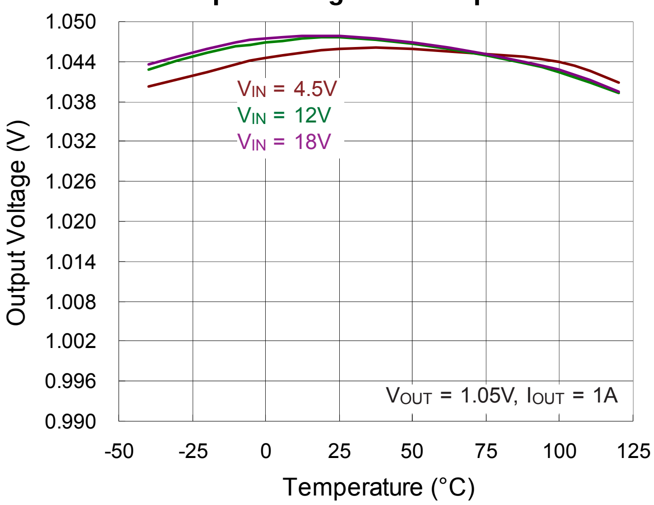
UVLO vs. Temperature



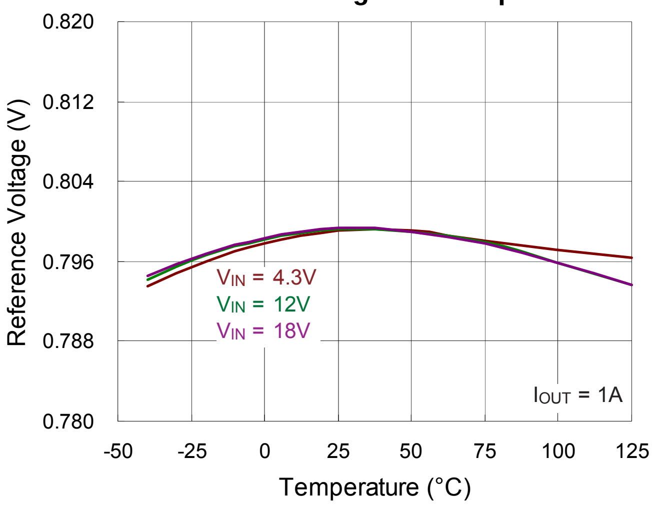
Enable Voltage vs. Temperature



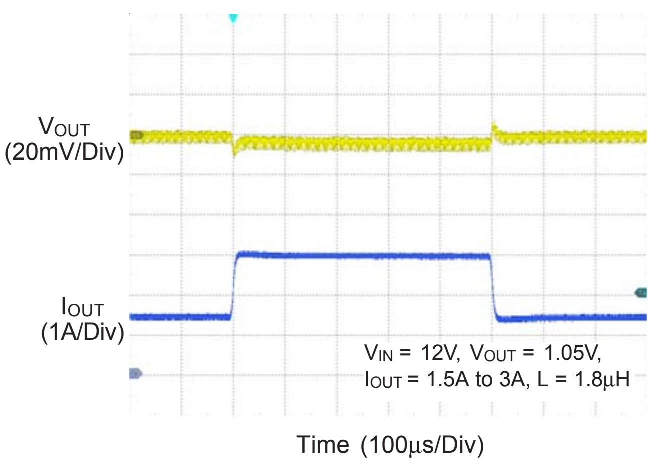
Output Voltage vs. Temperature



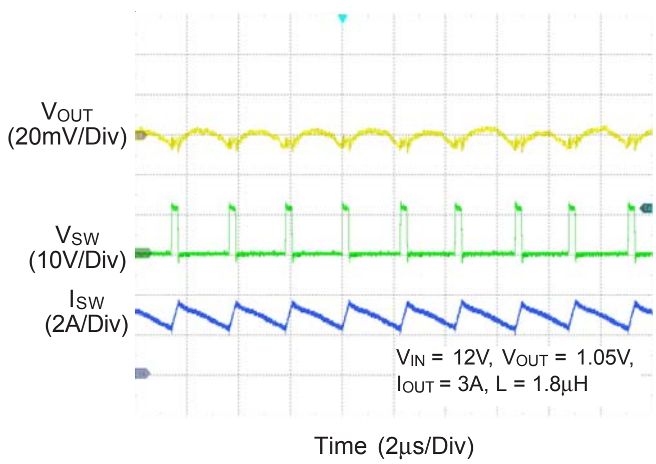
Reference Voltage vs. Temperature



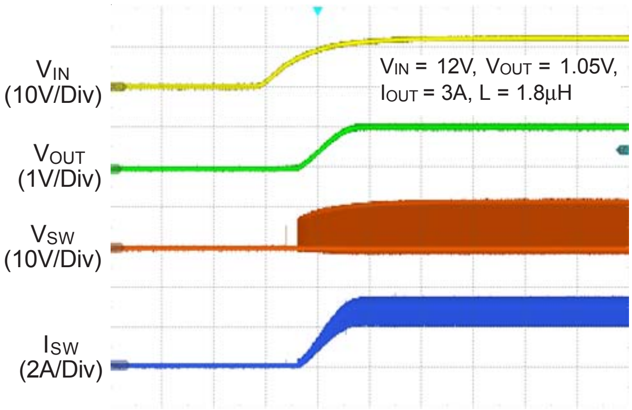
Load Transient Response



Output Ripple Voltage

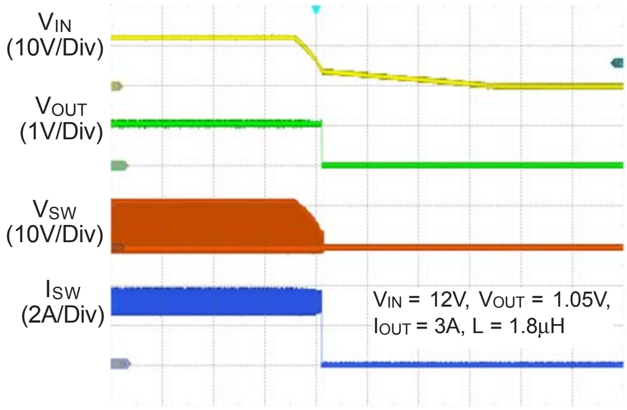


Power On from VIN



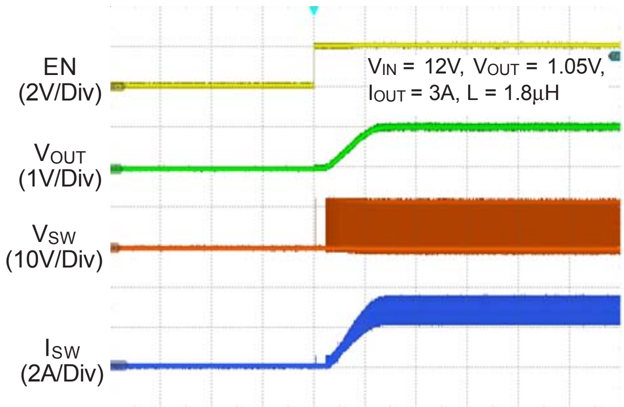
Time (4ms/Div)

Power Off from VIN



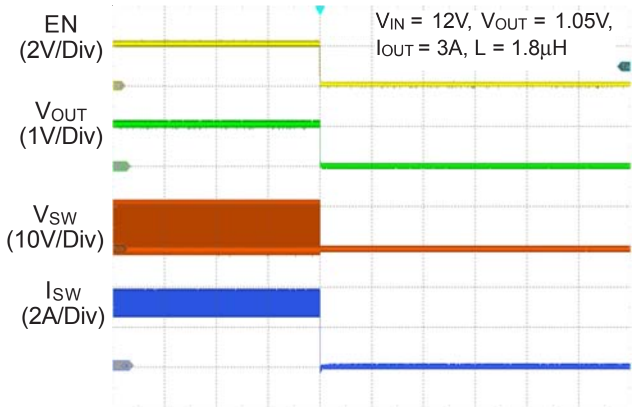
Time (10ms/Div)

Power On from EN



Time (4ms/Div)

Power Off from EN



Time (4ms/Div)

Application Information

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20% to 50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

$I_{L(PEAK)}$ should not exceed the minimum value of IC's upper current limit level or the IC may not be able to meet the desired output current. If needed, reduce the inductor ripple current (ΔI_L) to increase the average inductor current (and the output current) while ensuring that $I_{L(PEAK)}$ does not exceed the upper current limit level.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses some type of ferrite core is usually best and a shielded core type, although possibly larger or more expensive, will probably give fewer EMI and other noise problems.

Considering the Typical Operating Circuit for 1.2V output at 3A and an input voltage of 12V, using an inductor ripple of 0.9A (30%), the calculated inductance value is :

$$L = \frac{1.2 \times (12 - 1.2)}{12 \times 500\text{kHz} \times 0.9\text{A}} = 2.4\mu\text{H}$$

The ripple current was selected at 0.9A and, as long as we use the calculated 2.4μH inductance, that should be the actual ripple current amount. The ripple current and required peak current as below :

$$\Delta I_L = \frac{1.2 \times (12 - 1.2)}{12 \times 500\text{kHz} \times 2.4\mu\text{H}} = 0.9\text{A}$$

$$\text{and } I_{L(PEAK)} = 3\text{A} + \frac{0.9\text{A}}{2} = 3.45\text{A}$$

For the 2.4μH value, the inductor's saturation and thermal rating should exceed 3.45A. Since the actual value used was 2.4μH and the ripple current exactly 0.9A, the required peak current is 3.45A.

Input Capacitor Selection

The input filter capacitors are needed to smooth out the switched current drawn from the input power source and to reduce voltage ripple on the input. The actual capacitance value is less important than the RMS current rating (and voltage rating, of course). The RMS input ripple current (I_{RMS}) is a function of the input voltage, output voltage, and load current :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. However, take care when these capacitors are used at the input of circuits supplied by a wall adapter or other supply connected through long, thin wires. Current surges through the inductive wires can induce ringing at the RT6234A/B input which could potentially cause large, damaging voltage spikes at VIN. If this phenomenon is observed, some bulk input capacitance may be required. Ceramic capacitors (to meet the RMS current requirement) can be placed in parallel with other types such as tantalum, electrolytic, or polymer (to reduce ringing and overshoot).

Choose capacitors rated at higher temperatures than required. Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application. The typical operating circuit uses two 10μF and one 0.1μF low ESR ceramic capacitors on the input.

Output Capacitor Selection

The RT6234A/B are optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output Ripple

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

For the Typical Operating Circuit for 1.2V output and an inductor ripple of 0.4A, with 2 x 22μF output capacitance each with about 5mΩ ESR including PCB trace resistance, the output voltage ripple components are :

$$V_{RIPPLE(ESR)} = 0.9A \times 5m\Omega = 4.5mV$$

$$V_{RIPPLE(C)} = \frac{0.9A}{8 \times 44\mu F \times 500kHz} = 5.11mV$$

$$V_{RIPPLE} = 4.5mV + 5.11mV = 9.61mV$$

Feed-forward Capacitor (C_{ff})

The RT6234A/B are optimized for ceramic output capacitors and for low duty cycle applications. However for high-output voltages, with high feedback attenuation, the circuit's response becomes over-damped and transient response can be slowed. In high-output voltage circuits (V_{OUT} > 1.8V) transient response is improved by adding a small “feed-forward” capacitor (C_{ff}) across the upper FB divider resistor (Figure 1), to increase the circuit's Q and reduce damping to speed up the transient response without affecting the steady-state stability of the circuit. Choose a suitable capacitor value that following below step.

- Get the BW the quickest method to do transient response form no load to full load. Confirm the damping frequency. The damping frequency is BW.

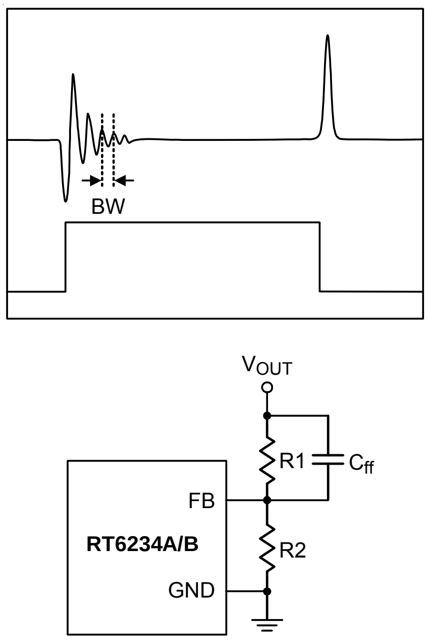


Figure 1. C_{ff} Capacitor Setting

- C_{ff} can be calculated base on below equation :

$$C_{ff} = \frac{1}{2 \times 3.1412 \times R1 \times BW \times 0.8}$$

Enable Operation (EN)

For automatic start-up the high-voltage EN pin can be connected to VIN, through a 100kΩ resistor. Its large hysteresis band makes EN useful for simple delay and timing circuits. EN can be externally pulled to VIN by adding a resistor-capacitor delay (R_{EN} and C_{EN} in Figure 2). Calculate the delay time using EN's internal threshold where switching operation begins.

An external MOSFET can be added to implement digital control of EN when no system voltage above 2V is available (Figure 3). In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input under voltage lockout threshold (Figure 4).

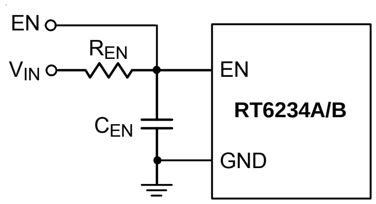


Figure 2. External Timing Control

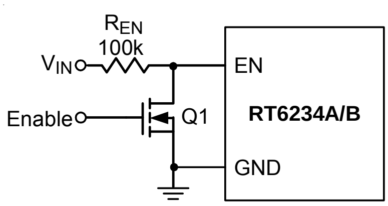


Figure 3. Digital Enable Control Circuit

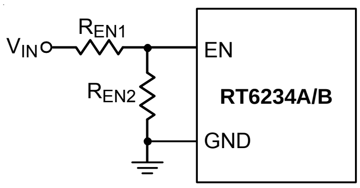


Figure 4. Resistor Divider for Lockout Threshold Setting

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

$$V_{OUT} = 0.8V \times (1 + \frac{R1}{R2})$$

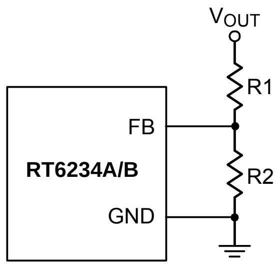


Figure 5. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

External BOOT Bootstrap Diode

When the input voltage is lower than 5.5V it is recommended to add an external bootstrap diode between VIN (or VINR) and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

External BOOT Capacitor Series Resistance

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{SW} rises rapidly. During switch turn-off, SW is discharged relatively slowly by the inductor current during the dead time between high-side and low-side switch on-times. In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<47Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and $V_{SW's}$ rise. To remove the resistor from the capacitor charging path (avoiding poor enhancement due to undercharging the BOOT capacitor), use the external diode shown in Figure 6 to charge the BOOT capacitor and place the resistance between BOOT and the capacitor/diode connection.

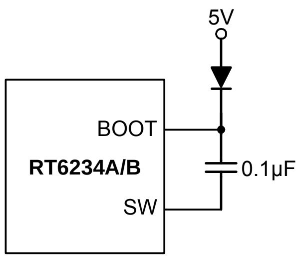


Figure 6. External Bootstrap Diode

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-8L 2x3 package, the thermal resistance, θ_{JA}, is 31.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (31.5°C/W) = 3.17W for a WDFN-8L 2x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

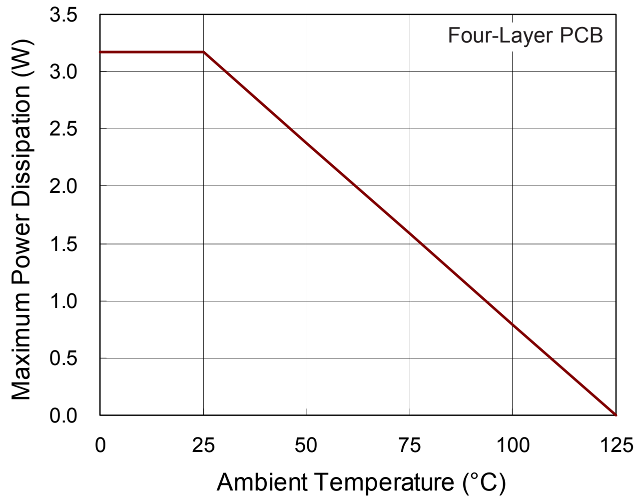


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and GND pins as possible. The major MLCC capacitors should be placed on the same layer as the RT6234A/B.
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Place the feedback components next to the FB pin.
- For better thermal performance, to design a wide and thick plane for GND pin or to add a lot of vias to GND plane.

An example of PCB layout guide is shown from Figure 8.

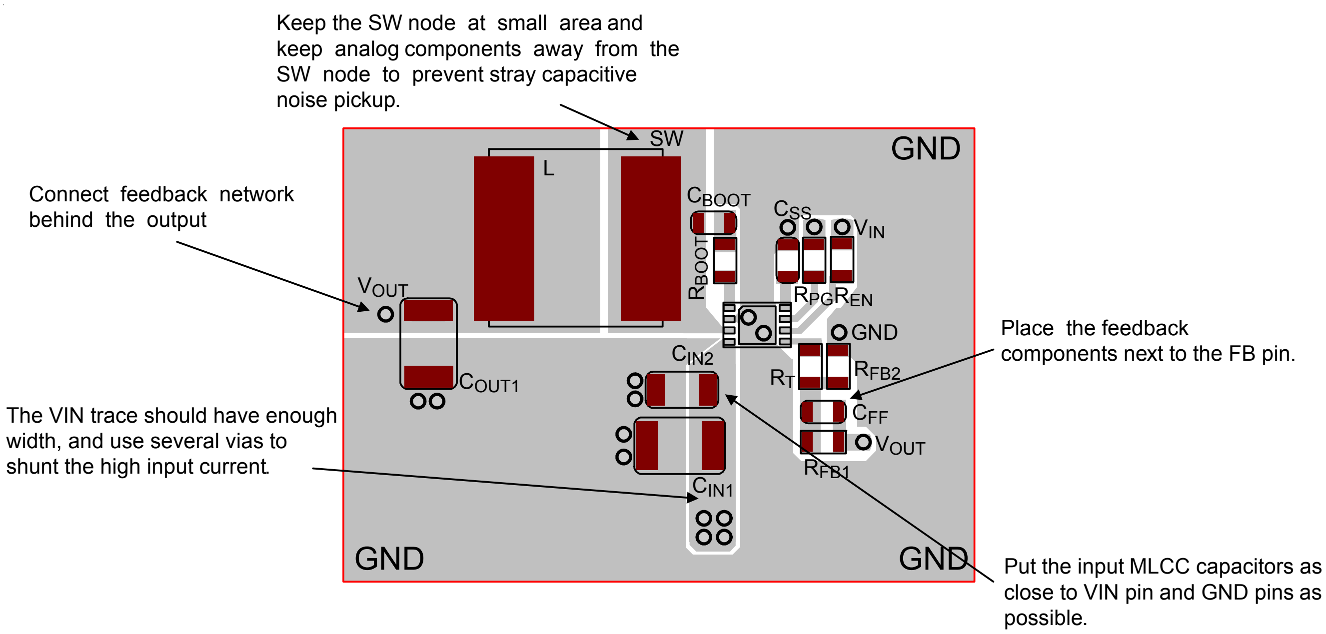
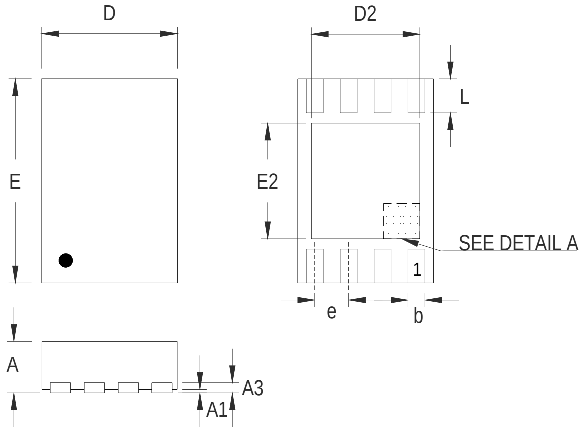
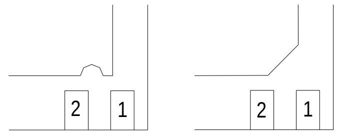


Figure 8. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.900	2.100	0.075	0.083
D2	1.550	1.650	0.061	0.065
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 8L DFN 2x3 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789