AN-1683 LMH7324 High Speed Comparator Evaluation Board

1 General Description

This board is designed to demonstrate the LMH7324 quad comparator with RSPECL outputs. It will facilitate the evaluation of the LMH7324 configured as a window detector. The board detects the level of the incoming signal and presents the outcome in a 3-bit presentation. One bit indicates that the signal is below the lowest window level, another bit indicates that the signal is above the highest window level, and the third bit indicates that the incoming signal is just between both set levels. All three outputs are fed to SMA connectors mounted at the edge of the board. The impedance of the output track is 50Ω which makes it easy to connect these signals to any scope or analyzer by the use of a 50Ω coaxial cable. Each comparator of the LMH7324 has individual positive supplies for the input and output circuits. The negative supply is common for all input and output circuitry. This setup will work with a supply of ±2.5V as a minimum supply, with the window voltage centered at ground. If a setup with only one positive supply voltage is used, jumper J1 (see Figure 7) has to be placed between both positive supply connections. To examine the possibility of two separate supplies for the input and the output stage the jumper has to be removed and an extra supply has to be connected.

2 Basic Operation

2.1 Reference Levels

The circuit is built around the four comparators of one LMH7324. Two reference levels are created using four resisters and two capacitors (R3, R6, R7, R9 and C9, C12 see Figure 7) The ‘ref high’ level is a positive voltage referred to the ground level and the ‘ref low’ level is a negative voltage referred to ground. The input connector (con2) is also referenced to ground which means that any AC signal at the input will vary around the ground level, which is in the center of the reference levels.

2.2 Comparators

The comparators B and C form the window detector, while the comparator A is a level detector indicating that the input voltage exceeds the ‘ref high’ voltage in the positive direction. The comparator D is a level detector indicating that the input signal exceeds the ‘ref low’ voltage in the negative direction. The outputs are connected to a 50Ω connector via a 50Ω track. All three outputs are ‘active low’ as can be seen in Table 1.

Table 1. Four Comparators Output

V_{IN}	$\overline{QA}$	$\overline{QB}$	$\overline{QC}$	$\overline{QD}$
High	0	1	0	1
In Window	1	0	0	1
Low	1	0	1	0

The window detector output is formed by the OR-function of combining both $\overline{Q}$ outputs of comparators B and C. Outputs which have an ECL (Emitter Coupled Logic) structure can be wired together to form an OR function. The overall truth table is shown in Table 2:

Table 2. Truth Table

V_{IN}	Con1	Con3	Con4
High	0	1	1
In Window	1	0	1
Low	1	1	0

2.3 Outputs

Every output has a Q and $\overline{Q}$ connection and both outputs have been made active by a resistor connected to the V_{EE} terminal. An ECL output becomes active when current flows out of the emitters of the output stage. This can be done by connecting a resistor to a 'termination' voltage (VT) which is 2V below the V_{CCO}. When using the VT solution every output resistor has to be 50Ω (R1, R2, R4, R5, R10, R11, R12). Another possibility is to connect a resistor to the most negative supply voltage. In case of a connection to V_{EE}, the resistor must have a value which causes a current that complies with the 'Normal Operating' conditions as mentioned in the datasheet. This demo board is designed for a supply voltage of 5V for the V_{CCO} with a resistor to V_{EE} with a value of 240Ω (R4 = 360 while R1, R2, R5, R10, R11, R12 = 240). In case the V_{CCO} is raised to 12V all output resistors to V_{EE} should be replaced with 500Ω resistors except R4 which should be 750Ω. All three output signals are connected via a 50Ω track and a combined capacitor and jumper which are connected in parallel. A customer can now make a choice between a DC or an AC coupled output signal. In the case of a DC coupled output be aware of the offset voltage which causes an extra DC current into a connected scope or analyzer with 50Ω input impedance.

2.4 Supply Voltages

This demo board can operate with a simple dual supply of ±2.5V. The output voltages are now about 1.35V and 1.0V and comply with LVDS and RSPECL levels. In the case of a single supply voltage of +5V the output levels are 3.85V and 3.5V, which is only RSPECL level compliant. In a single supply configuration be aware that the detection window starts at V_{EE} level, which is actually the ground level. The LMH7324 is ground sensing but in this configuration the input signals cannot extend more than 200 mV below the ground level. Every comparator has a separate connection for the V_{CCI}, V_{CCO} and the V_{EE}. The supply pins are decoupled with a small capacitance of 10 nF to the ground plane. Since the outputs are referenced to the V_{CCO} the output resistors are decoupled to this supply pin. For better low frequency decoupling a 47 µF capacitor is placed at the supply connector (con5). The supplies V_{CCI} and V_{CCO} can be shortened by a jumper (J1) in case both positive supply voltages are the same value.

3 Layout Considerations

The layout is done with a four layer board which makes it easy to keep the design compact with small 50Ω tracks. The advantage of this is that such tracks route easily and connect perfectly to small components. At the same time the length and number of supply lines are reduced, while decoupling to these supplies is easy and direct. Signals are routed on the top and bottom layer, making it easy to measure them.

4 Measurement Hints and Results

Measurements can be done at the output connectors by connecting a scope or analyzer to the test board. The outputs are capable of driving a 50Ω load. This board offers the possibility of making the output DC or AC coupled. When DC coupling is used be aware of the DC offset voltage present on the output signals. When working with a high supply voltage on the V_{CCO} it is possible to damage the output stage of the device or the input impedance of the equipment. To show what signals can be expected sample measurement results are shown in the following figures. Measurements were taken at different frequencies and waveforms. In the first instance measurements were taken at a frequency of 5 MHz with a sawtooth waveform. The supply voltages are +2.5V and –2.5V. This means that both thresholds are at the same level of approximately 50 mV. There are three results shown: one with the input signal crossing only the upper level (see Figure 1) and one while the input signal is only crossing the lowest level (see Figure 2). The third plot shows the waveforms when the input signal crosses the complete window from below the lowest level until above the upper level (see Figure 3).

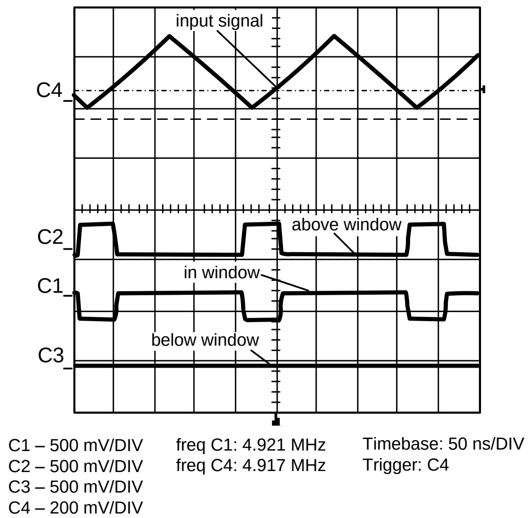


Figure 1. 5 MHz Crossing Upper Level

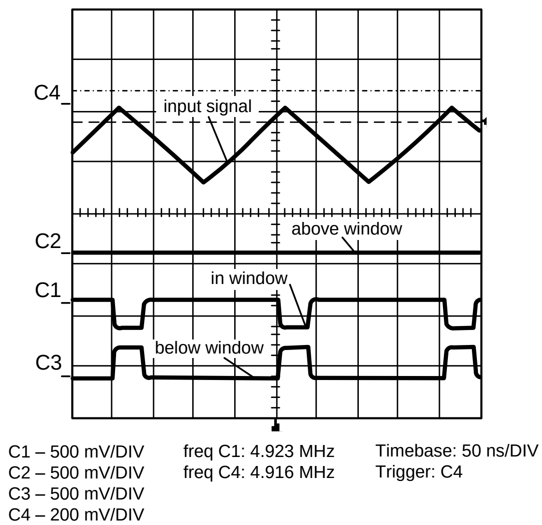


Figure 2. 5 MHz Crossing Lower Level

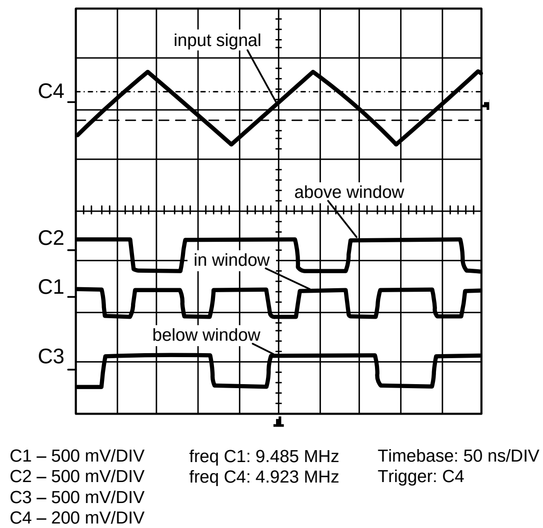


Figure 3. 5 MHz Crossing Whole Window

Higher frequencies will make the pulses much shorter, especially when a sine wave is used and the signal rises far above the window levels. This situation would make the time that the signal crosses the window levels very short, because a sine wave has the highest dV/dt at the transition points. Figure 4, Figure 5, and Figure 6 show the measurements taken when a sine wave is used. In Figure 4 a sine wave of 10 MHz is used and it just crosses both levels of the window. This creates a reasonable pulse width for both the detection signals “above window” and “below window” and for the detection signal “in window.” The added hysteresis works since no oscillations can be seen although the input signal crosses the levels very slowly and with low overdrive. When using a signal with the same frequency but with a much greater amplitude, the time it takes for the signal to cross the window becomes much shorter as can be seen in Figure 5. Note that the frequency of the detection signal “in window” doubles compared to the input frequency. Also the crossing time through the window levels is very short and, for this example, it is equal to one period of a frequency of 227 MHz (see marker indication in plot). This means that the detection signal “in window” is the most critical of the three detection signals and will be the first to incur problems due to frequency limits. The setup of Figure 6 uses an input frequency of 100 MHz with a big overdrive at the window levels. This results in a very small pulse for the detection signal “in window” which is equal to one period of a 1.05 GHz signal (see markers indication in plot). All signals are measured using a cable with a length of 1 meter connected to a four channel oscilloscope. All channels are AC coupled and terminated with 50Ω.

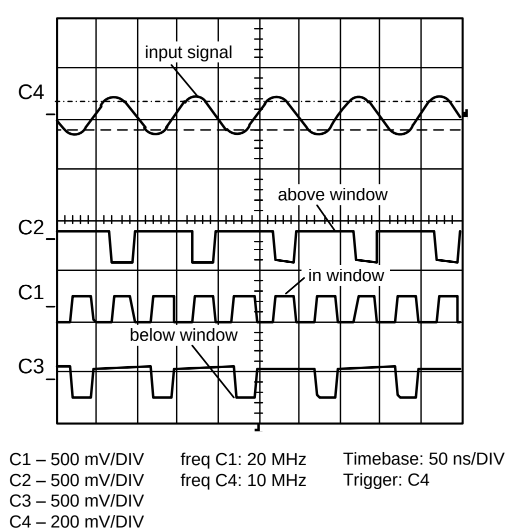
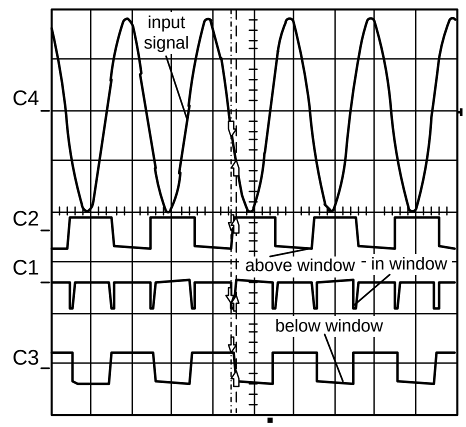


Figure 4. 10 MHz Just Above Thresholds

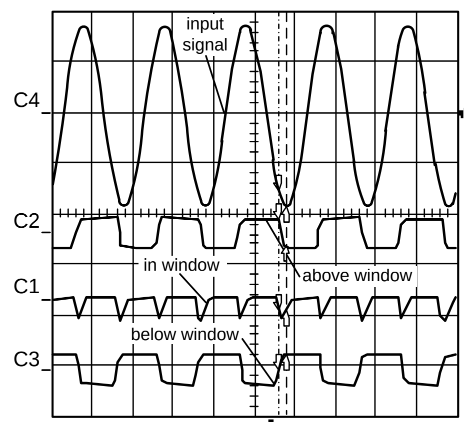


C1 – 500 mV/DIV
C2 – 500 mV/DIV
C3 – 500 mV/DIV
C4 – 200 mV/DIV

freq C1: 20 MHz
freq C4: 10 MHz
ΔT markers: 4.4 ns
1/ΔT markers: 227 MHz

Timebase: 50 ns/DIV
Trigger: C4

Figure 5. 10 MHz Far Above Thresholds



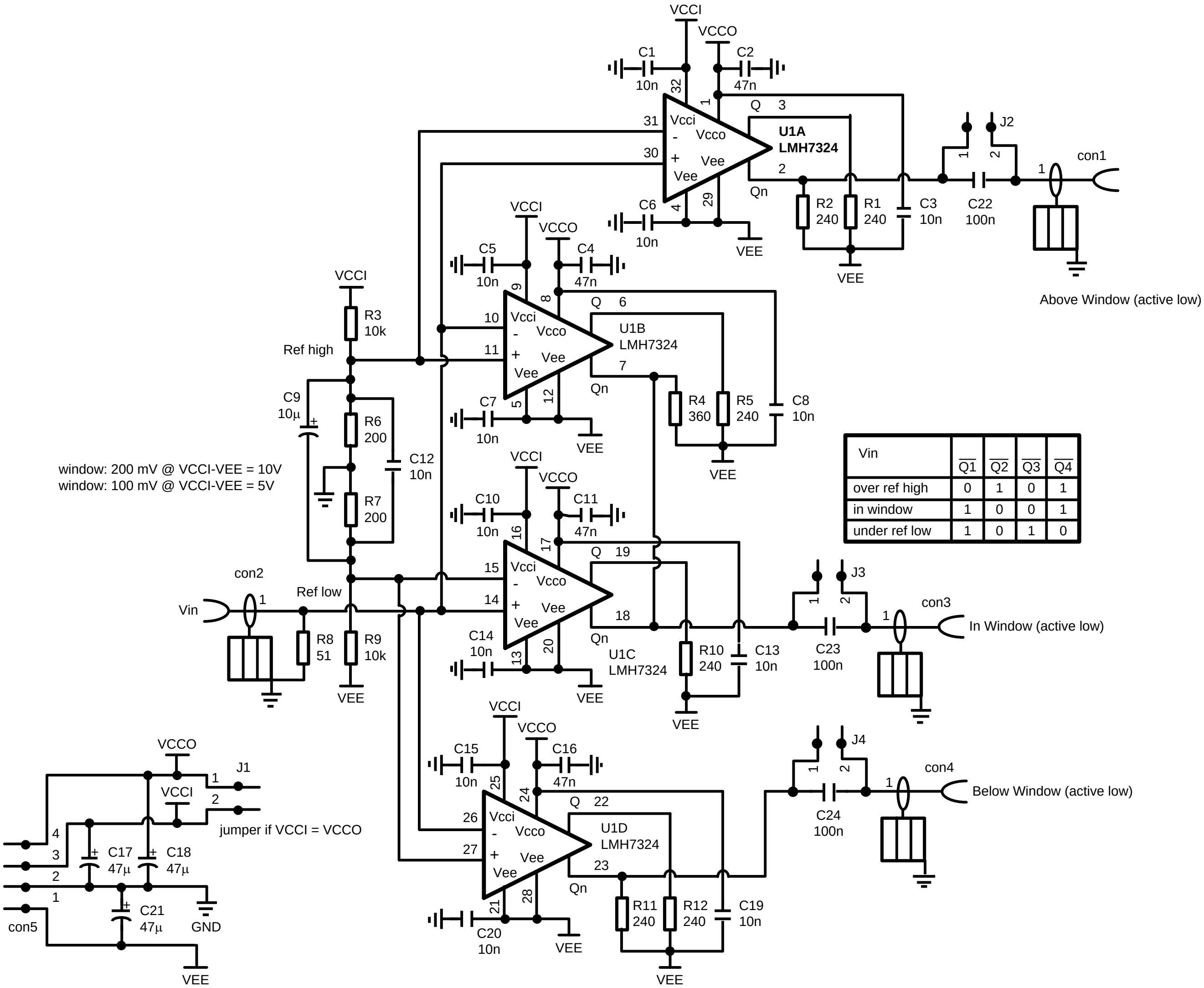
C1 – 500 mV/DIV
C2 – 500 mV/DIV
C3 – 500 mV/DIV
C4 – 200 mV/DIV

freq C1: 190.25 MHz
freq C4: 99.98 MHz
ΔT markers: 950 ps
1/ΔT markers: 1.05 GHz

Timebase: 5 ns/DIV
Trigger: C4

Figure 6. 100 MHz Far Above Thresholds

5 Board Schematic



Vin	$\overline{Q1}$	$\overline{Q2}$	$\overline{Q3}$	$\overline{Q4}$
over ref high	0	1	0	1
in window	1	0	0	1
under ref low	1	0	1	0

Figure 7. Schematic Diagram

6 Board Layout

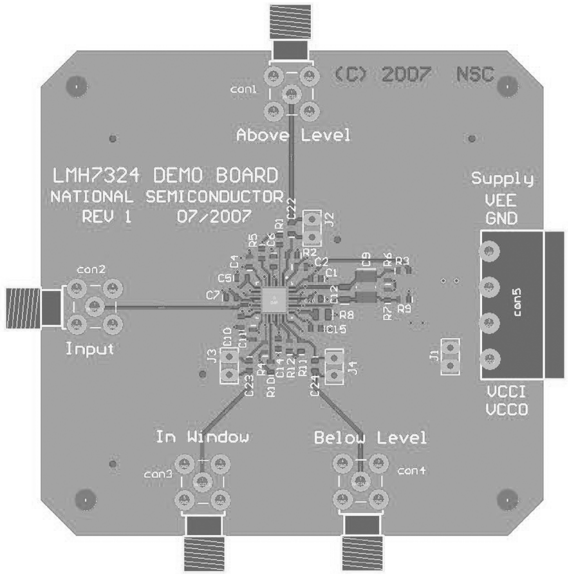


Figure 8. Top Side

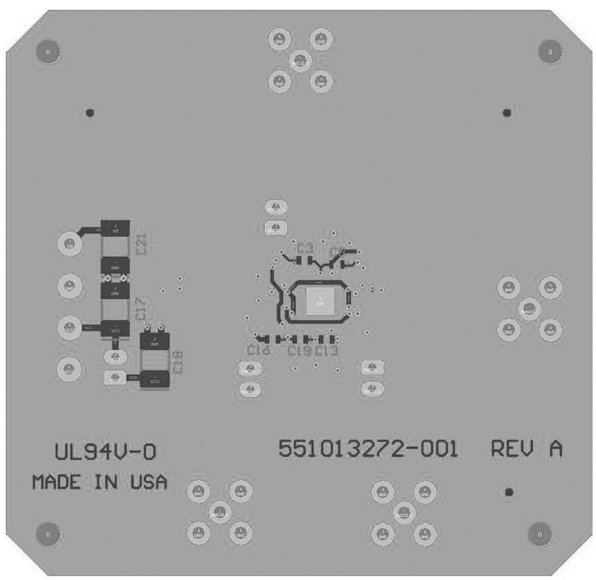


Figure 9. Bottom Side

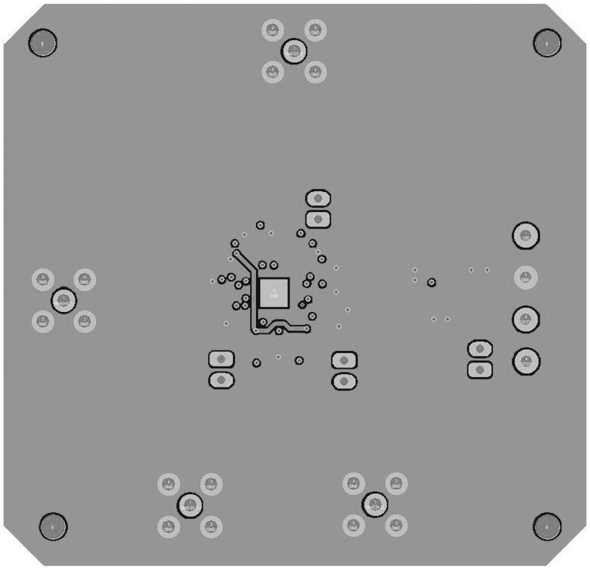


Figure 10. Mid Layer 1

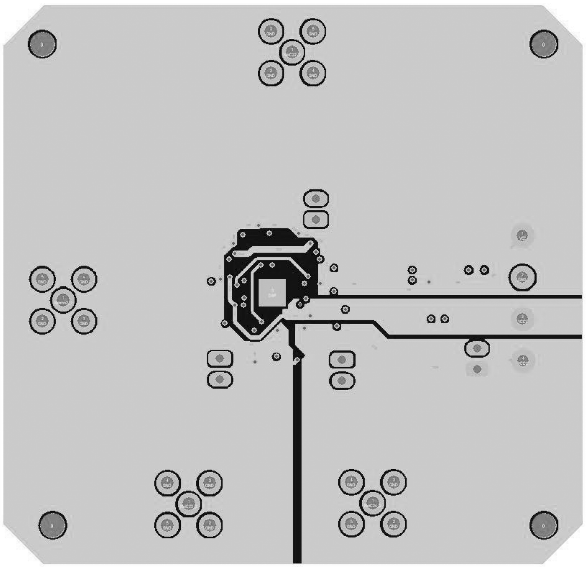


Figure 11. Mid Layer 2

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