Features

- **2.7 to 3.6V Supply**
  - **Full Read and Write Operation**
- **Low Power Dissipation**
  - **8 mA Active Current**
  - **50 µA CMOS Standby Current**
- **Read Access Time - 250 ns**
- **Byte Write - 3 ms**
- **Direct Microprocessor Control**
  - **$\overline{\text{DATA}}$ Polling**
  - **READ/$\overline{\text{BUSY}}$ Open Drain Output on TSOP**
- **High Reliability CMOS Technology**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 10 Years**
- **Low Voltage CMOS Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Commercial and Industrial Temperature Ranges**

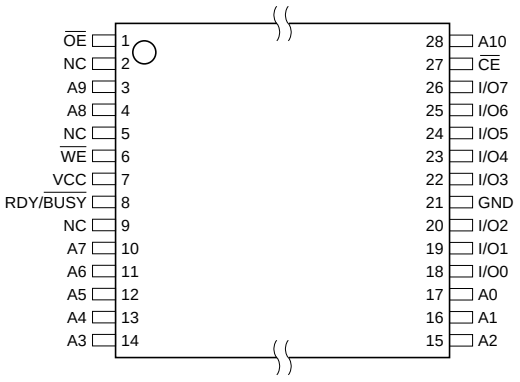
Description

The AT28BV16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28BV16 is a 16K memory organized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology. *(continued)*

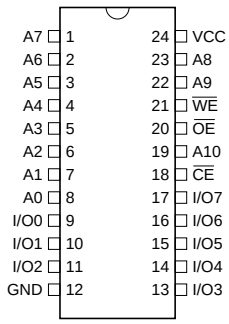
Pin Configurations

Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{Busy}}$ Output
NC	No Connect
DC	Don't Connect

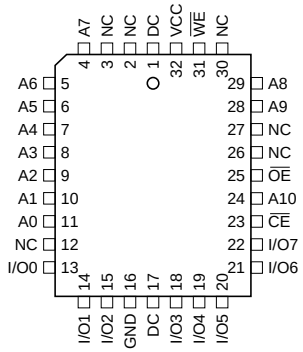
TSOP
Top View



PDIP, SOIC
Top View



PLCC
Top View



16K (2K x 8) *Battery-Voltage*™ Parallel EEPROMs

AT28BV16

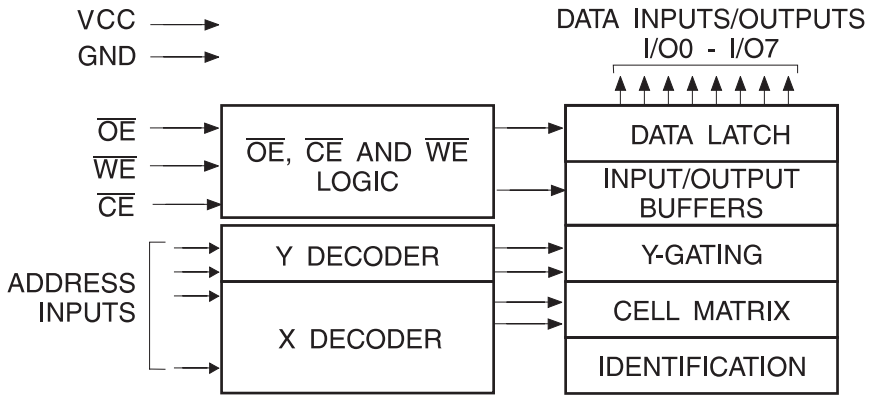
Rev. 0380B–10/98

The AT28BV16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{DATA}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 250 ns at low power dissipation. When the chip is deselected the standby current is less than 50 µA.

Atmel's 28BV16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes of EEPROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28BV16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28BV16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

$\overline{\text{DATA}}$ POLLING: The AT28BV16 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

READY/$\overline{\text{BUSY}}$ (TSOP only): READY/$\overline{BUSY}$ is an open drain output; it is pulled low during the internal write cycle and released at the completion of the write cycle.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 2.0V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 2.0V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) Write Inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

DEVICE IDENTIFICATION: An extra 32-bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		AT28BV16-25	AT28BV16-30
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

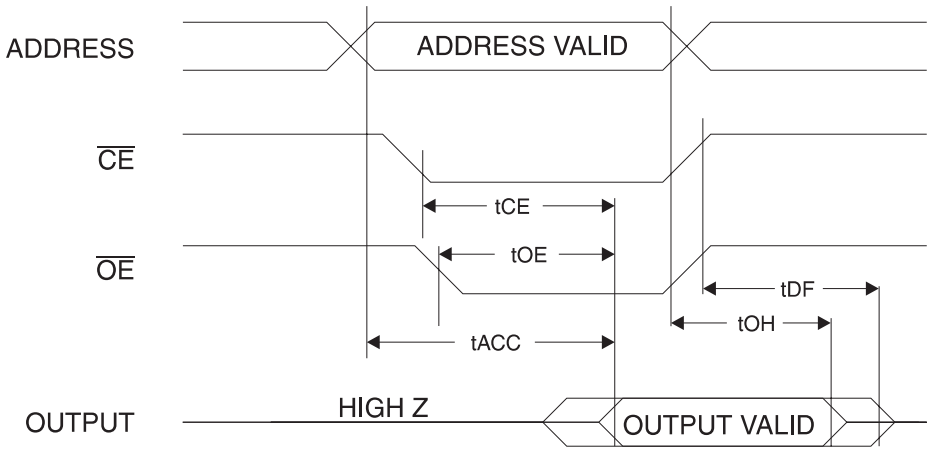
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1.0V		5	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		5	µA
I_{SB}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V		50	µA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA; CE = V_{IL}		8	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.3	V
		I_{OL} = 2 mA for RDY/$\overline{BUSY}$		0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	2.0		V

AC Read Characteristics

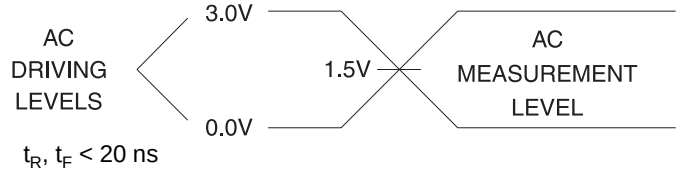
Symbol	Parameter	AT28BV16-25		AT28BV16-30		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		250		300	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		250		300	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay		100		100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms[1][2][3][4]



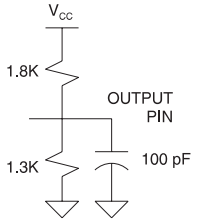
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

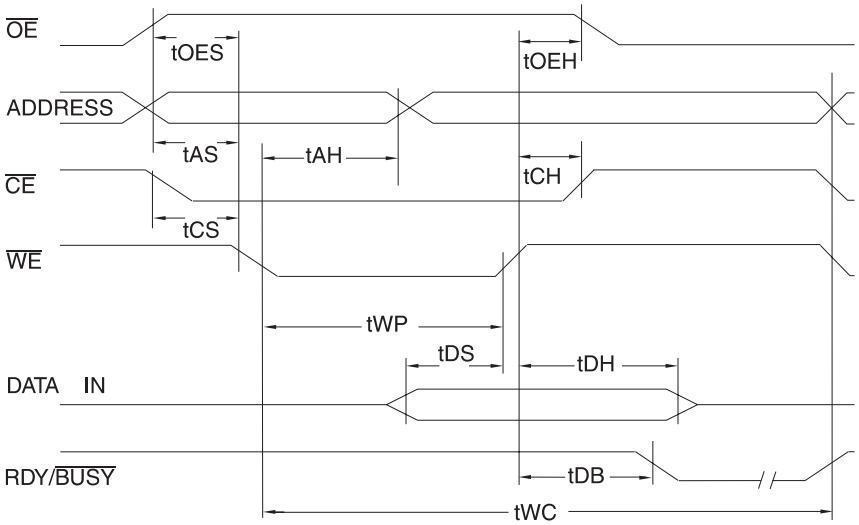
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

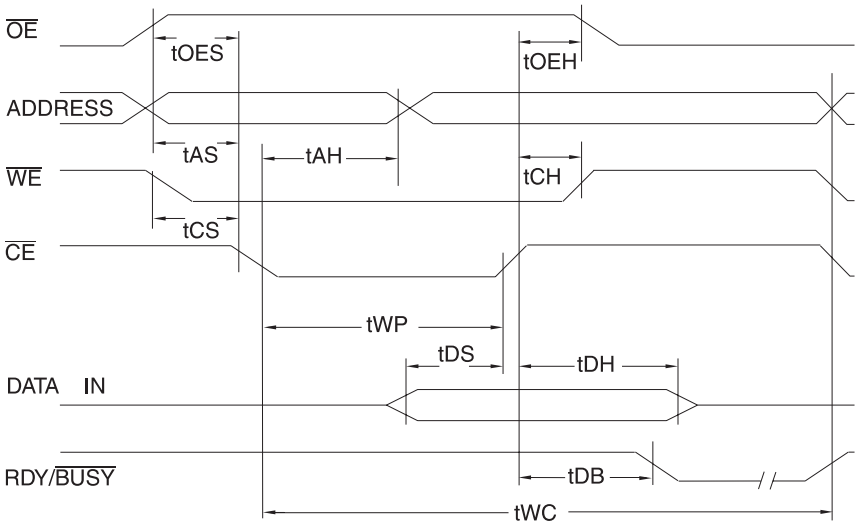
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150	1000	ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time	0		ns
t_{WC}	Write Cycle Time		3.0	ms
t_{DB}	Time to Device Busy		50	ns

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

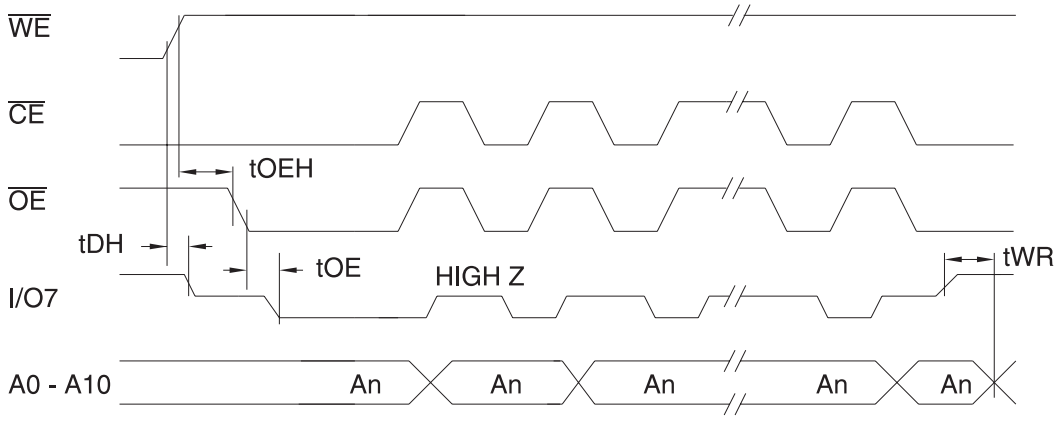


$\overline{\text{Data}}$ Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Characteristics.

$\overline{\text{Data}}$ Polling Waveforms



Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	8	0.05	AT28BV16-25TC AT28BV16-25JC AT28BV16-25PC AT28BV16-25SC	28T 32J 24P6 24S	Commercial (0°C to 70°C)
	8	0.05	AT28BV16-25TI AT28BV16-25JI AT28BV16-25PI AT28BV16-25SI	28T 32J 24P6 24S	Industrial (-40°C to 85°C)
300	8	0.05	AT28BV16-30TC AT28BV16-30JC AT28BV16-30PC AT28BV16-30SC	28T 32J 24P6 24S	Commercial (0°C to 70°C)
	8	0.05	AT28BV16-30TI AT28BV16-30JI AT28BV16-30PI AT28BV16-30SI	28T 32J 24P6 24S	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28BV16	25	JC, JI, PC, PI, SC, SI, TC, TI
AT28BV16	30	JC, JI, PC, PI, SC, SI, TC, TI

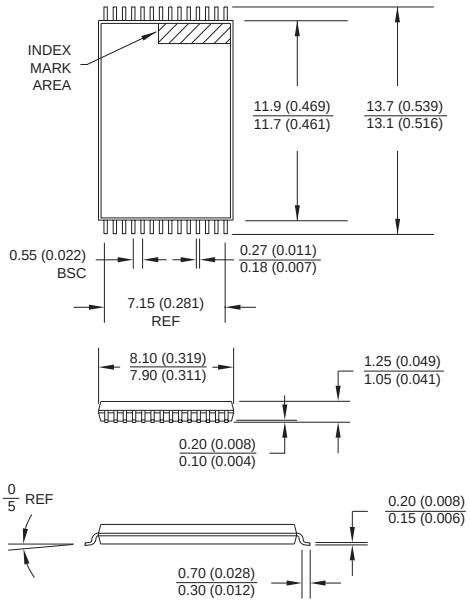
Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P6	24-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

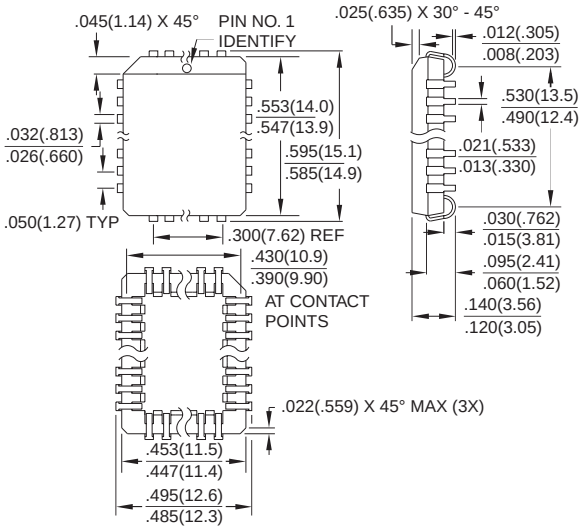
Packaging Information

28T, 28-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*

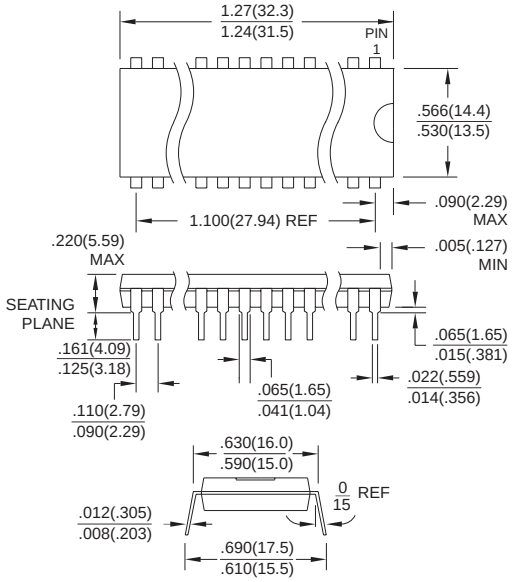


*Controlling dimension: millimeters

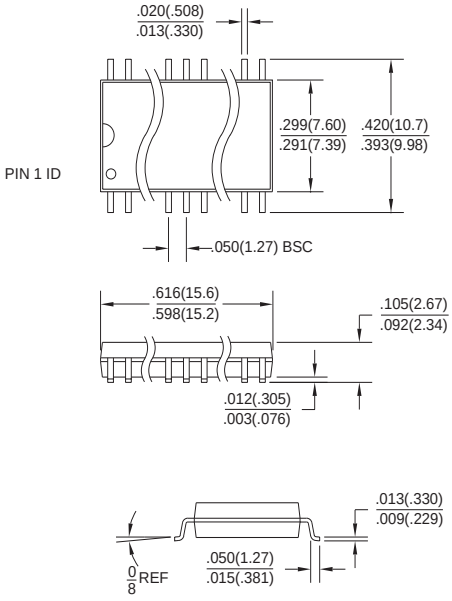
32J, 32-Lead, Plastic J-Leaded Chip Carier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE



24P6, 24-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AA



24S, 24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



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