

Top View

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Vishay Siliconix

## Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	100
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0034
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0040
I <sub>D</sub> (A)	135
Configuration	Single
Package	PowerPAK 8 x 8L

# PowerPAK® 8 x 8L Single Only Only

**Bottom View** 

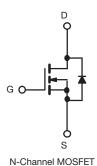
#### **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>q</sub> and UIS tested
- Fully lead (Pb)-free device
- Thin 1.9 mm height
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>





ROHS COMPLIANT HALOGEN FREE



ABSOLUTE MAXIMUM RATING	S (T <sub>C</sub> = 25 °C, unless	s otherwise noted	)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V <sub>DS</sub>	100	V
Gate-Source Voltage		$V_{GS}$	± 20	V
Continuous Drain Current	T <sub>C</sub> = 25 °C	1	135	
Continuous Drain Current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	78	
Continuous Source Current (Diode Conduc	tion)	I <sub>S</sub>	124	Α
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	210	
Single Pulse Avalanche Current  L = 0.1 mH		I <sub>AS</sub>	68	
Single Pulse Avalanche Energy	L = 0.1 IIII	E <sub>AS</sub>	231	mJ
Maximum Dawar Dissination	T <sub>C</sub> = 25 °C	D	136	W
Maximum Power Dissipation	T <sub>C</sub> = 125 °C	$P_{D}$	45	VV
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering Recommendations (Peak Temperature) c, d			260	C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount b	$R_{thJA}$	50	°C/W
Junction-to-Case (Drain)		R <sub>thJC</sub>	1.1	G/VV

#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. When mounted on 1" square PCB (FR4 material).
- c. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0$ , $I_D = 250 \mu A$		100	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	2	2.5	1 °
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 100 V	-	-	1	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0 V$	$V_{DS} = 100 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$	ı	-	50	μΑ
		$V_{GS} = 0 V$	V <sub>DS</sub> = 100 V, T <sub>J</sub> = 175 °C	1	-	500	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	50	-	-	Α
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	ı	0.0028	0.0034	
Drain-Source On-State Resistance a	D	$V_{GS} = 4.5 \text{ V}$	I <sub>D</sub> = 10 A	1	0.0033	0.0040	Ω
Dialii-Source Oil-State nesistance "	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	ı	-	0.0058	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0074	1
Forward Transconductance b	9fs	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		-	84	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			-	5620	7350	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	2850	3750	рF
Reverse Transfer Capacitance	C <sub>rss</sub>			-	220	290	1
Total Gate Charge <sup>c</sup>	Qg			-	97	150	
Gate-Source Charge c	$Q_{gs}$	V <sub>GS</sub> = 10 V	$V_{DS} = 50 \text{ V}, I_{D} = 10 \text{ A}$	-	15	-	nC
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	20	-	
Gate Resistance	$R_g$	f = 1 MHz		0.95	1.92	3	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	19	30	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_1 = 5 \Omega$		-	40	60	7
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A},$	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	69	110	ns
Fall Time <sup>c</sup>	t <sub>f</sub>	1		-	87	135	
Source-Drain Diode Ratings and Cha	racteristics b						
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	210	Α
		I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V			<b></b>		V

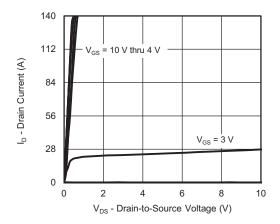
#### Notes

- a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

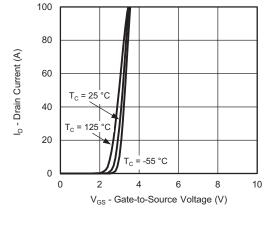
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



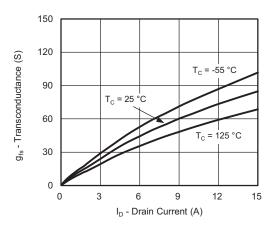
#### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



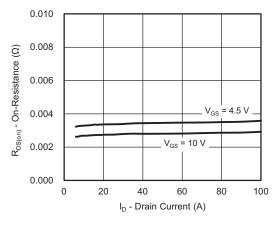
#### **Output Characteristics**



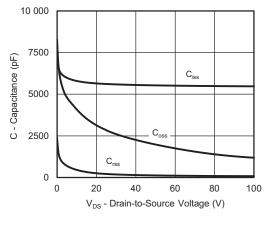
**Transfer Characteristics** 



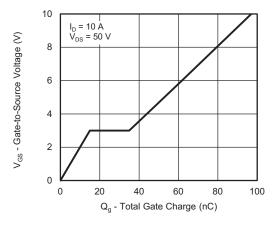
Transconductance



On-Resistance vs. Drain Current



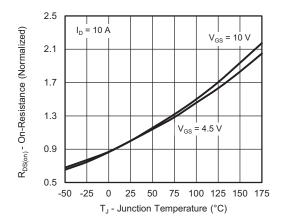




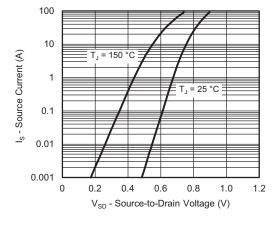
**Gate Charge** 



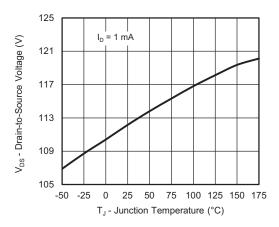
#### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



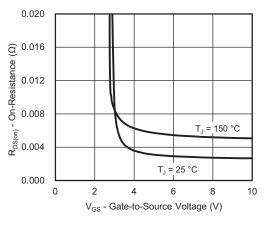
On-Resistance vs. Junction Temperature



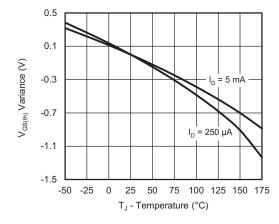
**Source Drain Diode Forward Voltage** 



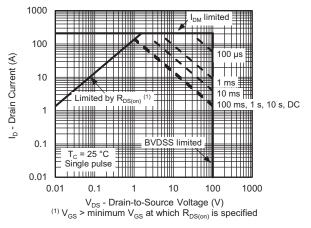
Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



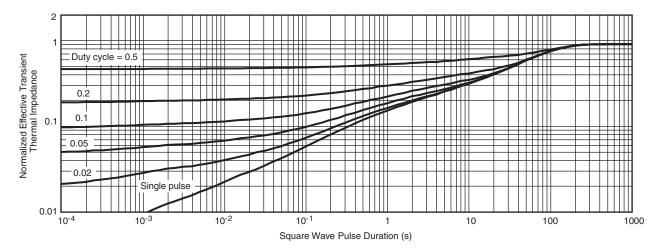
**Threshold Voltage** 



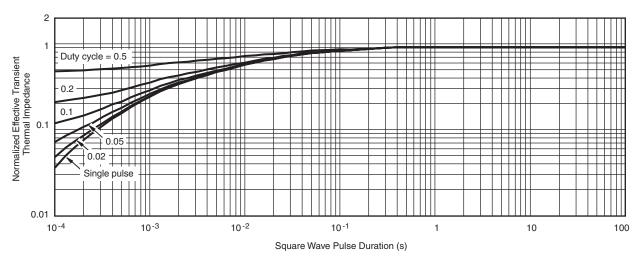
Safe Operating Area



#### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Ambient

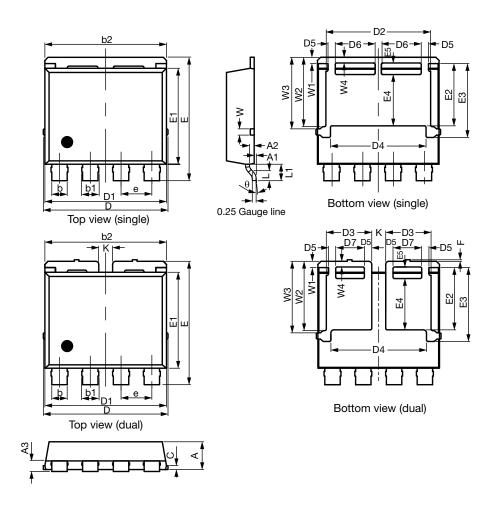


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?76643">www.vishay.com/ppg?76643</a>.



# PowerPAK® 8 x 8L Case Outline



DIM		MILLIMETERS		INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	1.70	1.80	1.90	0.067	0.071	0.075	
A1	0.00	0.08	0.13	0.000	0.003	0.005	
A2	0.25	0.30	0.35	0.010	0.012	0.014	
A3	0.55	0.62	0.70	0.022	0.024	0.028	
b	0.92	1.00	1.08	0.036	0.039	0.043	
b1	1.02	1.10	1.18	0.040	0.043	0.046	
b2	7.80	7.90	8.00	0.307	0.311	0.315	
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	8.00	8.10	8.25	0.315	0.319	0.325	
D1	7.80	7.90	8.00	0.307	0.311	0.315	
D2	6.70	6.80	6.90	0.264	0.268	0.272	
D3	2.85	2.95	3.05	0.112	0.116	0.120	
D4	6.11	6.21	6.31	0.241	0.244	0.248	
D5	0.37	0.47	0.57	0.015	0.019	0.022	
D6	2.49	2.59	2.69	0.098	0.102	0.106	
D7	1.76	1.86	1.96	0.069	0.073	0.077	

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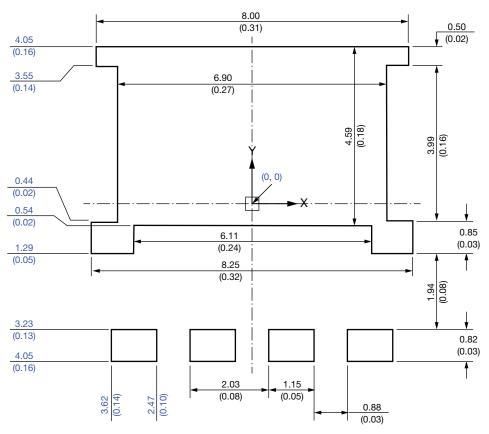
D.13.4	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	IN. NOM.		
е	1.95	2.00	2.05	0.077	0.079	0.081	
E	7.90	8.00	8.10	0.311	0.315	0.319	
E1	6.12	6.22	6.32	0.241	0.245	0.249	
E2	3.94	4.04	4.14	0.140	0.159	0.163	
E3	4.69	4.79	4.89	0.185	0.189	0.193	
E4	3.23	3.33	3.43	0.127	0.131	0.135	
E5	0.65	0.75	0.85	0.026	0.030	0.033	
F	0.00	0.10	0.15	0.000	0.004	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K	0.80	0.90	1.00	0.031	0.035	0.039	
W	0.30	0.40	0.50	0.012	0.016	0.020	
W1	0.30	0.40	0.50	0.012	0.016	0.020	
W2	4.39	4.49	4.59	0.173	0.177	0.181	
W3	4.54	4.64	4.74	0.179	0.183	0.187	
W4	0.32	0.37	0.42	0.013	0.015	0.017	
θ	6°	10°	14°	6°	10°	14°	

C17-1388-Rev. B, 16-Oct-17

DWG: 6026



# Recommended Minimum PADs for PowerPAK® 8 x 8L Single



#### Dimensions in millimeters (inches)

#### Note

• Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



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