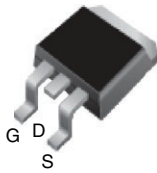


## Power MOSFET

**D<sup>2</sup>PAK (TO-263)**


N-Channel MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	200
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 5\text{ V}$   0.40
$Q_g$ max. (nC)	40
$Q_{gs}$ (nC)	5.5
$Q_{gd}$ (nC)	24
Configuration	Single

### FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic  $dv/dt$  rating
- Repetitive avalanche rated
- Logic-level gate drive
- $R_{DS(on)}$  specified at  $V_{GS} = 4\text{ V}$  and  $5\text{ V}$
- $150\text{ }^\circ\text{C}$  operating temperature
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK (TO-263) is a surface-mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D<sup>2</sup>PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

ORDERING INFORMATION			
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHL630S-GE3	SiHL630STRR-GE3 <sup>a</sup>	SiHL630STRL-GE3 <sup>a</sup>
Lead (Pb)-free	IRL630SPbF	IRL630STRRPbF <sup>a</sup>	IRL630STRLPbF <sup>a</sup>

### Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	200	V
Gate-source Voltage	$V_{GS}$	$\pm 10$	
Continuous drain current	$V_{GS}$ at 5 V	$T_C = 25\text{ }^\circ\text{C}$	9.0
		$T_C = 100\text{ }^\circ\text{C}$	5.7
Pulsed drain current <sup>a</sup>	$I_{DM}$	36	A
Linear derating factor		0.59	
Linear derating factor (PCB mount) <sup>e</sup>		0.025	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	250	mJ
Avalanche current <sup>a</sup>	$I_{AR}$	9.0	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	7.4	mJ
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$	74	W
Maximum power dissipation (PCB mount) <sup>e</sup>			
Peak diode recovery $dv/dt$ <sup>c</sup>	$dv/dt$	5.0	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	

### Notes

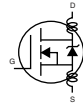

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 4.6\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 9.0\text{ A}$  (see fig. 12)
- $I_{SD} \leq 9.0\text{ A}$ ,  $di/dt \leq 120\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	200	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.27	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	-	2.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 10\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}, I_D = 5.4\text{ A}^b$	-	-	0.40	$\Omega$
		$V_{GS} = 4.0\text{ V}, I_D = 4.5\text{ A}^b$	-	-	0.50	
Forward transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 5.4\text{ A}^b$	4.8	-	-	S
<b>Dynamic</b>						
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	1100	-	pF
Output capacitance	$C_{oss}$		-	220	-	
Reverse transfer capacitance	$C_{rss}$		-	70	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 9.0\text{ A}, V_{DS} = 160\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	40	nC
Gate-source charge	$Q_{gs}$		-	-	5.5	
Gate-drain charge	$Q_{gd}$		-	-	24	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 100\text{ V}, I_D = 9.0\text{ A}, R_g = 6.0\text{ }\Omega, R_D = 11\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	8.0	-	ns
Rise time	$t_r$		-	57	-	
Turn-off delay time	$t_{d(off)}$		-	38	-	
Fall time	$t_f$		-	33	-	
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	$L_S$		-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	9.0	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$		-	-	36	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 9.0\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	2.0	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 9.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	230	350	ns
Body diode reverse recovery charge	$Q_{rr}$		-	1.7	2.6	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

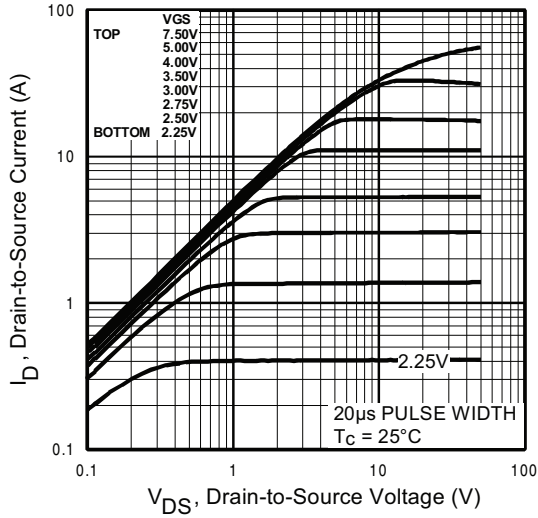


Fig. 1 - Typical Output Characteristics,  $T_c = 25^\circ\text{C}$

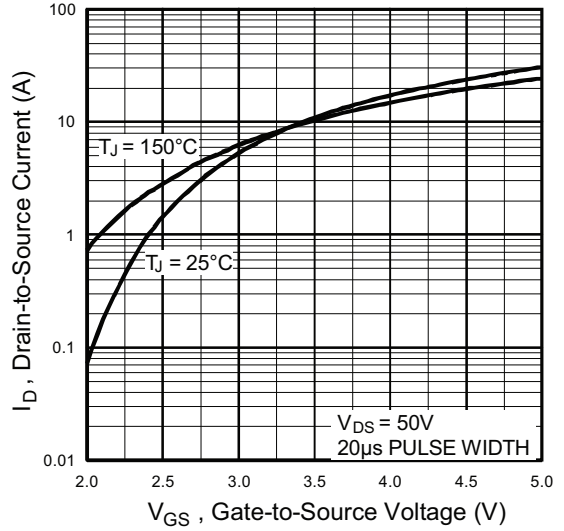


Fig. 3 - Typical Transfer Characteristics

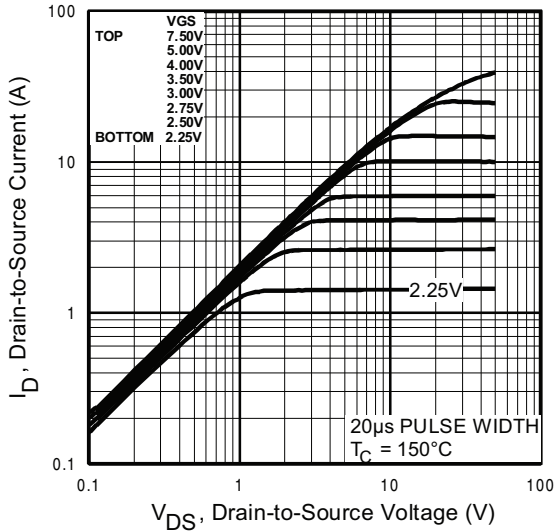


Fig. 2 - Typical Output Characteristics,  $T_c = 150^\circ\text{C}$

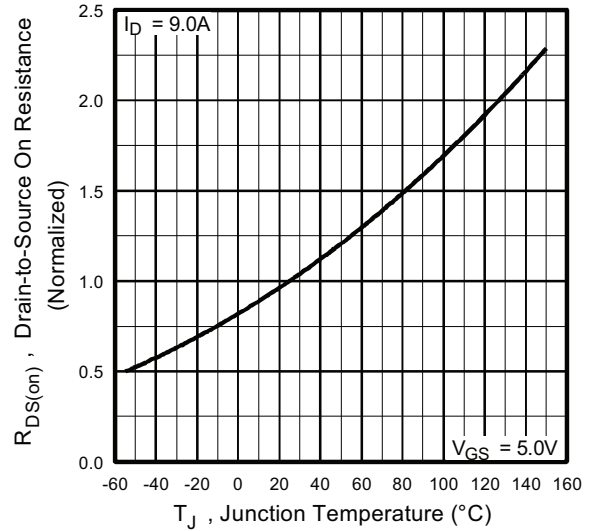


Fig. 4 - Normalized On-Resistance vs. Temperature

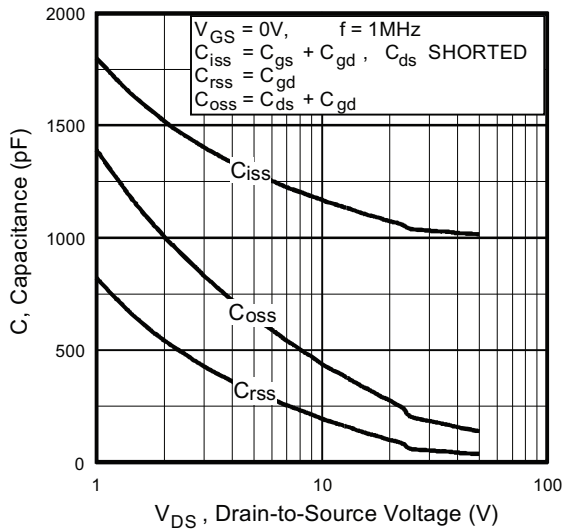


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

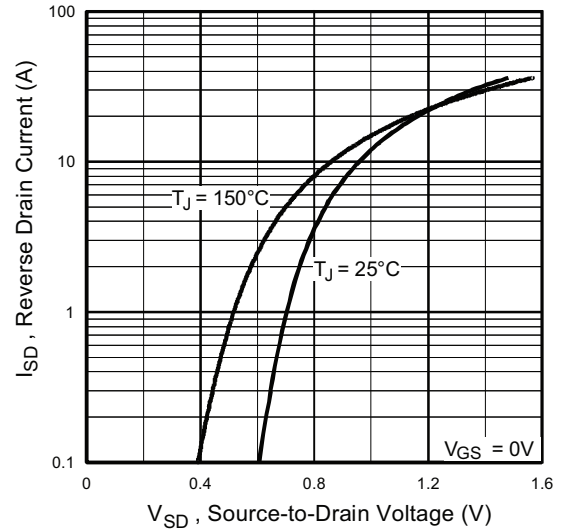


Fig. 7 - Typical Source-Drain Diode Forward Voltage

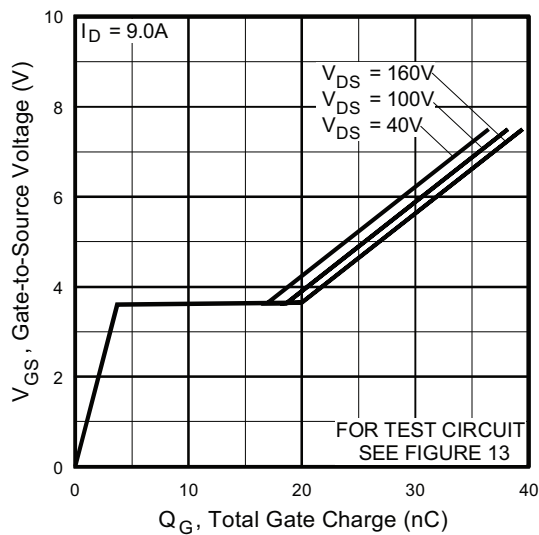


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

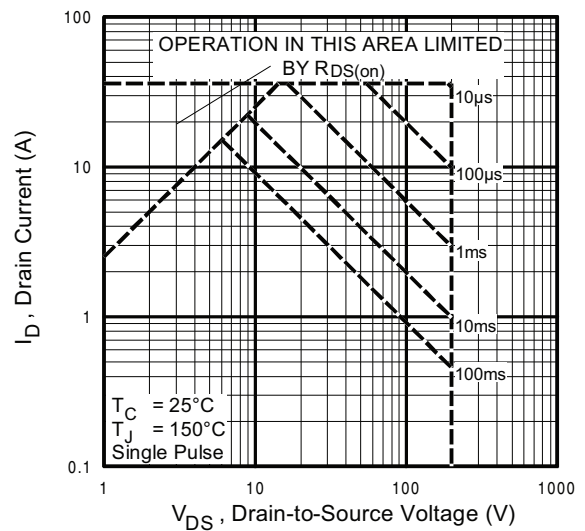


Fig. 8 - Maximum Safe Operating Area

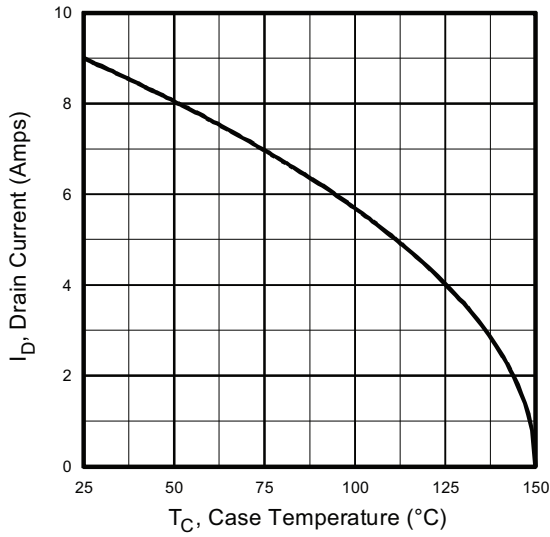


Fig. 9 - Maximum Drain Current vs. Case Temperature

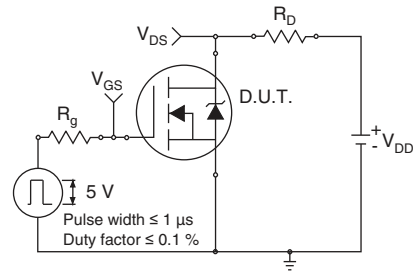


Fig. 10a - Switching Time Test Circuit

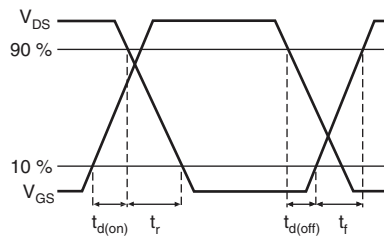


Fig. 10b - Switching Time Waveforms

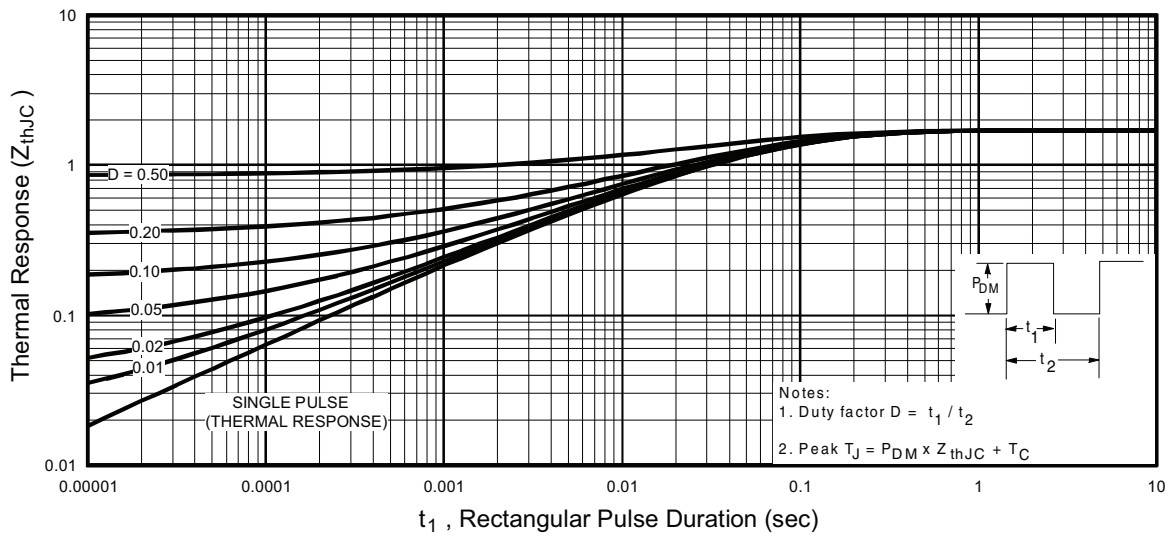
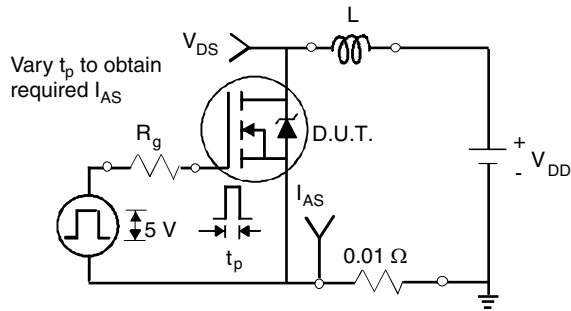
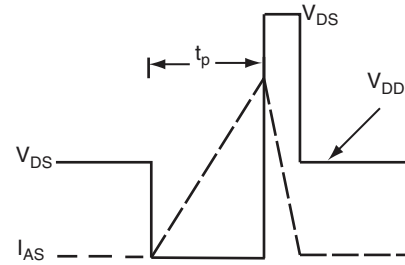
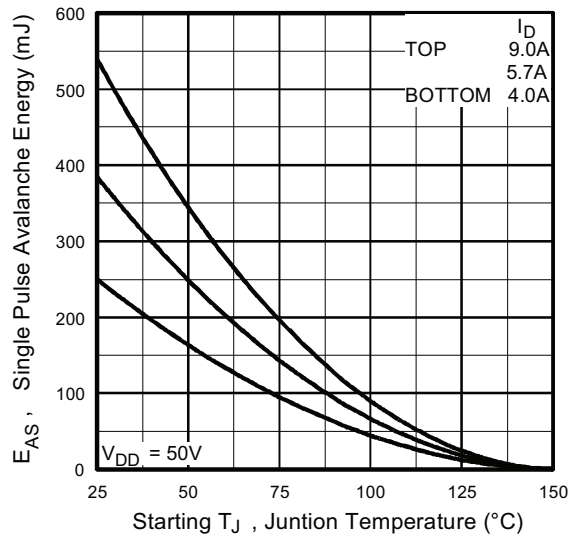
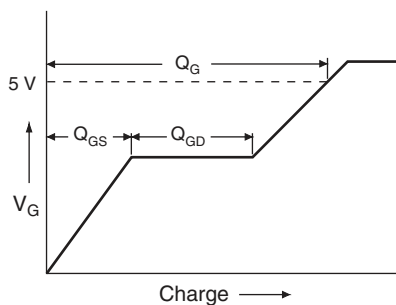
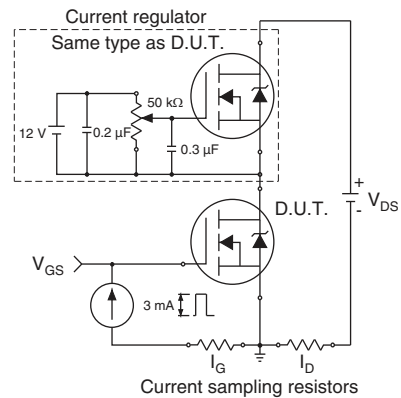
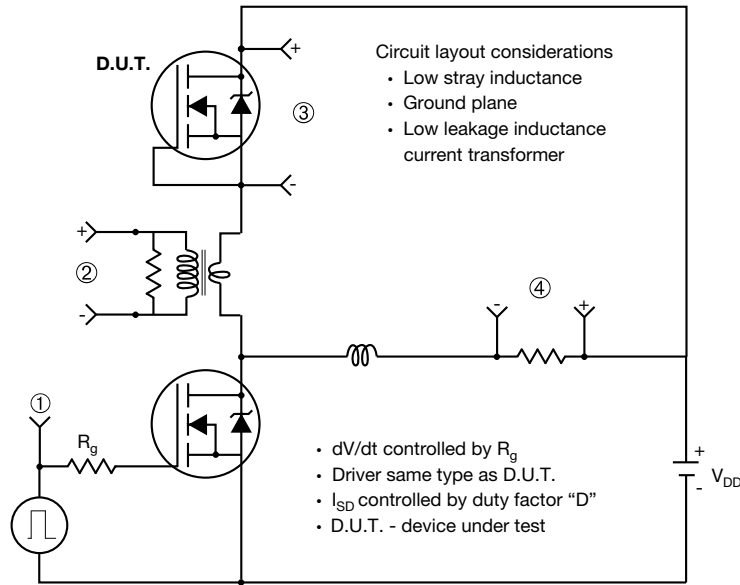


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

**Fig. 13a - Basic Gate Charge Waveform**

**Fig. 13b - Gate Charge Test Circuit**

Peak Diode Recovery dV/dt Test Circuit



**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?90390](http://www.vishay.com/ppg?90390).

### TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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