

## Power MOSFET

**D<sup>2</sup>PAK (TO-263)**


N-Channel MOSFET



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available

### FEATURES

- Advanced process technology
- Dynamic dV/dt
- 175 °C operating temperature
- Fast switching
- Fully avalanche rated
- Drop in replacement of the IRFZ48, SiHFZ48 for linear / audio applications
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### DESCRIPTION

Advanced power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>PAK is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D<sup>2</sup>PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2 W in a typical surface mount application.

### PRODUCT SUMMARY

V <sub>DS</sub> (V)	60	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	0.018
Q <sub>g</sub> (Max.) (nC)	110	
Q <sub>gs</sub> (nC)	29	
Q <sub>gd</sub> (nC)	36	
Configuration	Single	

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHFZ48RS-GE3
Lead (Pb)-free	IRFZ48RSPbF

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current <sup>e</sup>	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	A
		T <sub>C</sub> = 100 °C	
Pulsed Drain Current <sup>a, e</sup>	I <sub>DM</sub>	290	
Linear Derating Factor		1.3	W/°C
Single Pulse Avalanche Energy <sup>b, e</sup>	E <sub>AS</sub>	100	mJ
Maximum Power Dissipation	P <sub>D</sub>	190	W
Peak Diode Recovery dV/dt <sup>c, e</sup>	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	For 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V<sub>DD</sub> = 25 V, Starting T<sub>J</sub> = 25 °C, L = 22 μH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 72 A (see fig. 12)
- I<sub>SD</sub> ≤ 72 A, dI/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 175 °C
- 1.6 mm from case
- Current limited by the package, (die current = 72 A)



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.8	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^c$		-	0.60	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 43\text{ A}^b$	-	-	0.018	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 25\text{ V}, I_D = 43\text{ A}^b$		27	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$ , see fig. 5 <sup>c</sup>		-	2400	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	1300	-	
Reverse Transfer Capacitance	$C_{rss}$			-	190	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 72\text{ A}, V_{DS} = 48\text{ V},$ see fig. 6 and 13 <sup>b, c</sup>	-	-	110	nC
Gate-Source Charge	$Q_{gs}$			-	-	29	
Gate-Drain Charge	$Q_{gd}$			-	-	36	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 72\text{ A},$ $R_g = 9.1\text{ }\Omega, R_D = 0.34\text{ }\Omega$ , see fig. 10 <sup>b, c</sup>		-	8.1	-	ns
Rise Time	$t_r$			-	250	-	
Turn-Off Delay Time	$t_{d(off)}$			-	210	-	
Fall Time	$t_f$			-	250	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	50 <sup>c</sup>	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	290	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 72\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.0	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 72\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b, c$		-	120	180	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.50	0.80	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$
- c. Current limited by the package, (die current = 72 A)



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

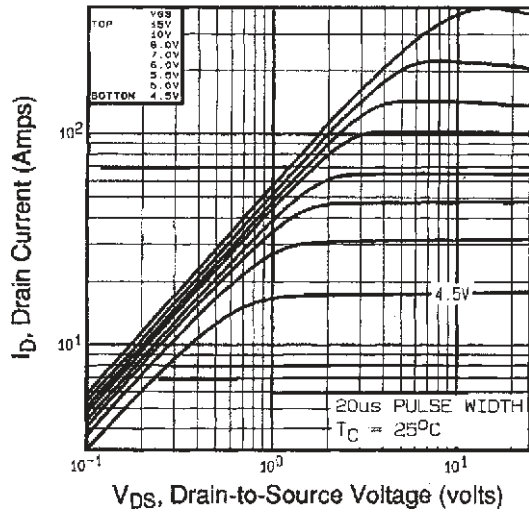


Fig. 1 - Typical Output Characteristics

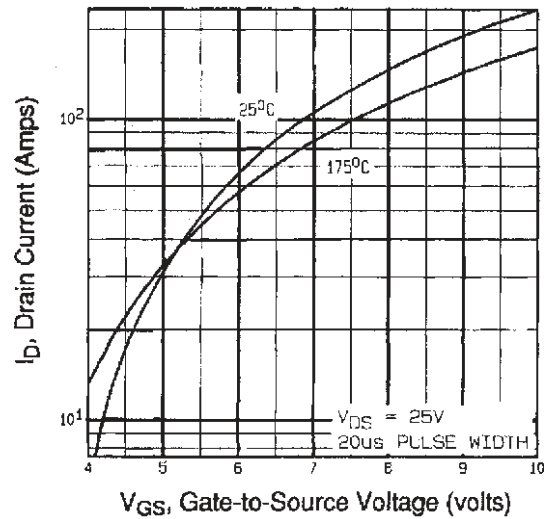


Fig. 2 - Typical Transfer Characteristics

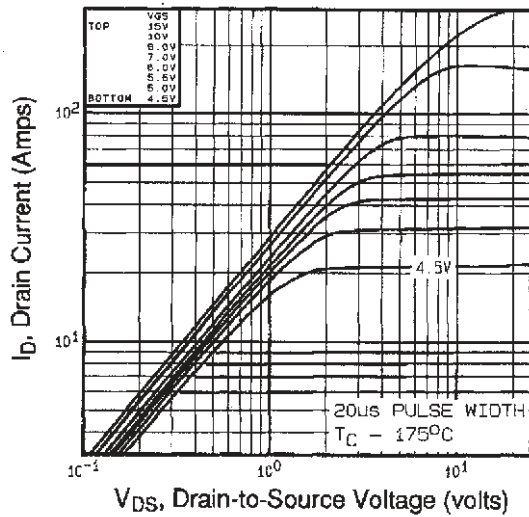


Fig. 1 - Typical Output Characteristics

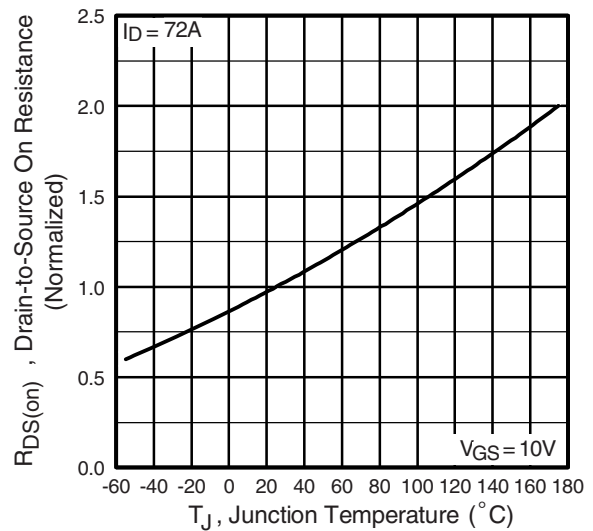


Fig. 3 - Normalized On-Resistance vs. Temperature

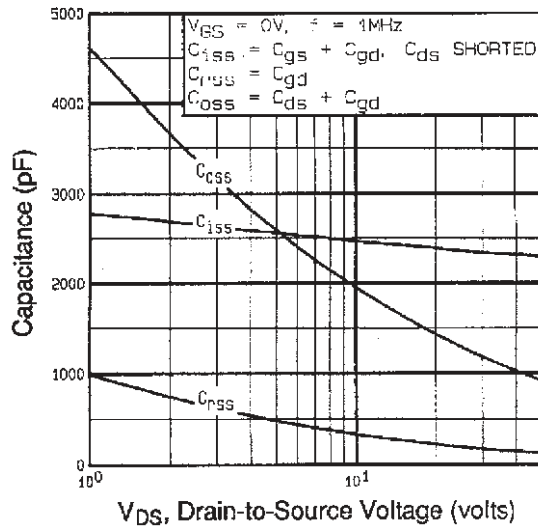


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

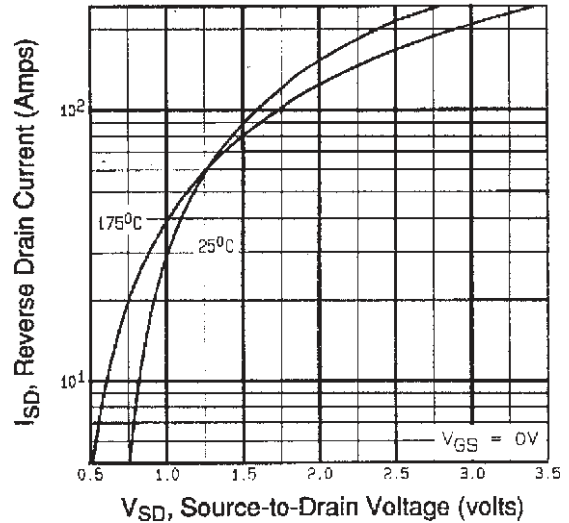


Fig. 6 - Typical Source-Drain Diode Forward Voltage

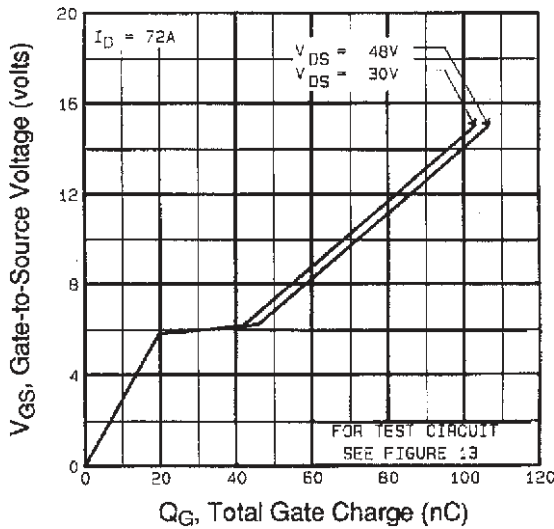


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

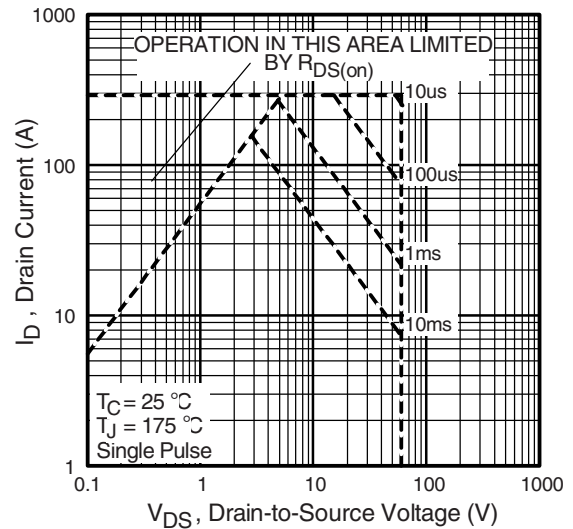


Fig. 7 - Maximum Safe Operating Area

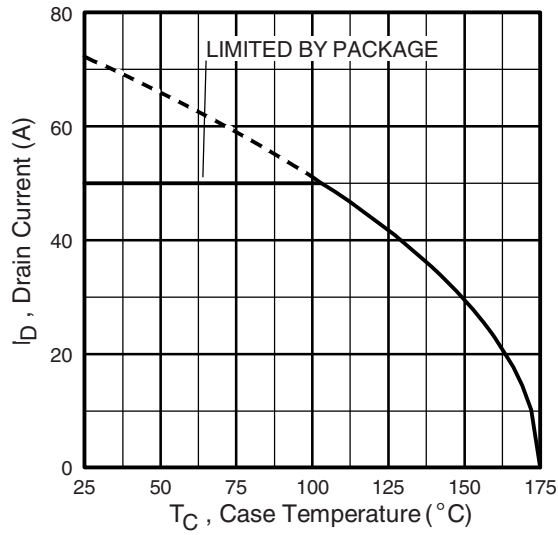


Fig. 8 - Maximum Drain Current vs. Case Temperature

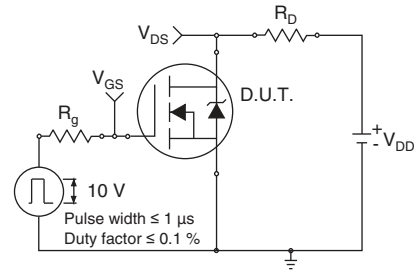


Fig. 10a - Switching Time Test Circuit

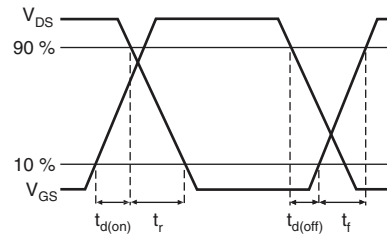


Fig. 10b - Switching Time Waveforms

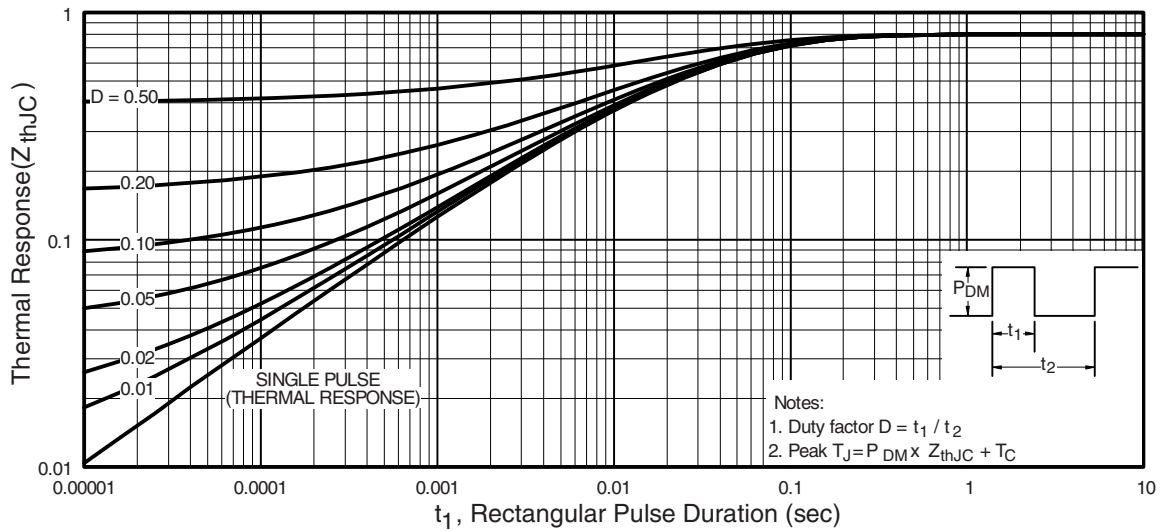


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

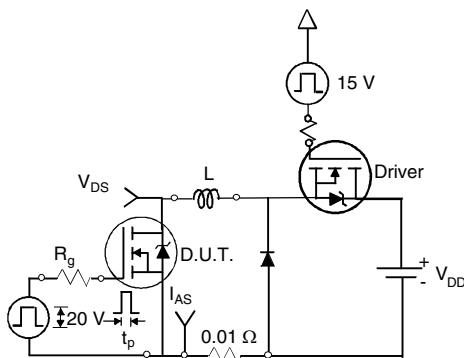


Fig. 12a - Unclamped Inductive Test Circuit

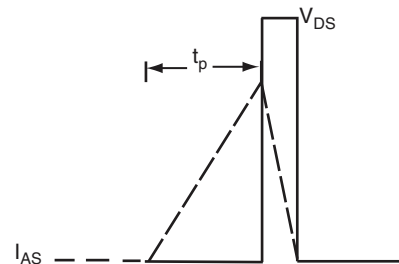


Fig. 12b - Unclamped Inductive Waveforms

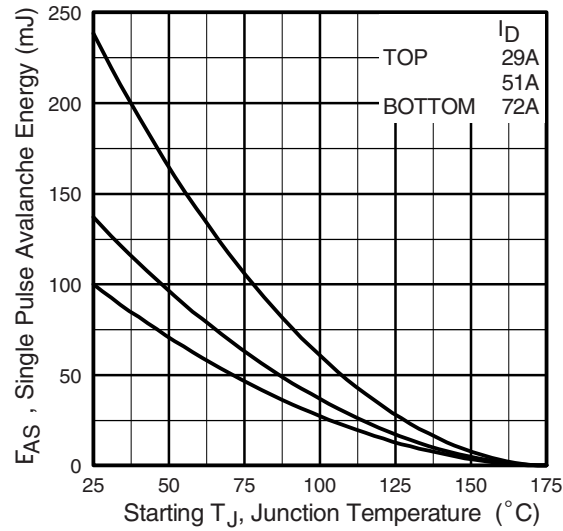


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

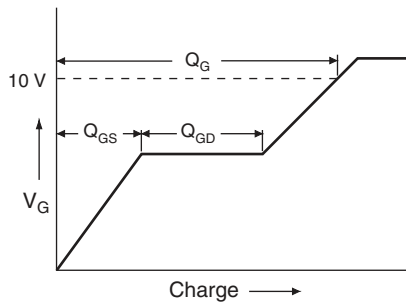


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

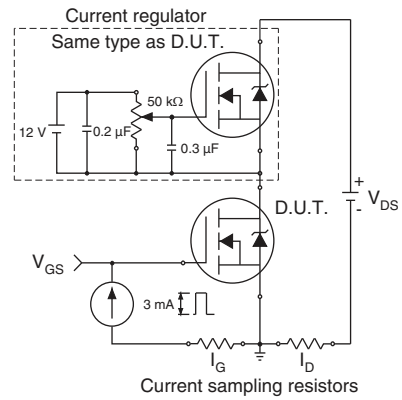
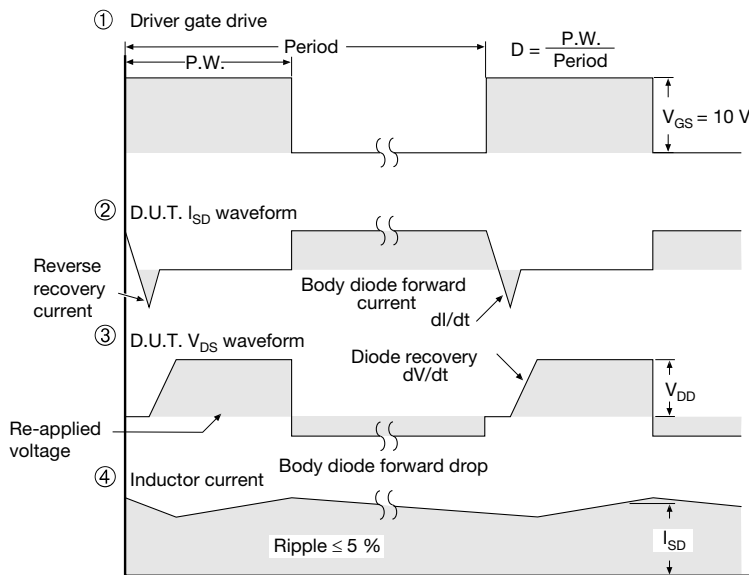
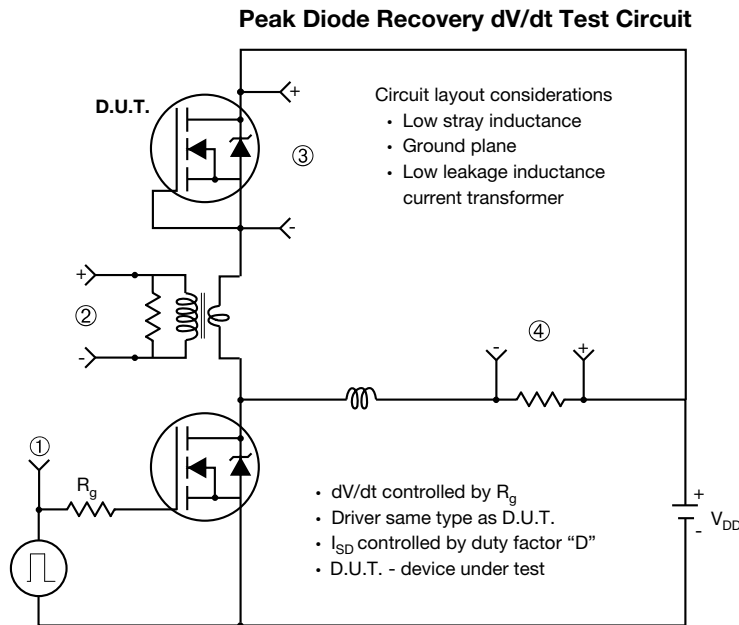


Fig. 13b - Gate Charge Test Circuit



**Note**  
 a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 10 - For N-Channel**

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### TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



## I<sup>2</sup>PAK (TO-262) (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08  
DWG: 5977

### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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