

## Power MOSFET

**TO-220 FULLPAK**


N-Channel MOSFET

### FEATURES

- Isolated package
- High voltage isolation = 2.5 kV<sub>RMS</sub> (t = 60 s; f = 60 Hz)
- Sink to lead creepage distance = 4.8 mm
- Dynamic dV/dt rating
- Low thermal resistance
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

### DESCRIPTION

Third generation power MOSFETs from Vishay provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

### PRODUCT SUMMARY

V <sub>DS</sub> (V)	600	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	1.2
Q <sub>g</sub> (Max.) (nC)	60	
Q <sub>gs</sub> (nC)	8.3	
Q <sub>gd</sub> (nC)	30	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIBC40GPbF

### ABSOLUTE MAXIMUM RATINGS T<sub>C</sub> = 25 °C, unless otherwise noted


PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V <sub>DS</sub>	600	V	
Gate-source voltage	V <sub>GS</sub>	± 20		
Continuous drain current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	A	
		T <sub>C</sub> = 100 °C		
Pulsed drain current <sup>a</sup>	I <sub>DM</sub>	14		
Linear derating factor		0.32	W/°C	
Single pulse avalanche energy <sup>b</sup>	E <sub>AS</sub>	500	mJ	
Repetitive avalanche current <sup>a</sup>	I <sub>AR</sub>	3.5	A	
Repetitive avalanche energy <sup>a</sup>	E <sub>AR</sub>	4.0	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	40	W
Peak diode recovery dV/dt <sup>c</sup>	dV/dt	3.0	V/ns	
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300 <sup>d</sup>		
Mounting torque	M3 screw	0.6		

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 74 mH, R<sub>G</sub> = 25 Ω, I<sub>AS</sub> = 3.5 A (see fig. 12)
- I<sub>SD</sub> ≤ 6.2 A, dI/dt ≤ 80 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C
- 1.6 mm from case



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	65	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	3.1	

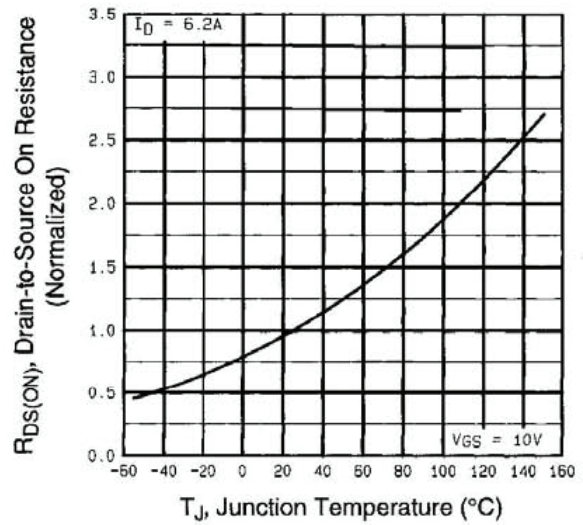
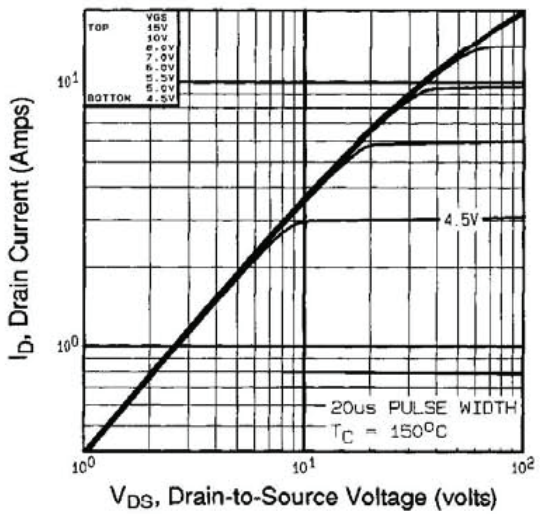
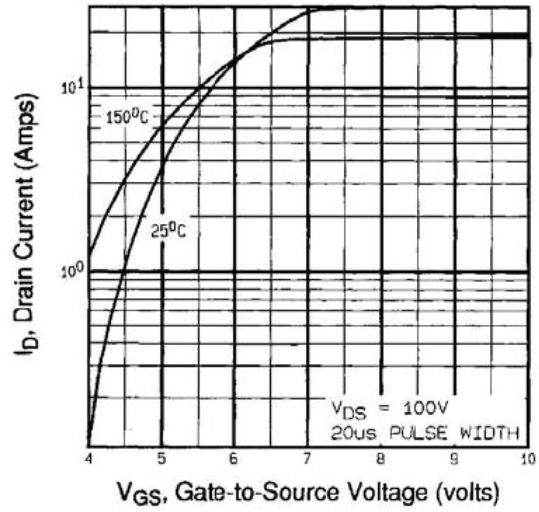
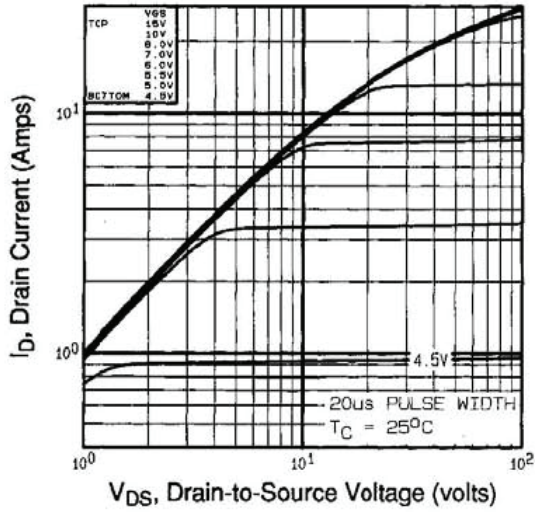
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.70	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	100	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 2.1\text{ A}^b$	-	-	1.2	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 2.1\text{ A}$		4.9	-	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	1300	-	pF
Output capacitance	$C_{oss}$			-	160	-	
Reverse transfer capacitance	$C_{rss}$			-	30	-	
Drain to sink capacitance	$C$	$f = 1.0\text{ MHz}$		-	12	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 6.2\text{ A}, V_{DS} = 360\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	60	nC
Gate-source charge	$Q_{gs}$			-	-	8.3	
Gate-drain charge	$Q_{gd}$			-	-	30	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 6.2\text{ A}, R_G = 9.1\text{ }\Omega, R_D = 47\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	13	-	ns
Rise time	$t_r$			-	18	-	
Turn-off delay time	$t_{d(off)}$			-	55	-	
Fall time	$t_f$			-	20	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	3.5	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	14	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 3.5\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 6.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	470	940	ns
Body diode reverse recovery charge	$Q_{rr}$			-	4.0	7.9	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\text{ }\%$



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



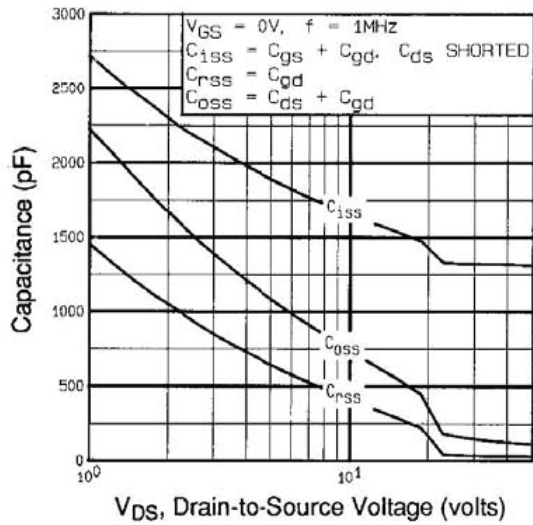


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

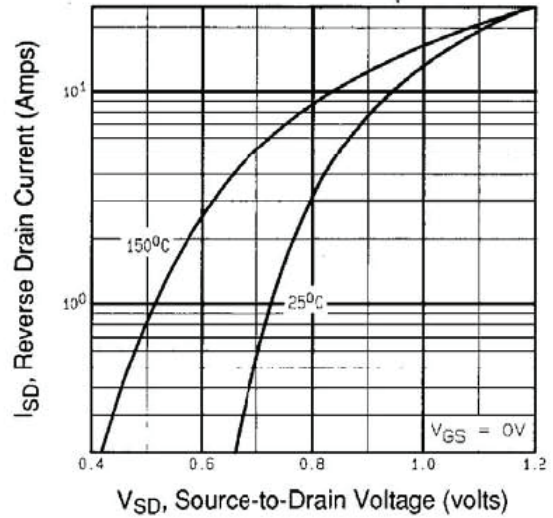


Fig. 7 - Typical Source-Drain Diode Forward Voltage

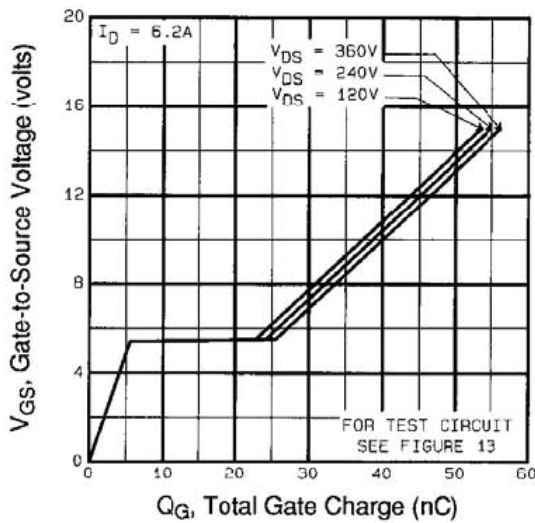


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

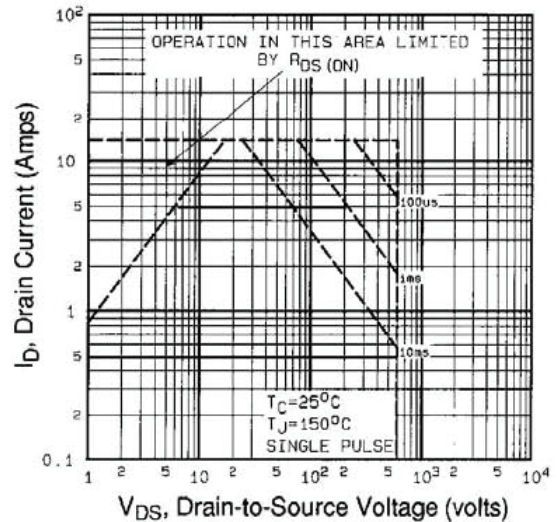


Fig. 8 - Maximum Safe Operating Area

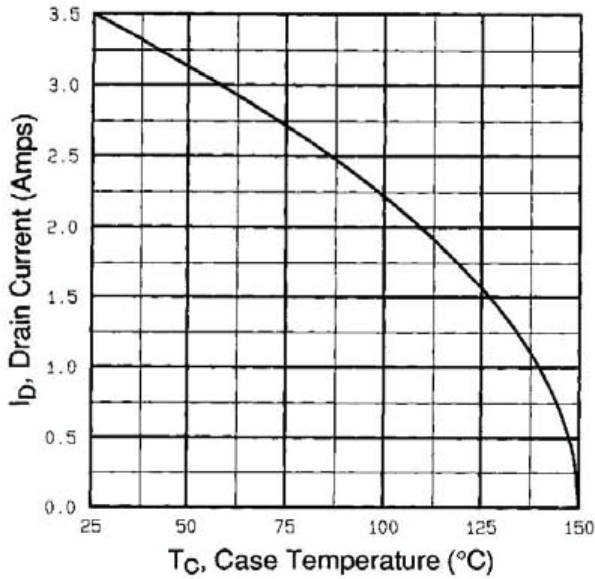


Fig. 9 - Maximum Drain Current vs. Case Temperature

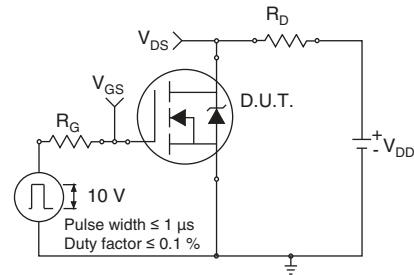


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

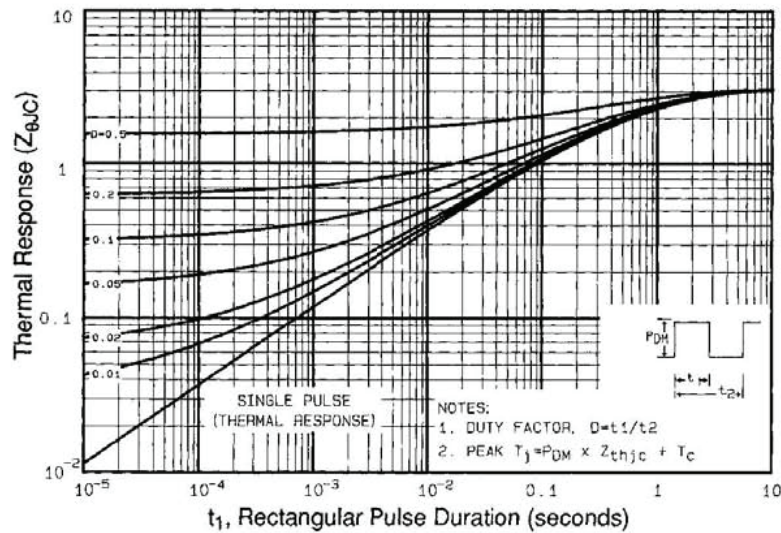


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

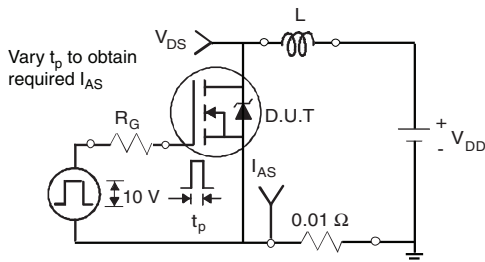


Fig. 12a - Unclamped Inductive Test Circuit

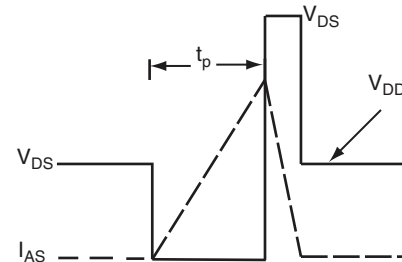


Fig. 12b - Unclamped Inductive Waveforms

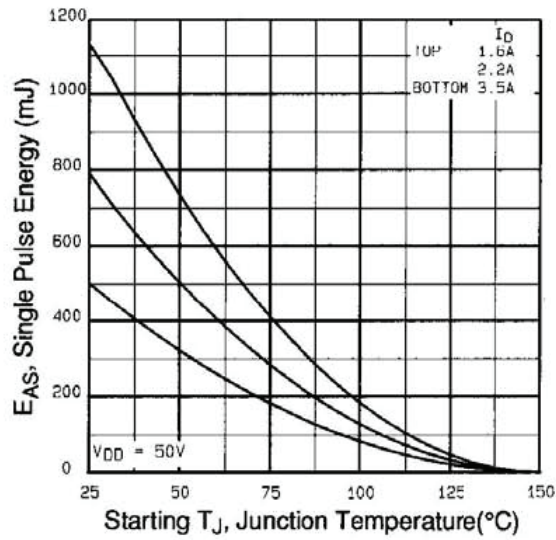


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

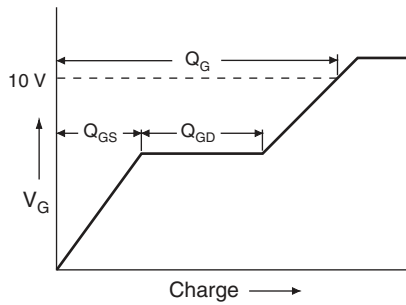


Fig. 13a - Basic Gate Charge Waveform

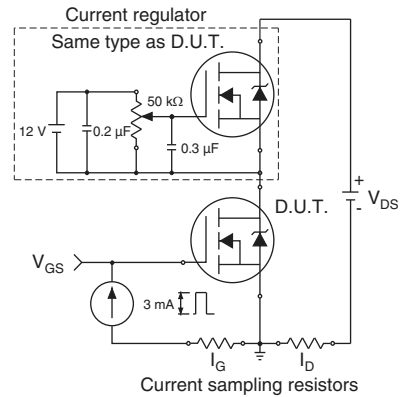
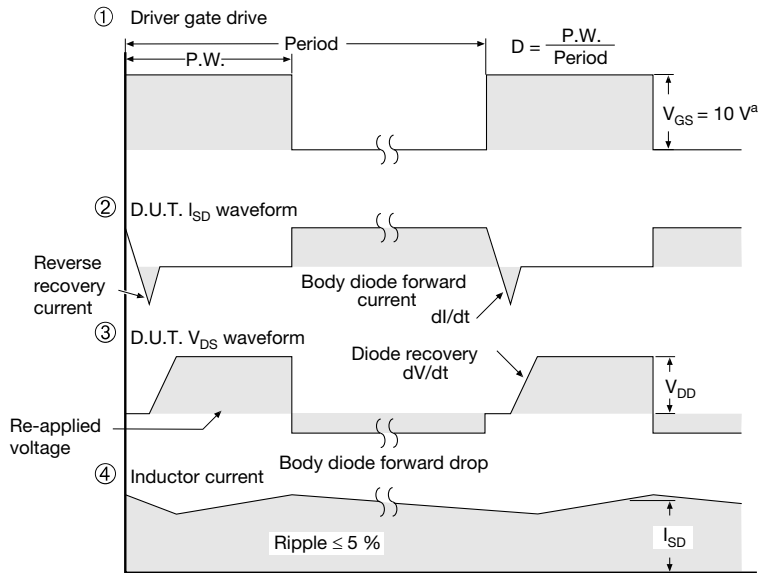
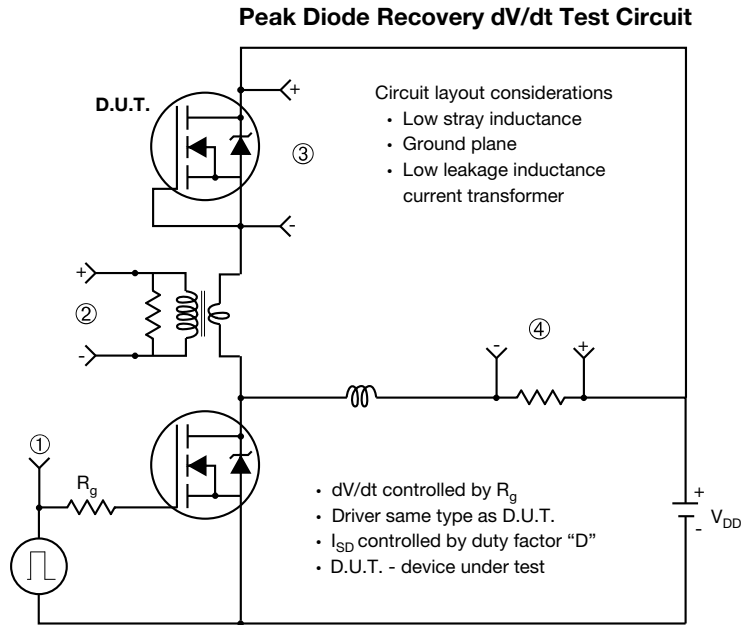


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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# TO-220 FULLPAK (High Voltage)

## OPTION 1: FACILITY CODE = 9



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
$\varnothing R$	3.08	3.18	3.28

### Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking





OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019  
DWG: 5972

Notes

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