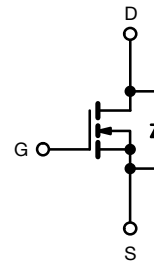
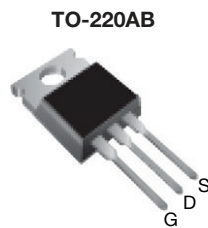


N-Channel 60 V(D-S) MOSFET

| PRODUCT SUMMARY | | |
|--------------------------|------------------------|-------|
| V _{DS} (V) | 60 | |
| R _{DS(on)} (Ω) | V _{GS} = 10 V | 0.072 |
| Q _g max. (nC) | 25 | |
| Q _{gs} (nC) | 5.8 | |
| Q _{gd} (nC) | 11 | |
| Configuration | Single | |

FEATURES

- Dynamic dV/dt rating
 - Fast switching
 - Ease of paralleling
- Simple drive requirements



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | |
|---|-------------------------|-----------------------------------|-------------------------|----------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | V _{DS} | 60 | V |
| Gate-Source Voltage | | V _{GS} | ± 20 | |
| Continuous Drain Current | V _{GS} at 10 V | I _D | T _C = 25 °C | 20 |
| | | | T _C = 100 °C | 12 |
| Pulsed Drain Current ^a | | I _{DM} | 68 | A |
| Linear Derating Factor | | | 0.40 | W/°C |
| Single Pulse Avalanche Energy ^b | | E _{AS} | 100 | mJ |
| Maximum Power Dissipation | | P _D | 60 | W |
| Peak Diode Recovery dV/dt ^c | | dV/dt | 4.5 | V/ns |
| Operating Junction and Storage Temperature Range | | T _J , T _{stg} | -55 to +175 | °C |
| Soldering Recommendations (Peak temperature) ^d | | | 300 | |
| Mounting Torque | 6-32 or M3 screw | | 10 | lbf · in |
| | | | 1.1 | N · m |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V_{DD} = 25 V, starting T_J = 25 °C, L = 403 μH, R_g = 25 Ω, I_{AS} = 17 A (see fig. 12).
- I_{SD} ≤ 17 A, di/dt ≤ 140 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
- 1.6 mm from case.

| THERMAL RESISTANCE RATINGS | | | | |
|-------------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W |
| Case-to-Sink, Flat, Greased Surface | R_{thCS} | 0.50 | - | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 2.5 | |

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|--|--|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 60 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | | - | 0.061 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 1.0 | - | 3.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 25 | μA |
| | | $V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$ | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 10\text{ A}^b$ | - | 0.072 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 25\text{ V}, I_D = 10\text{ A}$ | | 5.5 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$, see fig. 5 | | - | 640 | - | pF |
| Output Capacitance | C_{oss} | | | - | 360 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 79 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 17\text{ A}, V_{DS} = 48\text{ V},$ see fig. 6 and 13 ^b | - | - | 25 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 5.8 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 11 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 30\text{ V}, I_D = 17\text{ A},$ $R_g = 18\text{ }\Omega, R_D = 1.7\text{ }\Omega$, see fig. 10 ^b | | - | 13 | - | ns |
| Rise Time | t_r | | | - | 58 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 25 | - | |
| Fall Time | t_f | | | - | 42 | - | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact | | - | 4.5 | - | nH |
| Internal Source Inductance | L_S | | | - | 7.5 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode | | - | - | 20 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | | - | - | 68 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 17\text{ A}, V_{GS} = 0\text{ V}^b$ | | - | - | 1.5 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | | - | 88 | 180 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | - | 0.29 | 0.64 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\text{ }\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

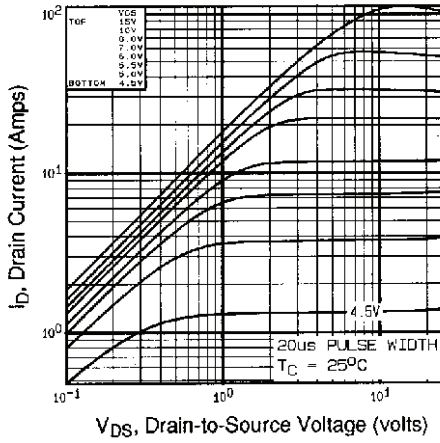


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ C$



Fig. 4 - Normalized On-Resistance vs. Temperature

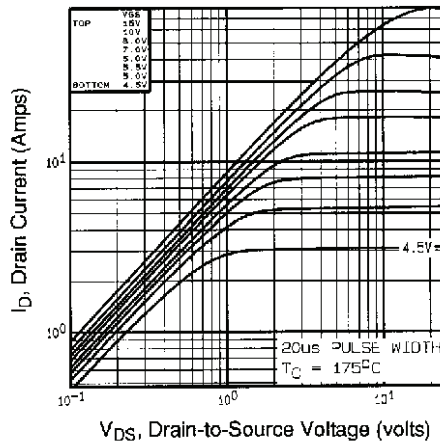


Fig. 2 - Typical Output Characteristics, $T_C = 175^\circ C$

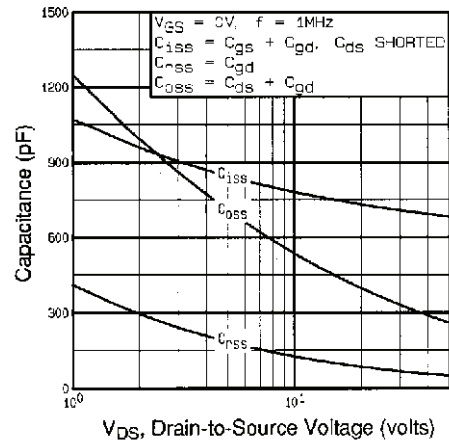


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

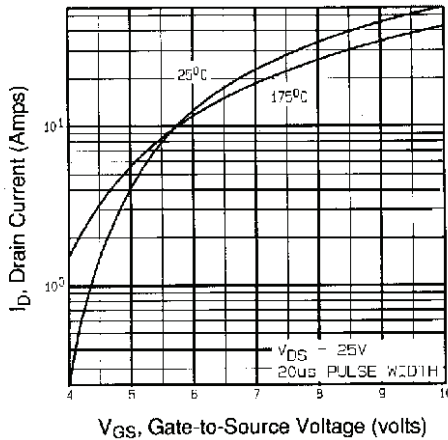


Fig. 3 - Typical Transfer Characteristics



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 8 - Maximum Safe Operating Area

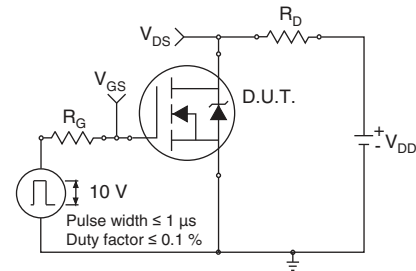


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

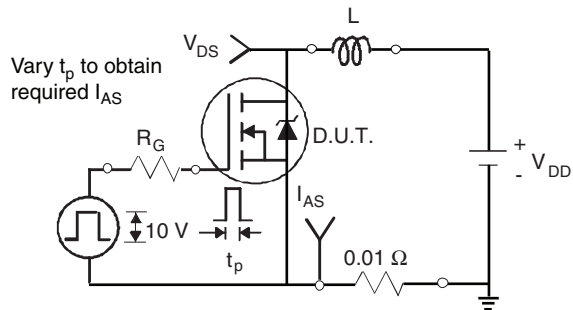


Fig. 12a - Unclamped Inductive Test Circuit

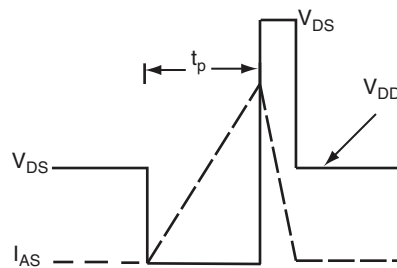


Fig. 12b - Unclamped Inductive Waveforms

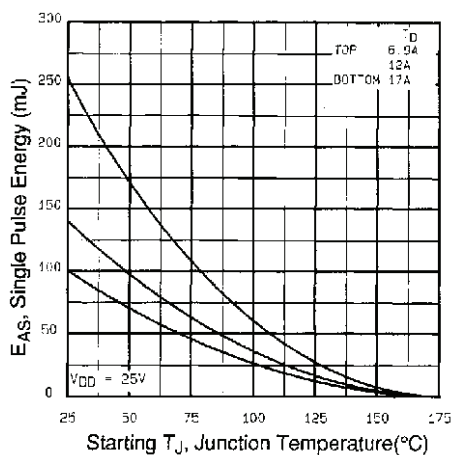


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

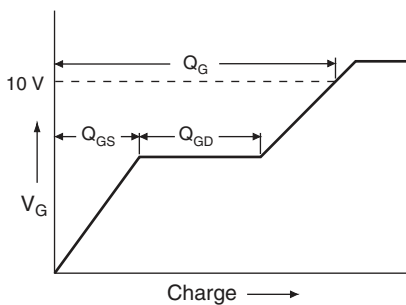


Fig. 13a - Basic Gate Charge Waveform

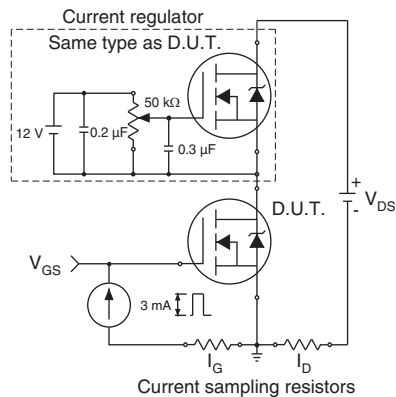
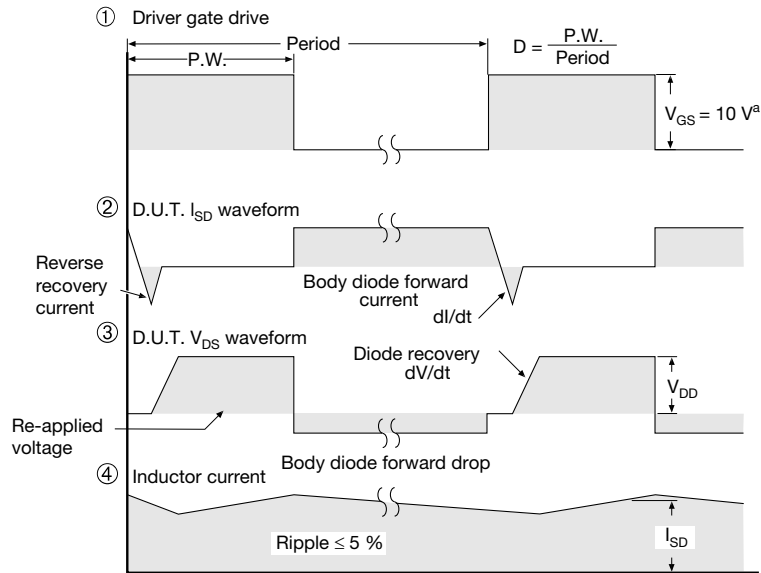
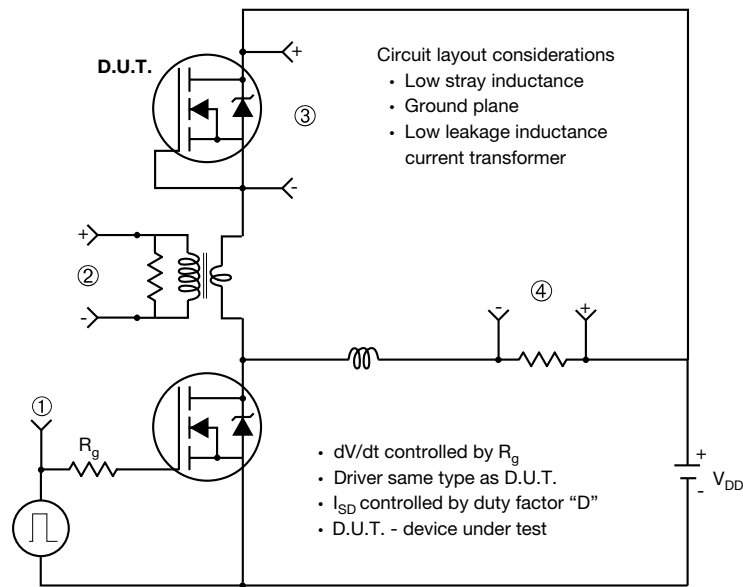


Fig. 13b - Gate Charge Test

Peak Diode Recovery dV/dt Test Circuit

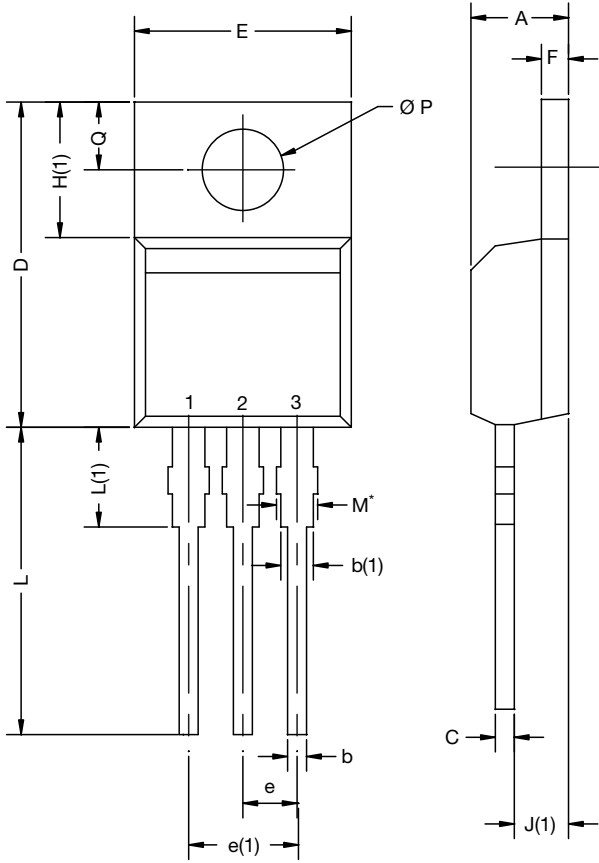


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-220



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.24 | 4.65 | 0.167 | 0.183 |
| b | 0.69 | 1.02 | 0.027 | 0.040 |
| b(1) | 1.14 | 1.78 | 0.045 | 0.070 |
| c | 0.36 | 0.61 | 0.014 | 0.024 |
| D | 14.33 | 15.85 | 0.564 | 0.624 |
| E | 9.96 | 10.52 | 0.392 | 0.414 |
| e | 2.41 | 2.67 | 0.095 | 0.105 |
| e(1) | 4.88 | 5.28 | 0.192 | 0.208 |
| F | 1.14 | 1.40 | 0.045 | 0.055 |
| H(1) | 6.10 | 6.71 | 0.240 | 0.264 |
| J(1) | 2.41 | 2.92 | 0.095 | 0.115 |
| L | 13.36 | 14.40 | 0.526 | 0.567 |
| L(1) | 3.33 | 4.04 | 0.131 | 0.159 |
| Ø P | 3.53 | 3.94 | 0.139 | 0.155 |
| Q | 2.54 | 3.00 | 0.100 | 0.118 |

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DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

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