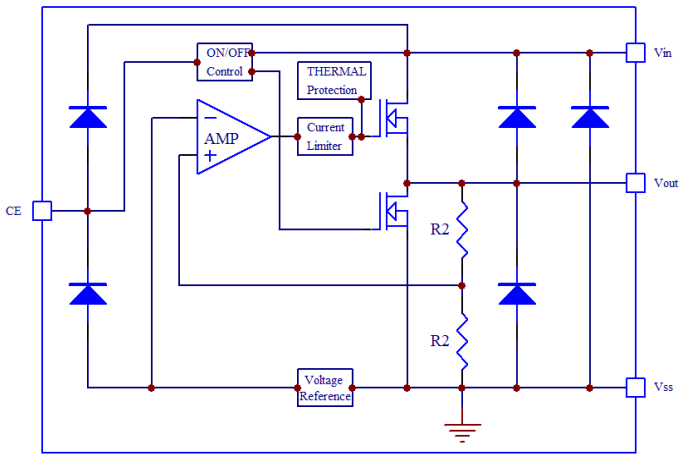
NH6302 Series

Low Dropout Regulator

INTRODUCTION

The NH6302 series are a group of positive voltage regulators manufactured by CMOS technologies with low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small. The NH6675 series can deliver 150mA output current and allow an input voltage as high as 50V. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

INTERNAL BOX DIAGRAM



MODEL DIFINITION

NH6375①②③④

DESIGNATOR	SYMBOL	DESCRIPTION
①	A B	Without EN With Shutdown Function
②	Integer	Output Voltage,e.g: 3.3V=33,5.0V=50 12V=120
③	M/ MC/ MY MF/MR	Package:SOT-23-3 Package:SOT-23-5
④	- 1	2% Accuracy 1% Accuracy

FEATURES

- Low Quiescent Current: 2uA
- Operating Voltage Range: 2.5V~18V
- Output Current: 300mA
- Low Dropout Voltage:
- 160mV@100mA(VOUT=3.3V)
- Output Voltage: 1.2~ 12V
- High Accuracy: ±2%/±1%(Typ.)
- High Power Supply Rejection Ratio:
  65dB@1kHz
- Low Output Noise:
  $27xV_{OUT}$ μVRMS (10Hz~100kHz)
- Excellent Line and Load Transient Response
- Built-in Current Limiter, Short-Circuit Protection
- Over-Temperature Protection

- Wireless Communication Equipments
- Portable Audio Video Equipments

- Car Navigation Systems
- LAN Cards

- Ultra Low Power Microcontroller

APPLICATIONS

- Cordless Phones
- Radio control systems
- Laptop, Palmtops and PDAs
- Single-lens reflex DSC
- PC peripherals with memory

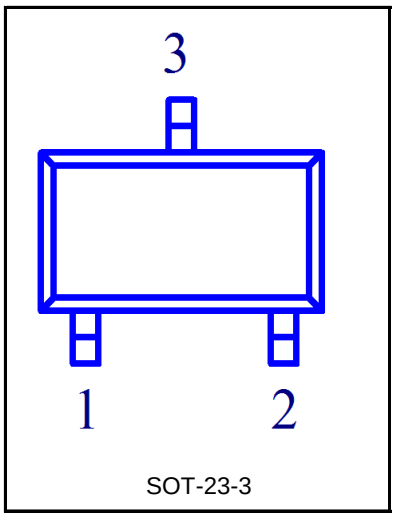
MARKING

Model	Marking
NH6302①②③④	Model code+YW

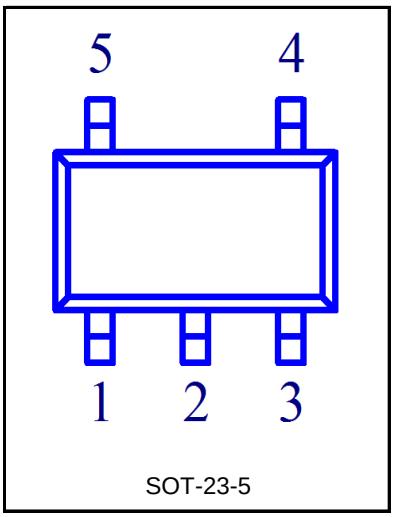
NH6302 Series

Low Dropout Regulator

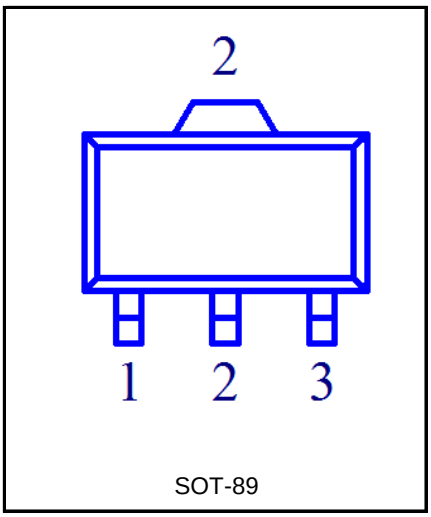
PIN Diagram Discription



SOT-23-3



SOT-23-5



SOT-89

NH6375Axx Series Pin Function Discription

PIN NUMBER						PIN NAME	FUNCTION DISCRIPTION
SOT-23-3			SOT-89-3				
M	MC	MY	P	PT	PL		
1	3	3	1	2	2	V_{SS}	Ground
2	2	1	3	1	3	V_{OUT}	Output
3	1	2	2	3	1	V_{IN}	Power input

NH6375Bxx Series Pin Function Discription

PIN NUMBER	PIN NAME	FUNCTION DISCRIPTION
SOT-23-5		
1	V_{IN}	Power input Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	NC	NO Connection
5	V_{OUT}	Output

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	RATINGS	Unit
Input Voltage (Note 2)	V_{IN}	-0.3~24	V
Output Voltage (Note 2)	V_{out}	-0.3~10	
CE Pin Voltage (Note 2)	V_{ce}	-0.3~24	
Output Current	I_{out}	600	mA
Maximum Power Dissipation SOT-23	P_D	0.4	W
Maximum Power Dissipation SOT-89		0.6	
ESD rasting (Note 3) HBM		8	KV
ESD rasting (Note 3) MM		400	V

THERMAL CHARACTERISTICS

Parameter	Symbol	Max.	Unit
Junction Temperature	T_j	-55 to +125	°C
Storage Temperature	T_{Stg}	-55 to +125	°C
Lead Temperature(Soldering, 10 sec)	T_{SOLDER}	260	°C

Note:

1.Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation ofthe device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

2.All voltages are with respect to network ground terminal.

3. ESD testing is performed according to the respective JESD22 JEDEC standard.The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

RECOMMENDED OPERATING CONDITIONS

Parameter	min.	nom.	max.	Unit
Supply voltage at VIN	2.5		18	V
Operating junction temperature range, Tj	-40		125	°C
Operating free air temperature range, TA	-40		85	°C

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ELECTRICAL CHARACTERISTICS(VIN=VOUT+1V, CIN=COUT=1μF,TA=25°C,unless otherwise specified)

PARAMETER	Condition	Symbol	Min.	Typ.(Note5)	Max.	Unit
Input Voltage	N/A	V_{IN}	2.5	-	18	V
Output Voltage Range	N/A	V_{OUT}	1.2	-	5	V
DC Output Accuracy	I_{OUT}=1mA		-2	-	2	%
			-1	-	1	%
Dropout Voltage(note 6)	I_{OUT}=100mA,V_{OUT}=3.3V	V_{DIF}	-	160	-	mV
Supply Current	I_{OUT}=0mA VIN≤5.0V	I_{SS}	-	2	5	uA
	I_{OUT}=0mA VIN≥5.0V			5	10	
Line Regulation	Iout=10mA V_{OUT}+1V≤V_{IN}≤18V	$\frac{\Delta Vout}{(Voutx\Delta VIN)}$	-	0.01	0.3	%/V
Load Regulation	V_{IN}= V_{OUT}+1V, 1mA≤I_{OUT}≤100mA	ΔVout	-	10	-	mV
Temperature Coefficient	I_{OUT}=10mA, -40°C<T_A<125°C	$\frac{\Delta Vout}{(Voutx\Delta TA)}$	-	50	-	ppm/°C
Output Current Limit	V_{OUT}= 0.5 x $V_{OUT(Normal)}$, V_{IN}=5v	I_{LIM}	350	500	-	mA
Short Current	V_{OUT} =V_{SS}	I_{SHORT}	-	25	-	mA
Power Supply Rejection Ratio	IOUT= 50mA, 100Hz	PSRR	-	80	-	dB
	IOUT= 50mA, 1KHZ		-	65	-	
	IOUT= 50mA, 10KHZ		-	50	-	
	IOUT= 50mA, 100KHZ		-	45	-	
Output Noise Voltage	BW=10Hz to 100kHz	V_{ON}	-	27 x V_{OUT}	-	uV_{RMS}
Thermal Shutdown Temperature	N/A	T_{SD}	-	150	-	°C
Thermal Shutdown Hysteresis	N/A	ΔT_{SD}	-	20	-	°C
CE"High"Voltage	N/A	V_{CE}"H"	1.5		V_{IN}	V
CE"Low"Voltage	N/A	V_{CE}"L"			0.3	V

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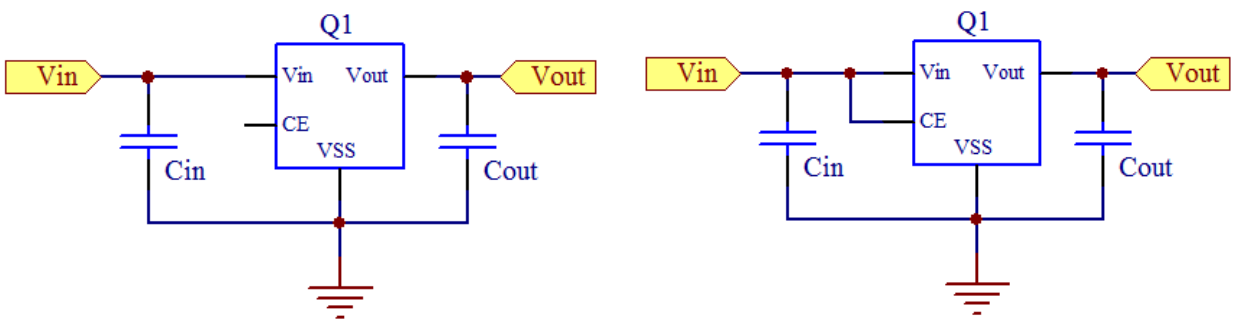
TYPICAL APPLICATION CIRCUIT



SELECTION OF INPUT/OUTPUT CAPACITORS

Phase compensation is provided to secure operation even when the load current is varied.For this purpose. use a 1.0uF or more output capacitor (Cout) with good frequency characteristics and proper ESR (Equivalent Series Resistance).Connect a 1.0uF or more input capacitor(CIN)between the Vin pin and the Vss pin as close as possible to the pins. The value of the output overshoot or undershoot transient response varies depending on the value of the outout capacitor. When selecting the output capacitor, perform sufficient evaluation, including evaluation of temperature characteristicson the actual device.

In the design of portable devices the ceramic capacitors are often chosen because of their small size, low equivalent series resistance (ESR) and high RMS current capability. Alsodesigners have been looking to ceramic capacitors due to shortages of tantalum capacitors.

Unfortunately, using ceramic capacitors for input filtering can cause problems. Applying avoltage step to a ceramic capacitor causes a large current surge that stores energy in the inductances of the power leads. A large voltage spike is created when the stored energy is transferred from these inductances into the ceramic capacitor. These voltage spikes can easily be twice the amplitude of the input voltage step. (See “Ceramic Input Capacitors CanCause Overvoltage Transients”——Linear Technology application note 88, March 2001)

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors (MLCC). Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the LDO input to a live power source. Adding a 3Ω resistor in series with an X5R ceramic capacitor will minimizestart-up voltage transients.

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RATINGANDCHARACTERISTICCURVES

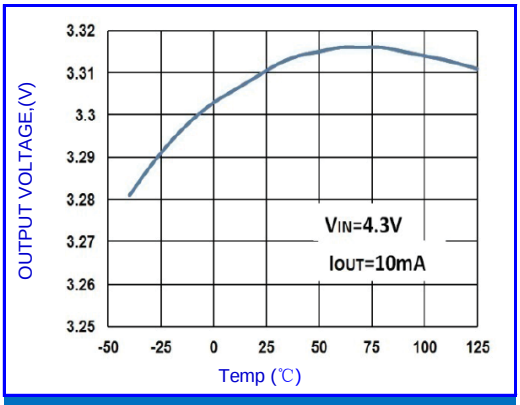

Fig.1-OUTPUT VOLTAGE VS. TEMPERATURE

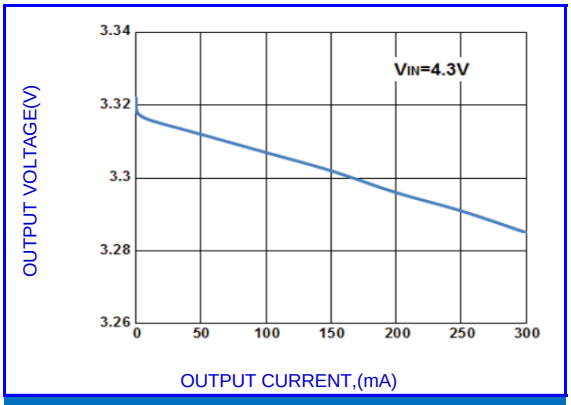

Fig.2-OUTPUT VOLTAGE VS. OUTPUT CURRENT

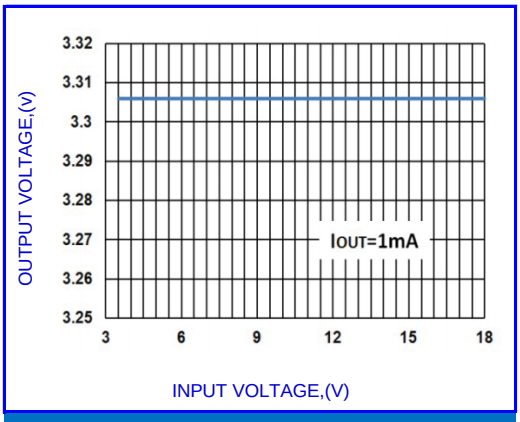

Fig.3-OUTPUT VOLTAGE VS. INPUT VOLTAGE

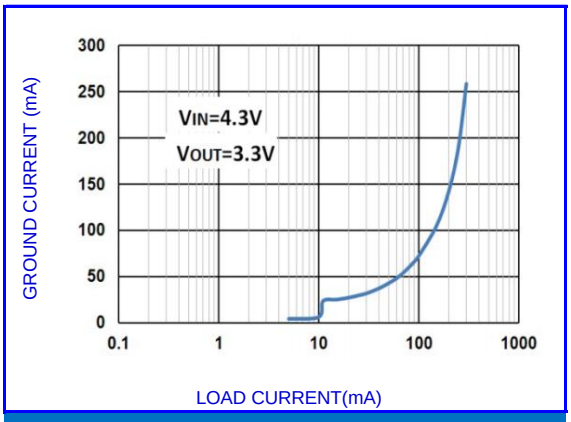

Fig.4-GROUND CURRENT VS. LOAD CURRENT

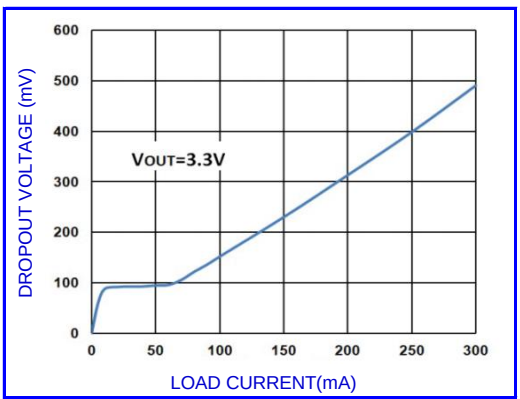

Fig.5-MAX. DROPOUT VOLTAGE VS. LOAD CURRENT

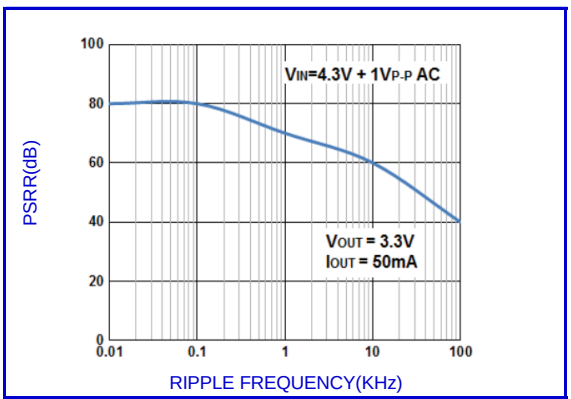

Fig.6-PSRR VS. FREQUENCY

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RATINGANDCHARACTERISTICCURVES

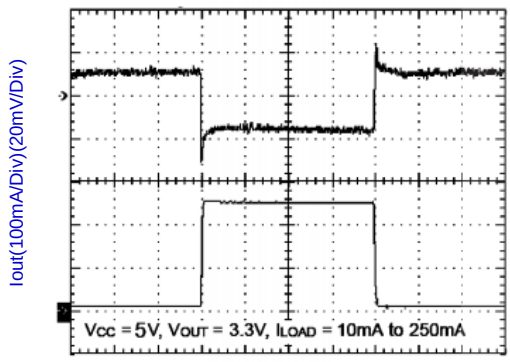

Fig.7-LOAD TRANSIENT RESPONSE

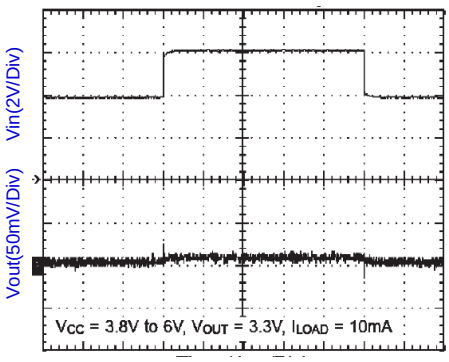

Fig.8- LINE TRANSIENT RESPONSE

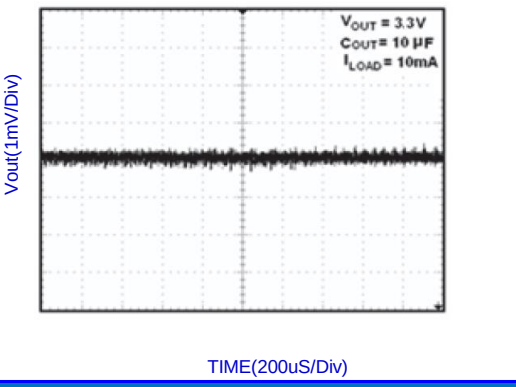

Fig.9- OUTPUT NOISE 10Hz to 100KHz

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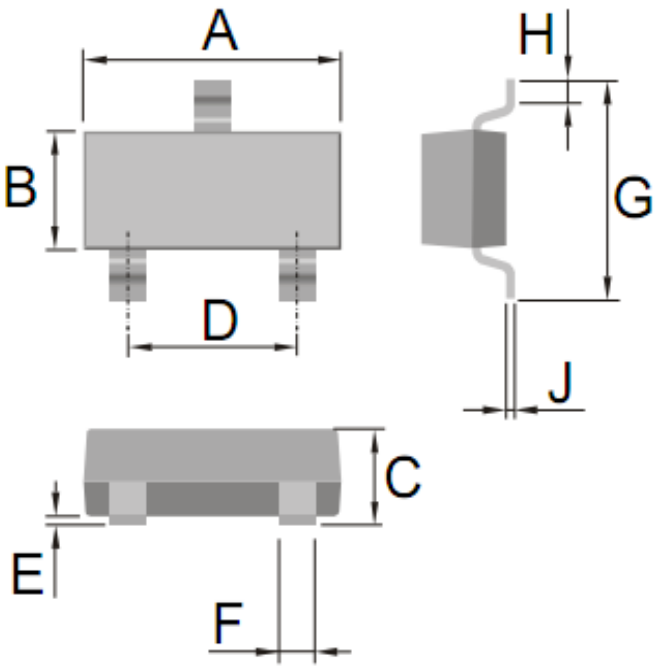
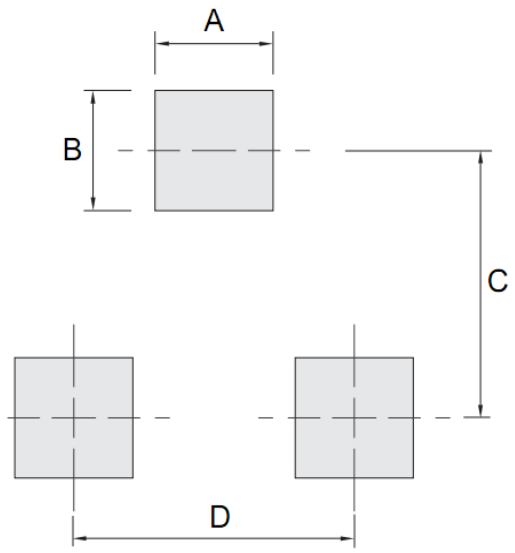
OUTLINE DRAWINGS — SOT-23-3



OUTLINE DIMENSIONS

Dim.	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.820	-	3.020	0.1110	-	0.1189
B	1.500	-	1.700	0.0591	-	0.0669
C	1.050	-	1.250	0.0413	-	0.0492
D	1.800	-	2.000	0.0709	-	0.0787
E	0.000	-	0.100	0.0000	-	0.0039
F	0.300	-	0.500	0.0118	-	0.0197
G	2.650	-	2.950	0.1043	-	0.1161
H	0.300	-	0.600	0.0118	-	0.0236
J	0.100	-	0.200	0.0039	-	0.0079

OUTLINE DRAWINGS — SOT-23-3



OUTLINE DIMENSIONS

Dim.	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	0.800	-	-	0.0315	-
B	-	0.900	-	-	0.0354	-
C	-	2.400	-	-	0.0945	-
D	-	1.900	-	-	0.0748	-

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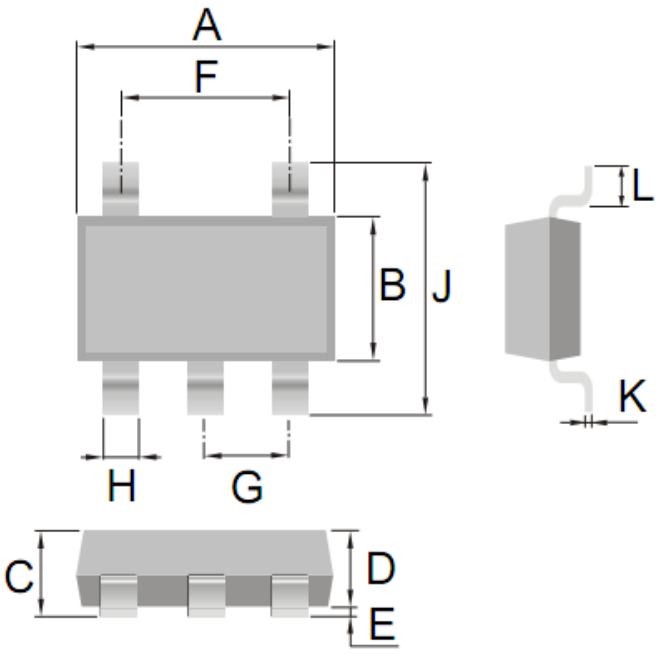
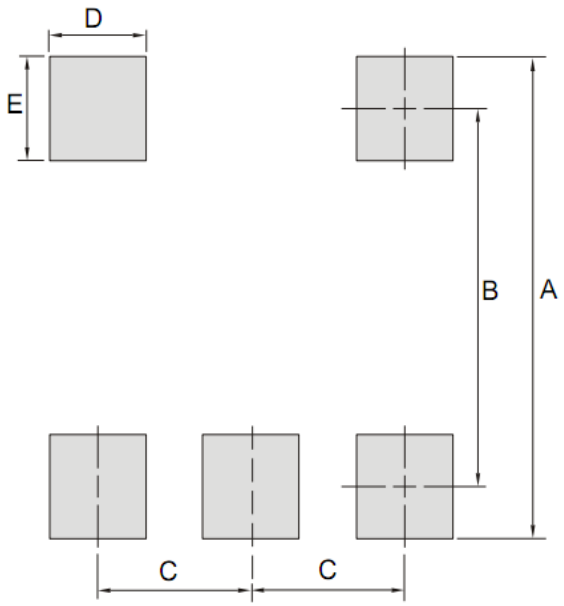
OUTLINE DRAWINGS — SOT-23-5



OUTLINE DIMENSIONS						
Dim.	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.820	-	3.020	0.1110	-	0.1189
B	1.500	-	1.700	0.0591	-	0.0669
C	1.050	-	1.250	0.0413	-	0.0492
D	1.050	-	1.150	0.0413	-	0.0453
E	0.000	-	0.100	0.0000	-	0.0039
F	1.800	-	2.000	0.0709	-	0.0787
G	0.900	-	1.000	0.0354	-	0.0394
H	0.300	-	0.500	0.0118	-	0.0197
J	2.650	-	2.950	0.1043	-	0.1161
K	0.100	-	0.200	0.0039	-	0.0079
L	0.300	-	0.600	0.0118	-	0.0236

OUTLINE DRAWINGS — SOT-23-5



RECOMMEDNED MOUNTING PAD DIMENSIONS						
Dim.	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	3.200	-	-	0.1260	-
B	-	2.250	-	-	0.0886	-
C	-	0.950	-	-	0.0374	-
D	-	0.600	-	-	0.0236	-
E	-	0.950	-	-	0.0374	-

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OUTLINE DRAWINGS

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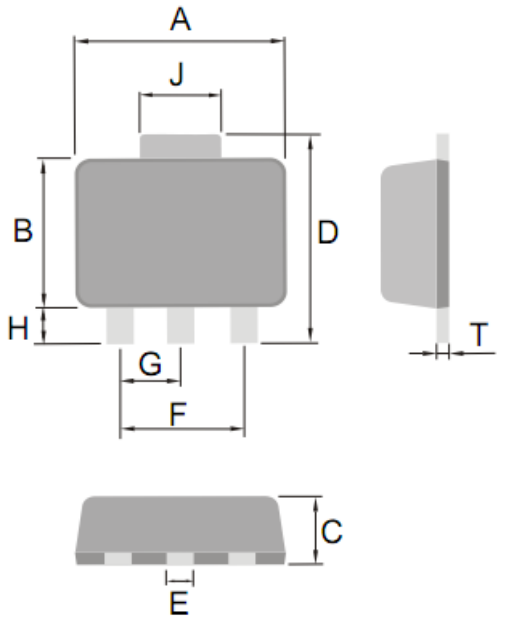
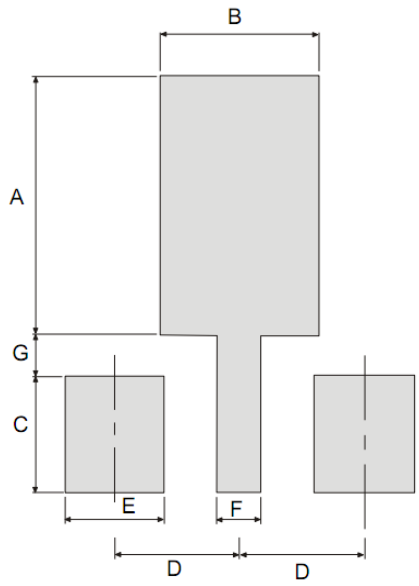


OUTLINE DIMENSIONS						
Dim.	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.400	-	4.600	0.1732	-	0.1811
B	2.300	-	2.600	0.0906	-	0.1024
C	1.400	-	1.600	0.0551	-	0.0630
D	3.940	-	4.250	0.1551	-	0.1673
E	0.320	-	0.520	0.0126	-	0.0205
F	-	3.000	-	-	0.1181	-
G	-	1.500	-	-	0.0591	-
H	0.900	-	1.200	0.0354	-	0.0472
T	0.350	-	0.440	-	#VALUE!	-

RECOMMEDNED LAYOUT DRAWINGS

SOT-89



RECOMMEDNED MOUNTING PAD DIMENSIONS						
Dim.	Milimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	4.000	-	-	0.1575	-
B	-	2.400	-	-	0.0945	-
C	-	1.800	-	-	0.0709	-
D	-	1.900	-	-	0.0748	-
E	-	1.500	-	-	0.0591	-
F	-	0.700	-	-	0.0276	-
G	-	0.600	-	-	0.0236	-

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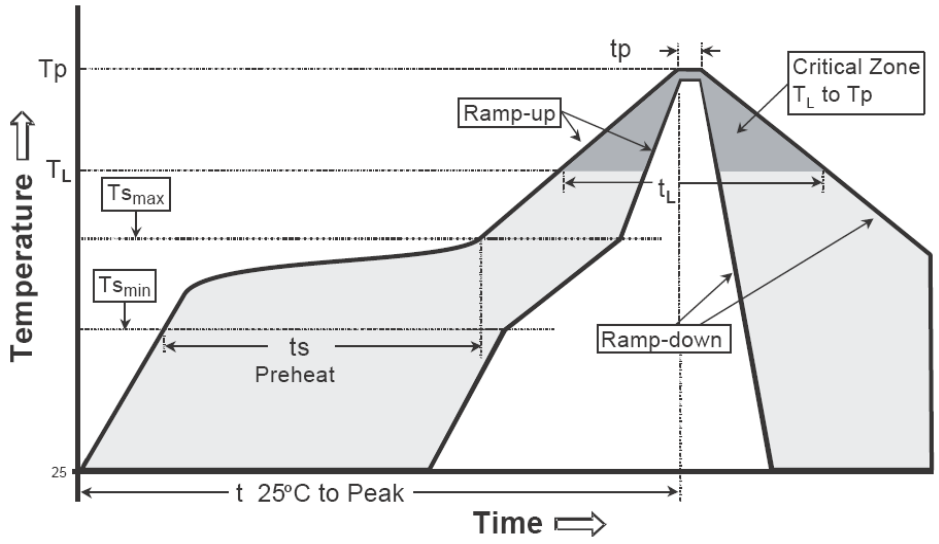
Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(TS min) −Temperature Max(TS max) −Time(ts min to ts max)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

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