General Description

The 74HC597/74HCT597 is an 8-bit shift register with input flip-flops

Features

- Supply voltage range:
  SN74HC597: 2~6V
  SN74HCT597: 4.5~5.5V
- Input levels:
  SN74HC597: CMOS level
  SN74HCT597: TTL level
- Temperature range:-40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74HC597N	DIP-16	74HC597N	Tube	1000Pcs/Box
XBLW SN74HC597DTR	SOP-16	74HC597	Tape	2500Pcs/Reel
XBLW SN74HC597TDTR	TSSOP-16	74HC597	Tape	3000Pcs/Reel
XBLW SN74HCT597N	DIP-16	74HCT597N	Tube	1000Pcs/Box
XBLW SN74HCT597DTR	SOP-16	74HCT597	Tape	2500Pcs/Reel
XBLW SN74HCT597TDTR	TSSOP-16	74HCT597	Tape	3000Pcs/Reel

Block Diagram And Pin Description

Block Diagram

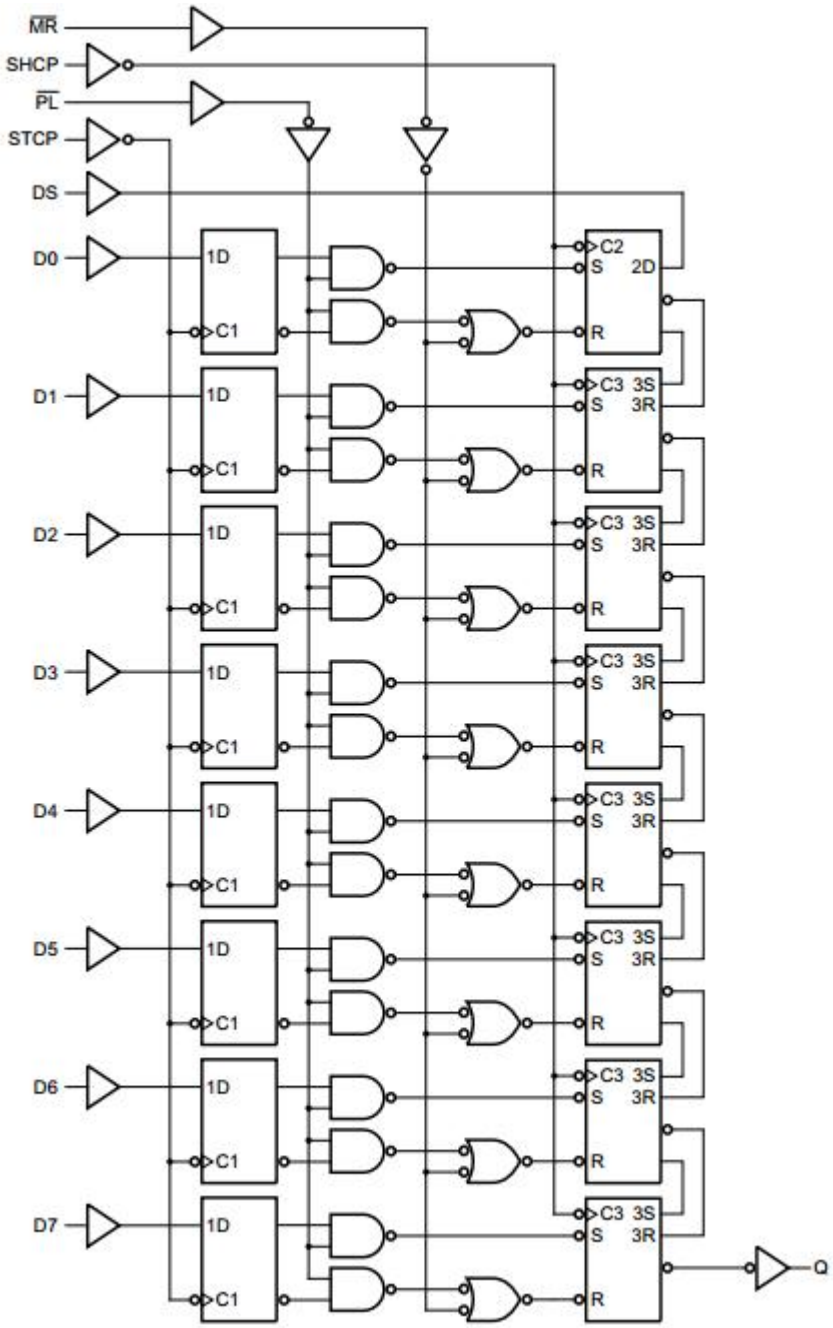
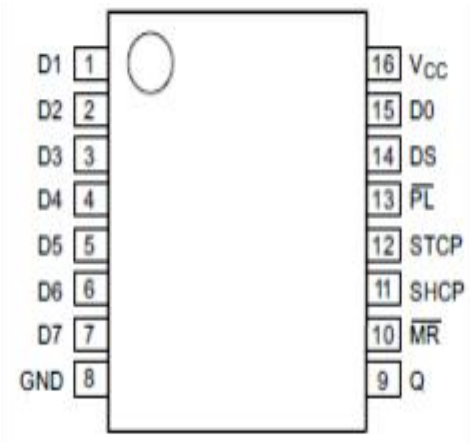


Figure 1. Logic symbol

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	D1	parallel data output
2	D2	parallel data output
3	D3	parallel data output
4	D4	parallel data output
5	D5	parallel data outputt
6	D6	parallel data output
7	D7	parallel data output
8	GND	ground (0V)
9	Q	serial data output
10	$\overline{MR}$	asynchronous master reset input (active LOW)
11	SHCP	shift register clock input (LOW-to-HIGH, edge-triggered)
12	STCP	storage register clock input (LOW-to-HIGH, edge-triggered)
13	$\overline{PL}$	parallel load input (active LOW)
14	DS	serial data input
15	D0	parallel data inputs
16	V_{CC}	supply voltage

Function Table

Input				Function
STCP	SHCP	$\overline{PL}$	$\overline{MR}$	
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
No clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register is indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked Qn = Qn-1, Q0 = DS

Note: H=HIGH voltage level; L=LOW voltage level. ↑=LOW-to-HIGH transition .X= don't care

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7	V
ground current	I_{GND}	-		-50	-	mA
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	-0.5V < V_O < V_{CC}+0.5V		-	±25	mA
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74HC597						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃
SN74HCT597						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	℃

Electrical Characteristics

DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Vcc	Conditions	Min.	Typ.	Max.	Unit
SN74HC597							
HIGH-level input voltage	V_{IH}	2.0V	-	1.5	1.2	-	V
		4.5V	-	3.15	2.4	-	V
		6.0V	-	4.2	3.2	-	V
LOW-level input voltage	V_{IL}	2.0V	-	-	0.8	0.5	V
		4.5V	-	-	2.1	1.35	V
		6.0V	-	-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	2.0V	I_O=-20uA	1.9	2.0	-	V
		4.5V	I_O=-20uA	4.4	4.5	-	V
		6.0V	I_O=-20uA	5.9	6.0	-	V
		4.5V	I_O=-4.0mA	3.84	4.32	-	V
		6.0V	I_O=-5.2mA	5.34	5.81	-	V
LOW-level output voltage	V_{OL}	2.0V	I_O=20uA	-	0	0.1	V
		4.5V	I_O=20uA	-	0	0.1	V
		6.0V	I_O=20uA	-	0	0.1	V
		4.5V	I_O=4.0mA	-	0.15	0.33	V
		6.0V	I_O=5.2mA	-	0.16	0.33	V
input leakage current	I_I	6.0V	V_I=V_{CC} or GND	-	-	±2	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND;I_O=0A	-	-	80	uA
SN74HCT597							
HIGH-level input voltage	V_{IH}	4.5~ 5.5V	-	2.0	1.6	-	V
LOW-level input voltage	V_{IL}	4.5~ 5.5V	-	-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4.0mA	3.84	4.32	-	V
LOW-level output voltage	V_{OL}	4.5V	I_O=20uA	-	0	0.1	V
			I_O=4.0mA	-	0.15	0.33	V
input leakage current	I_I	5.5V	V_I=V_{CC} or GND	-	-	±2	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND;I_O=0A	-	-	80	uA
additional supply current	ΔI_{CC}	4.5~ 5.5V	One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A	-	-	135	uA

DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Vcc	Conditions	Min.	Typ.	Max.	Unit
SN74HC597							
HIGH-level input voltage	V_{IH}	2.0V	-	1.5	-	-	V
		4.5V	-	3.15	-	-	V
		6.0V	-	4.2	-	-	V
LOW-level input voltage	V_{IL}	2.0V	-	-	-	0.5	V
		4.5V	-	-	-	1.35	V
		6.0V	-	-	-	1.8	V
HIGH-level output voltage	V_{OH}	2.0V	I_O=-20uA	1.9	-	-	V
		4.5V	I_O=-20uA	4.4	-	-	V
		6.0V	I_O=-20uA	5.9	-	-	V
		4.5V	I_O=-4.0mA	3.7	-	-	V
		6.0V	I_O=-5.2mA	5.2	-	-	V
LOW-level output voltage	V_{OL}	2.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=20uA	-	-	0.1	V
		6.0V	I_O=20uA	-	-	0.1	V
		4.5V	I_O=4.0mA	-	-	0.4	V
		6.0V	I_O=5.2mA	-	-	0.4	V
input leakage current	I_I	6.0V	V_I=V_{CC} or GND	-	-	±4	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND;I_O=0A	-	-	160	uA
SN74HCT597							
HIGH-level input voltage	V_{IH}	4.5~ 5.5V	-	2.0	-	-	V
LOW-level input voltage	V_{IL}	4.5~ 5.5V	-	-	-	0.8	V
HIGH-level output voltage	V_{OH}	4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	4.5V	I_O=20uA	-	-	0.1	V
			I_O=4.0mA	-	-	0.4	V
input leakage current	I_I	5.5V	V_I=V_{CC} or GND	-	-	±4	uA
supply current	I_{CC}	6.0V	V_I=V_{CC} or GND;I_O=0A	-	-	160	uA
additional supply current	ΔI_{CC}	4.5~ 5.5V	One input at V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A	-	-	147	uA

AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Vcc	Conditions		Min.	Typ.	Max.	Unit
SN74HC597								
SHCP to Q propagation delay	t_{PLH}, t_{PHL}	2.0V	C_L=50pF	see Figure 5	-	55	220	ns
		4.5V	C_L=50pF		-	20	44	ns
		5.0V	C_L=15pF		-	17	-	ns
		6.0V	C_L=50pF		-	16	37	ns
$\overline{MR}$ to Q propagation delay		2.0V	C_L=50pF	see Figure 6	-	58	220	ns
		4.5V	C_L=50pF		-	21	44	ns
		6.0V	C_L=50pF		-	17	37	ns
STCP to Q propagation delay		2.0V	C_L=50pF	see Figure 5	-	80	315	ns
		4.5V	C_L=50pF		-	29	63	ns
		5.0V	C_L=15pF		-	25	-	ns
		6.0V	C_L=50pF		-	23	54	ns
$\overline{PL}$ to Q propagation delay		2.0V	C_L=50pF	see Figure 7	-	69	270	ns
		4.5V	C_L=50pF		-	25	54	ns
		5.0V	C_L=15pF		-	21	-	ns
		6.0V	C_L=50pF		-	20	46	ns
transition time	tt	2.0V	C_L=50pF	see Figure 5	-	19	95	ns
		4.5V	C_L=50pF		-	7	19	ns
		6.0V	C_L=50pF		-	6	16	ns
STCP(HIGH or LOW) pulse width	tw	2.0V	C_L=50pF	see Figure 5	100	11	-	ns
		4.5V	C_L=50pF		20	4	-	ns
		6.0V	C_L=50pF		17	3	-	ns
SHCP(HIGH or LOW) pulse width		2.0V	C_L=50pF	see Figure 5	100	14	-	ns
		4.5V	C_L=50pF		20	5	-	ns
		6.0V	C_L=50pF		17	4	-	ns
$\overline{MR}$ LOW		2.0V	C_L=50pF	see Figure 6	100	22	-	ns
		4.5V	C_L=50pF		20	8	-	ns
		6.0V	C_L=50pF		17	6	-	ns
$\overline{PL}$ LOW		2.0V	C_L=50pF	see Figure 7	100	22	-	ns
		4.5V	C_L=50pF		20	8	-	ns
		6.0V	C_L=50pF		17	6	-	ns
Dn to STCP Set_up time	tsu	2.0V	C_L=50pF	see Figure 9	75	8	-	ns
		4.5V	C_L=50pF		15	3	-	ns
		6.0V	C_L=50pF		13	2	-	ns
DS to SHCP Set_up time		2.0V	C_L=50pF	see Figure 9	75	11	-	ns
		4.5V	C_L=50pF		15	4	-	ns
		6.0V	C_L=50pF		13	3	-	ns
$\overline{PL}$ to SHCP Set_up time		2.0V	C_L=50pF	see Figure 10	75	11	-	ns
		4.5V	C_L=50pF		15	4	-	ns
		6.0V	C_L=50pF		13	3	-	ns
Dn to STCP hold time	th	2.0V	C_L=50pF	see Figure 9	5	-3	-	ns
		4.5V	C_L=50pF		5	-1	-	ns
$\overline{MR}$ to SHCP recovery time	trec	4.5V	C_L=50pF	see Figure 8	15	-2	-	ns
maximum frequency	fmax	4.5V	C_L=15pF	see Figure 5	24	75	-	MHZ
		5.0V	C_L=15pF		-	83	-	MHZ

AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Vcc	Conditions		Min.	Typ.	Max.	Unit
SN74HC597								
SHCP to Q propagation delay	t_{PLH}, t_{PHL}	2.0V	C_L=50pF	see Figure 5	-	-	265	ns
		4.5V	C_L=50pF		-	-	53	ns
		6.0V	C_L=50pF		-	-	45	ns
$\overline{MR}$ to Q propagation delay		2.0V	C_L=50pF	see Figure 6	-	-	265	ns
		4.5V	C_L=50pF		-	-	53	ns
		6.0V	C_L=50pF		-	-	45	ns
STCP to Q propagation delay		2.0V	C_L=50pF	see Figure 5	-	-	375	ns
		4.5V	C_L=50pF		-	-	75	ns
		6.0V	C_L=50pF		-	-	64	ns
$\overline{PL}$ to Q propagation delay		2.0V	C_L=50pF	see Figure 7	-	-	325	ns
		4.5V	C_L=50pF		-	-	65	ns
		6.0V	C_L=50pF		-	-	55	ns
transition time	tt	2.0V	C_L=50pF	see Figure 5	-	-	110	ns
		4.5V	C_L=50pF		-	-	22	ns
		6.0V	C_L=50pF		-	-	19	ns
STCP(HIGH or LOW) pulse width	tw	2.0V	C_L=50pF	see Figure 5	120	-	-	ns
		4.5V	C_L=50pF		24	-	-	ns
		6.0V	C_L=50pF		20	-	-	ns
SHCP(HIGH or LOW) pulse width		2.0V	C_L=50pF	see Figure 5	120	-	-	ns
		4.5V	C_L=50pF		24	-	-	ns
		6.0V	C_L=50pF		20	-	-	ns
$\overline{MR}$ LOW		2.0V	C_L=50pF	see Figure 6	120	-	-	ns
		4.5V	C_L=50pF		24	-	-	ns
		6.0V	C_L=50pF		20	-	-	ns
$\overline{PL}$ LOW		2.0V	C_L=50pF	see Figure 7	120	-	-	ns
		4.5V	C_L=50pF		24	-	-	ns
		6.0V	C_L=50pF		20	-	-	ns
Dn to STCP Set_up time	tsu	2.0V	C_L=50pF	see Figure 9	90	-	-	ns
		4.5V	C_L=50pF		18	-	-	ns
		6.0V	C_L=50pF		15	-	-	ns
DS to SHCP Set_up time		2.0V	C_L=50pF	see Figure 9	90	-	-	ns
		4.5V	C_L=50pF		18	-	-	ns
		6.0V	C_L=50pF		15	-	-	ns
$\overline{PL}$ to SHCP Set_up time		2.0V	C_L=50pF	see Figure 10	90	-	-	ns
		4.5V	C_L=50pF		18	-	-	ns
		6.0V	C_L=50pF		15	-	-	ns
Dn to STCP hold time	th	2.0V	C_L=50pF	see Figure 9	5	-	-	ns
		4.5V	C_L=50pF		5	-	-	ns
		6.0V	C_L=50pF		5	-	-	ns
DS to SHCP hold time		2.0V	C_L=50pF	see Figure 9	5	-	-	ns
		4.5V	C_L=50pF		5	-	-	ns

		6.0V	C_L=50pF		5	-	-	ns
$\overline{PL}$ to SHCP hold time		2.0V	C_L=50pF	see Figure 10	5	-	-	ns
		4.5V	C_L=50pF		5	-	-	ns
		6.0V	C_L=15pF		5	-	-	ns
$\overline{MR}$ to SHCP recovery time	trec	2.0V	C_L=50pF	see Figure 8	90	-	-	ns
		4.5V	C_L=50pF		18	-	-	ns
		6.0V	C_L=50pF		15	-	-	ns
SHCP maximum frequency	fmax	2.0V	C_L=50pF	see Figure 5	4.8	-	-	MHZ
		4.5V	C_L=50pF		24	-	-	MHZ
		6.0V	C_L=50pF		28	-	-	MHZ
SN74HCT597								
SHCP to Q propagation delay	t_{PLH}, t_{PHL}	4.5V	C_L=50pF	see Figure 5	-	-	60	ns
$\overline{MR}$ to Q propagation delay		4.5V	C_L=50pF	see Figure 6	-	-	74	ns
STCP to Q propagation delay		4.5V	C_L=50pF	see Figure 5	-	-	86	ns
$\overline{PL}$ to Q propagation delay		4.5V	C_L=50pF	see Figure 7	-	-	78	ns
transition time	tt	4.5V	C_L=50pF	see Figure 5	-	-	22	ns
STCP(HIGH or LOW) pulse width	tw	4.5V	C_L=50pF	see Figure 5	24	-	-	ns
SHCP(HIGH or LOW) pulse width		4.5V	C_L=50pF	see Figure 5	24	-	-	ns
$\overline{MR}$ LOW		4.5V	C_L=50pF	see Figure 6	38	-	-	ns
$\overline{PL}$ LOW		4.5V	C_L=50pF	see Figure 7	30	-		ns
Dn to STCP Set_up time	tsu	4.5V	C_L=50pF	see Figure 9	18	-	-	ns
DS to SHCP Set_up time		4.5V	C_L=50pF	see Figure 9	18	-	-	ns
$\overline{PL}$ to SHCP Set_up time		4.5V	C_L=50pF	see Figure 10	18	-	-	ns
Dn to SHCP hold time	th	4.5V	C_L=50pF	see Figure 9	5	-	-	ns
DS to SHCP hold time		4.5V	C_L=50pF	see Figure 9	5	-	-	ns
$\overline{PL}$ to SHCP hold time		4.5V	C_L=50pF	see Figure 10	5	-	-	ns
$\overline{MR}$ to SHCP recovery time	trec	4.5V	C_L=50pF	see Figure 8	18	-	-	ns
maximum frequency	fmax	4.5V	C_L=15pF	see Figure 5	20	-	-	MHZ

Testing Circuit

AC Testing Circuit

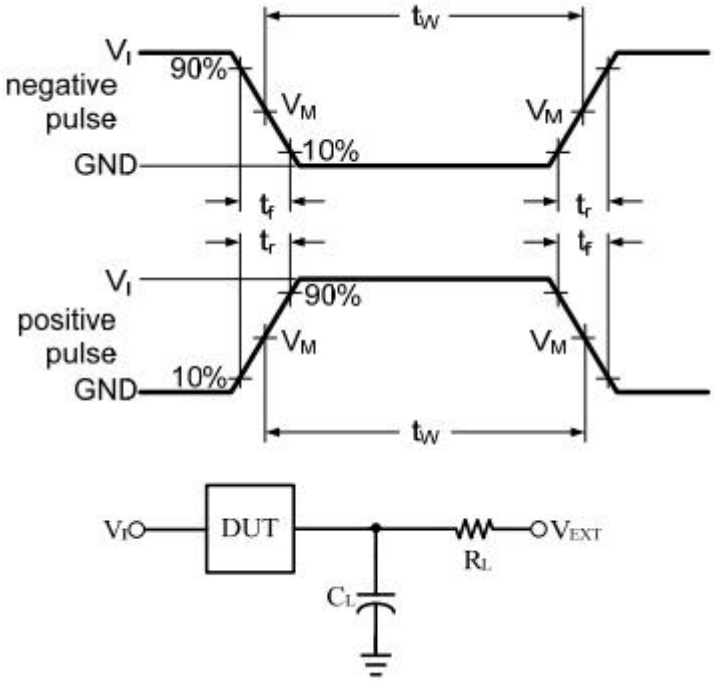


Figure 4. Test circuit for measuring switching times

CL includes probe and jig capacitance.

AC Testing Waveforms

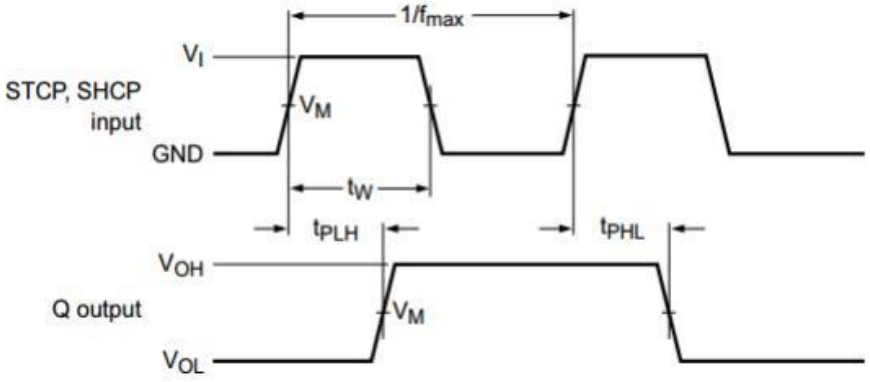


Figure 5. Shift clock and storage clock inputs to output, propagation delays, pulse widths and maximum clock frequency

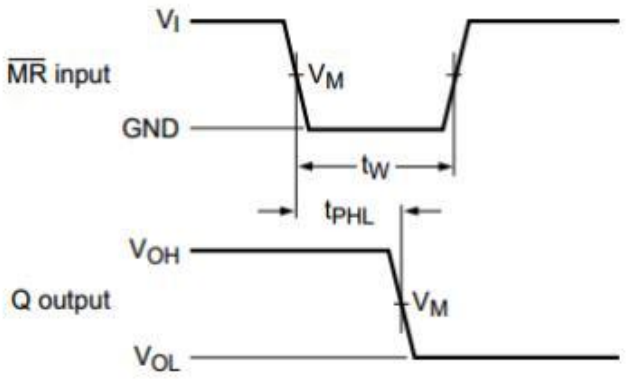


Figure 6. input ($\overline{M}$R) to (Q), output propagation delays and ($\overline{M}$R) pulse width

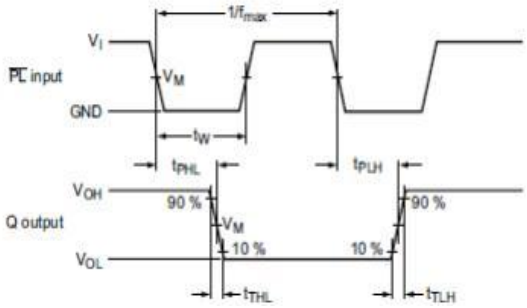


Figure 7 Input ($\overline{PL}$) to (Q), output propagation delays, $\overline{PL}$ pulse width and output transition times

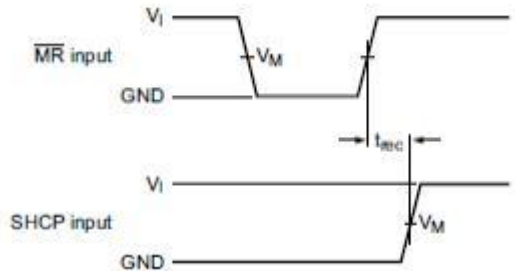


Figure 8 Input ($\overline{M}$R) to shift clock (SHCP) and storage clock (STCP) recovery times

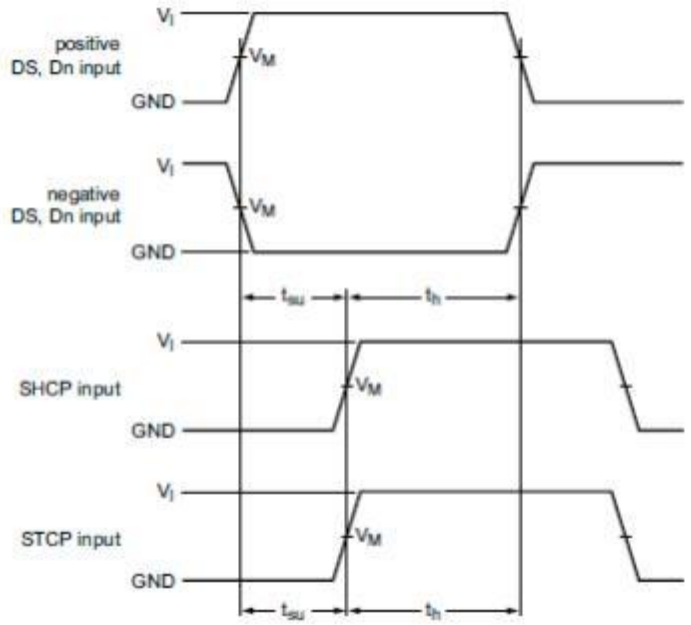


Figure 9 Hold and set-up times for (DS), (Dn) inputs to (SHCP), (STCP) inputs

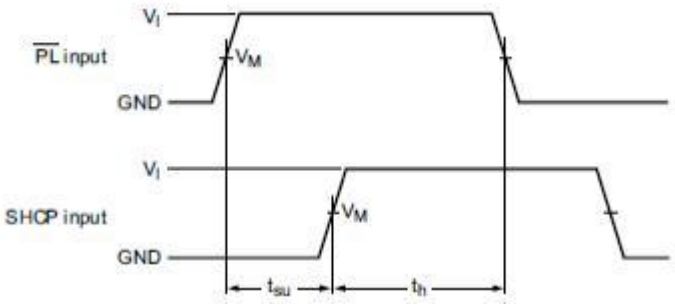


Figure 10 Set-up times for ($\overline{PL}$) input to (SHCP) input

Measurement Points

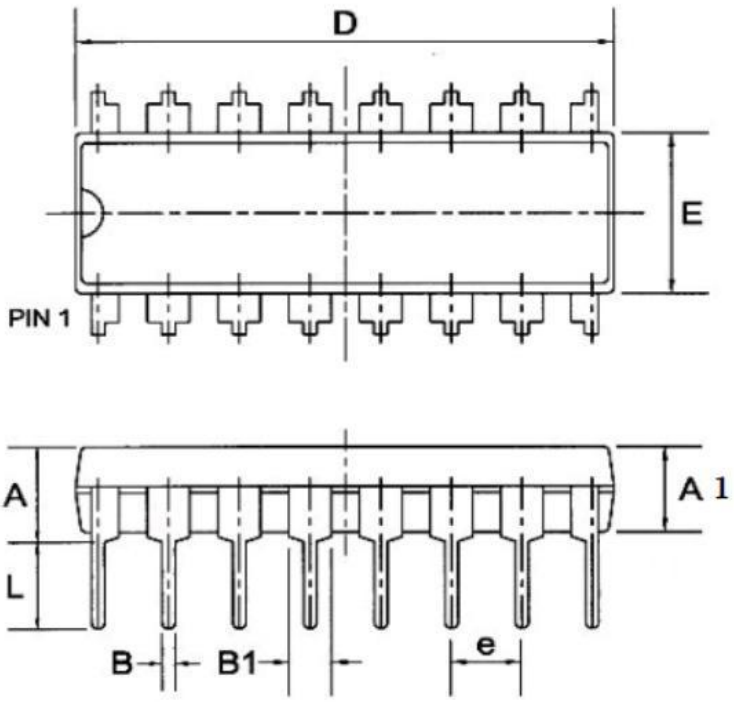
Type	Input	Output		
	V_M	V_M	V_X	V_Y
SN74HC597	0.5×V_{CC}	0.5×V_{CC}	0.1×V_{CC}	0.9×V_{CC}
SN74HCT597	1.3V	1.3V	0.1×V_{CC}	0.9×V_{CC}

Test Data

Type	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
SN74HC597	V_{CC}	3.0ns	15pF, 50pF	1KΩ	Open	V_{CC}	GND
SN74HCT597	3.0V	3.0ns	15pF, 50pF	1KΩ	Open	V_{CC}	GND

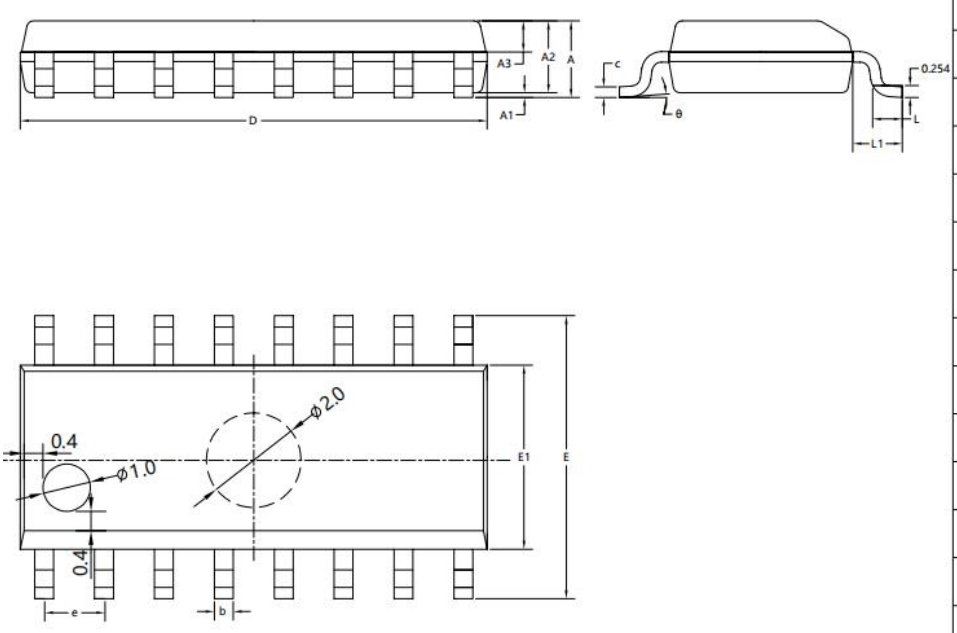
Package Information

DIP16



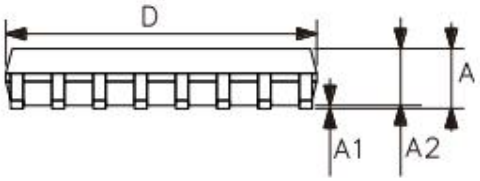
Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	--	4.31
A1	3.15	3.30	3.65
B	--	0.50	--
B1	--	1.6	--
C	--	0.27	--
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1	--	8.0	--
e	--	2.3	--
L	3.00	3.20	3.60

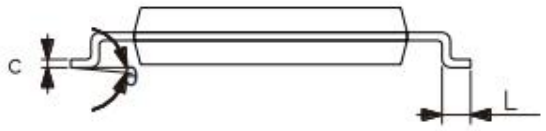
SOP16

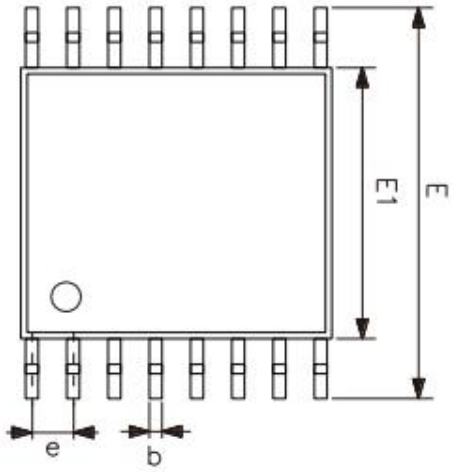


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

TSSOP16







Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

Statement：

✧ Shenzhen xinbole electronics co., ltd. reserves the right to change the product specifications, without notice! Before placing an order, the customer needs to confirm whether the information obtained is the latest version, and verify the integrity of the relevant information.

✧ Any semiconductor product is liable to fail or malfunction under certain conditions, and the buyer shall be responsible for complying with safety standards in the system design and whole machine manufacturing using Shenzhen xinbole electronics co., ltd products, and take appropriate security measures to avoid the potential risk of failure may result in personal injury or property losses of the situation occurred!

✧ This document is for referenceonly,and the actual use should be based on the application test results.

✧ Product performance is never ending, Shenzhen xinbole electronics co., ltd will be dedicated to provide customers with better performance, better quality of integrated circuit products.