

The CD14538 is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components,  $C_X$  and  $R_X$ . Output Pulse Width  $T = R_X \cdot C_X$  (secs)

$$R_X = \Omega$$

$$C_X = \text{Farads}$$

**Features**

- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10  $\mu$ s to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits

- Triggerable from Positive (A Input) or Negative-Going Edge (B-Input)
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-pin Compatible with CD14538
- Use the CD14538 for Pulse Widths Less Than 10  $\mu$ s with Supplies Up to 6 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

**MAXIMUM RATINGS** (Voltages Referenced to  $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Operating Temperature Range	-55 to +125	$^{\circ}$ C
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}$ C
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}$ C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

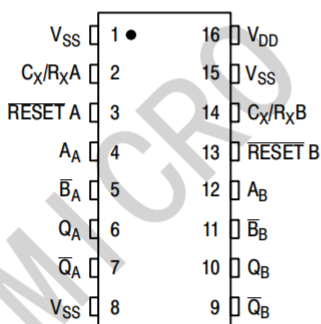
1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}$ C From 65 $^{\circ}$ C To 125 $^{\circ}$ C

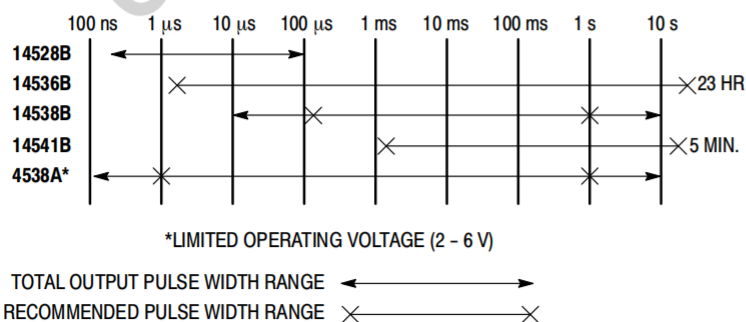
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

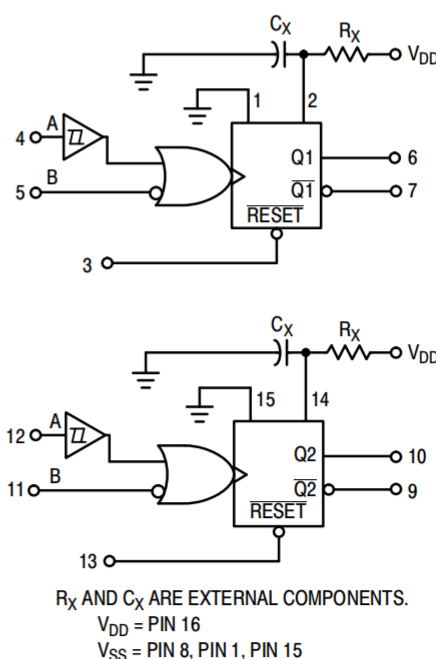
**PIN ASSIGNMENT**



**ONE-SHOT SELECTION GUIDE**



**BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level  $V_{OL}$	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
		15	-	0.05	-	0	0.05	-	0.05		
	"1" Level  $V_{OH}$	5.0	4.95	-	4.95	5.0	-	4.95	-		Vdc
		10	9.95	-	9.95	10	-	9.95	-		
		15	14.95	-	14.95	15	-	14.95	-		
Input Voltage ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)  ( $V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	"0" Level  $V_{IL}$	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
		15	-	4.0	-	6.75	4.0	-	4.0		
	"1" Level  $V_{IH}$	5.0	3.5	-	3.5	2.75	-	3.5	-		Vdc
		10	7.0	-	7.0	5.50	-	7.0	-		
		15	11	-	11	8.25	-	11	-		
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)  ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	Source  $I_{OH}$	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc	
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-		
		10	-1.6	-	-1.3	-2.25	-	-0.9	-		
		15	-4.2	-	-3.4	-8.8	-	-2.4	-		
	Sink  $I_{OL}$	5.0	0.64	-	0.51	0.88	-	0.36	-		mAdc
		10	1.6	-	1.3	2.25	-	0.9	-		
15	4.2	-	3.4	8.8	-	2.4	-	-			
Input Current, Pin 2 or 14	$I_{in}$	15	-	$\pm 0.05$	-	$\pm 0.00001$	$\pm 0.05$	-	$\pm 0.5$	$\mu$ Adc	
Input Current, Other Inputs	$I_{in}$	15	-	$\pm 0.1$	-	$\pm 0.00001$	$\pm 0.1$	-	$\pm 1.0$	$\mu$ Adc	
Input Capacitance, Pin 2 or 14	$C_{in}$	-	-	-	-	25	-	-	-	pF	
Input Capacitance, Other Inputs ( $V_{in} = 0$ )	$C_{in}$	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package) Q = Low, $\bar{Q}$ = High	$I_{DD}$	5.0	-	5.0	-	0.005	5.0	-	150	$\mu$ Adc	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Quiescent Current, Active State (Both) (Per Package) Q = High, $\bar{Q}$ = Low	$I_{DD}$	5.0	-	2.0	-	0.04	0.20	-	2.0	mAdc	
		10	-	2.0	-	0.08	0.45	-	2.0		
		15	-	2.0	-	0.13	0.70	-	2.0		
Total Supply Current at an external load capacitance ( $C_L$ ) and at external timing network ( $R_X, C_X$ ) (Note 3)	$I_T$	5.0	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$ $I_T = (8.0 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$ $I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$ where: $I_T$ in $\mu$ A (one monostable switching only), $C_X$ in $\mu$ F, $C_L$ in pF, $R_X$ in k ohms, and $f$ in Hz is the input frequency.							$\mu$ Adc	
		10									

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

**SWITCHING CHARACTERISTICS** (Note 4) ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ (Note 5)	Max	
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$	5.0 10 15	- - -	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{THL}$	5.0 10 15	- - -	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 255 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$ Reset to Q or $\bar{Q}$ $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 205 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15  5.0 10 15	- - -  - - -	300 150 100  250 125 95	600 300 220  500 250 190	ns   ns
Input Rise and Fall Times Reset  B Input  A Input	$t_r, t_f$	5 10 15  5 10 15  5 10 15	- - -  - - -  -	- - -  300 1.2 0.4  No Limit	15 5 4  1.0 0.1 0.05  -	$\mu\text{s}$  ms  -
Input Pulse Width A, B, or Reset	$t_{WH},$ $t_{WL}$	5.0 10 15	170 90 80	85 45 40	- - -	ns
Retrigger Time	$t_{rr}$	5.0 10 15	0 0 0	- - -	- - -	ns
Output Pulse Width — Q or $\bar{Q}$ Refer to Figures 8 and 9 $C_X = 0.002 \mu\text{F}, R_X = 100 \text{ k}\Omega$  $C_X = 0.1 \mu\text{F}, R_X = 100 \text{ k}\Omega$  $C_X = 10 \mu\text{F}, R_X = 100 \text{ k}\Omega$	T	5.0 10 15  5.0 10 15  5.0 10 15	198 200 202  9.3 9.4 9.5  0.91 0.92 0.93	210 212 214  9.86 10 10.14  0.965 0.98 0.99	230 232 234  10.5 10.6 10.7  1.03 1.04 1.06	$\mu\text{s}$  ms  s
Pulse Width Match between circuits in the same package. $C_X = 0.1 \mu\text{F}, R_X = 100 \text{ k}\Omega$	100 $[(T_1 - T_2)/T_1]$	5.0 10 15	- - -	$\pm 1.0$ $\pm 1.0$ $\pm 1.0$	$\pm 5.0$ $\pm 5.0$ $\pm 5.0$	%

 4. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

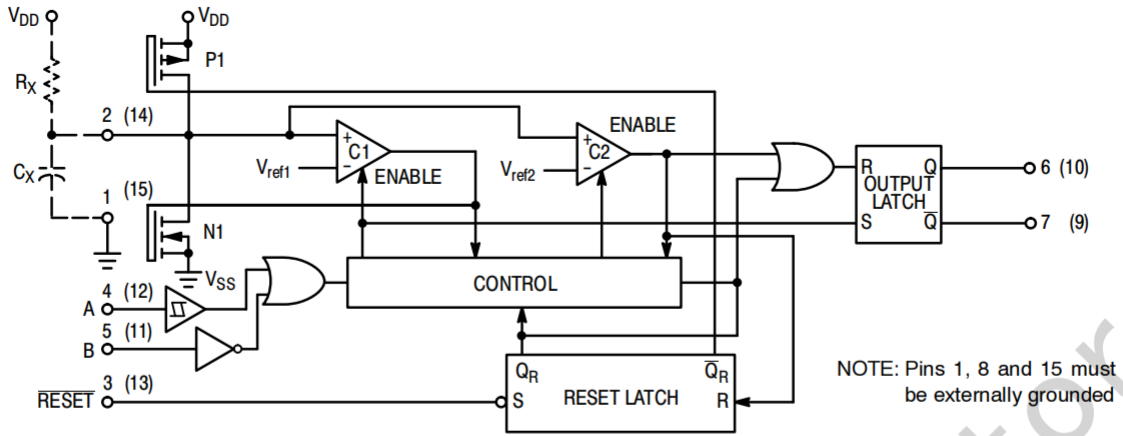
5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**OPERATING CONDITIONS**

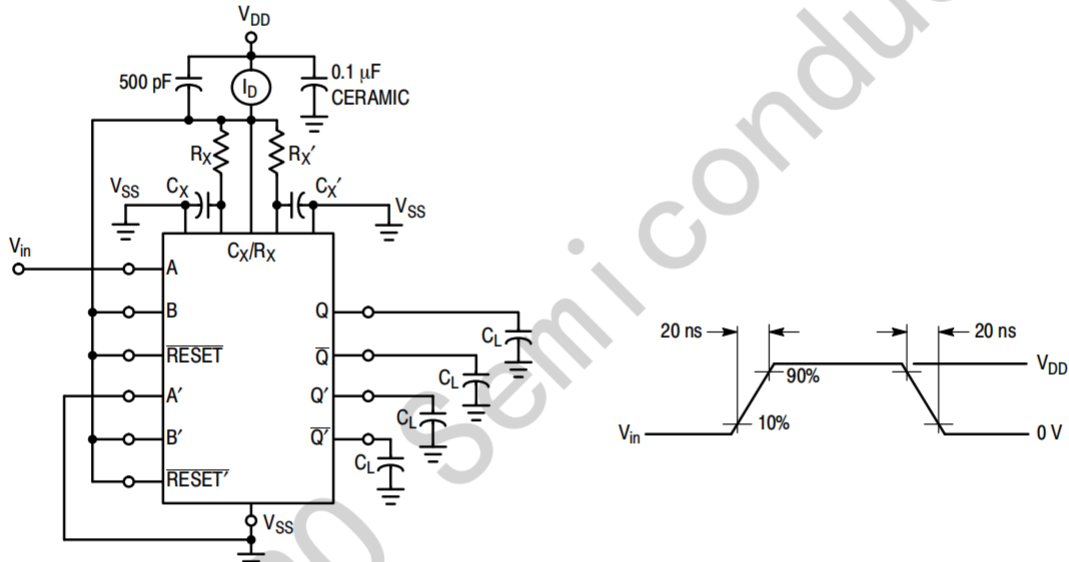
External Timing Resistance	$R_X$	-	5.0	-	(Note 6)	$\text{k}\Omega$
External Timing Capacitance	$C_X$	-	0	-	No Limit (Note 7)	$\mu\text{F}$

 6. The maximum usable resistance  $R_X$  is a function of the leakage of the capacitor  $C_X$ , leakage of the CD14538, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for  $R_X > 1 \text{ M}\Omega$ .

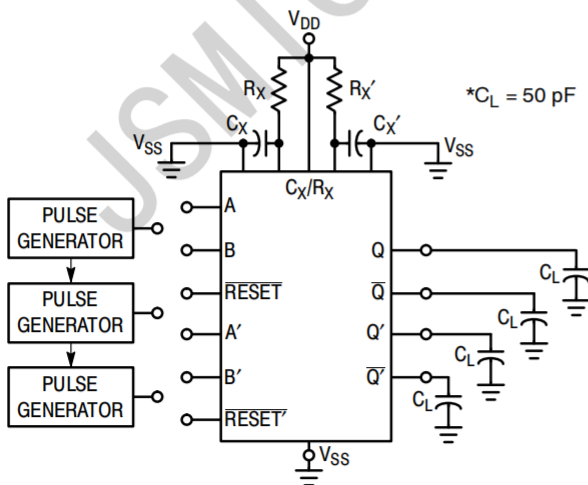
 7. If  $C_X > 15 \mu\text{F}$ , use discharge protection diode per Fig. 11.



**Figure 1. Logic Diagram  
(1/2 of Device Shown)**



**Figure 2. Power Dissipation Test Circuit and Waveforms**



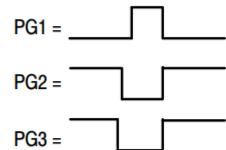
**Figure 3. Switching Test Circuit**

**INPUT CONNECTIONS**

Characteristics	Reset	A	B
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ , $T$ , $t_{WH}$ , $t_{WL}$	$V_{DD}$	PG1	$V_{DD}$
$t_{PLH}$ , $t_{PHL}$ , $t_{TLH}$ , $t_{THL}$ , $T$ , $t_{WH}$ , $t_{WL}$	$V_{DD}$	$V_{SS}$	PG2
$t_{PLH(R)}$ , $t_{PHL(R)}$ , $t_{WH}$ , $t_{WL}$	PG3	PG1	PG2

\*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 4.



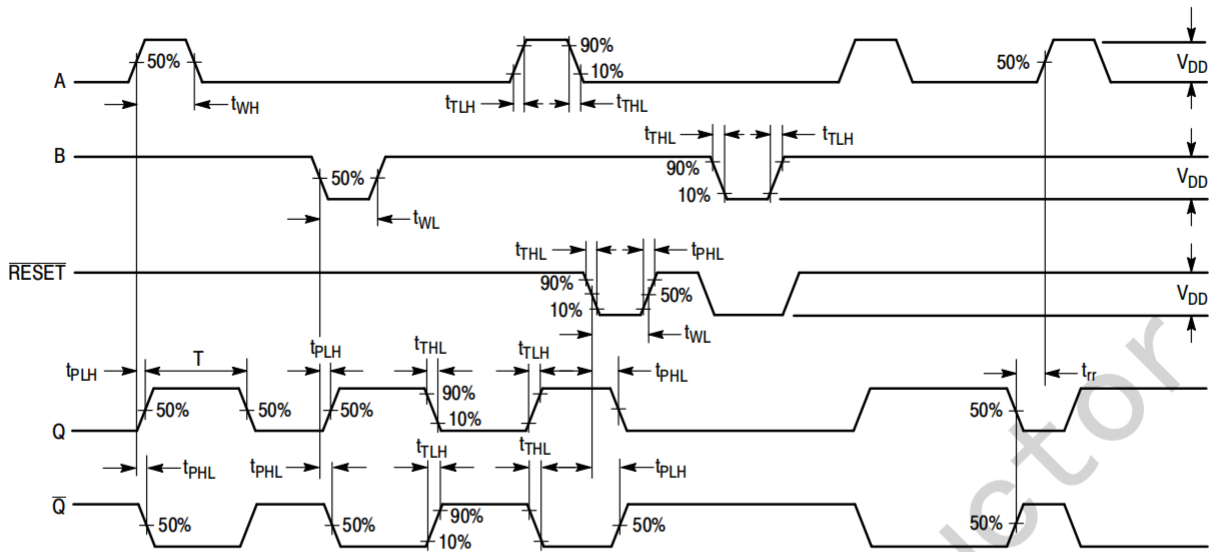


Figure 4. Switching Test Waveforms

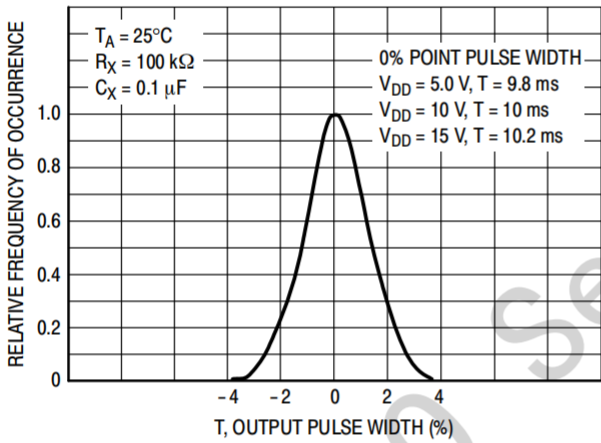


Figure 5. Typical Normalized Distribution of Units for Output Pulse Width

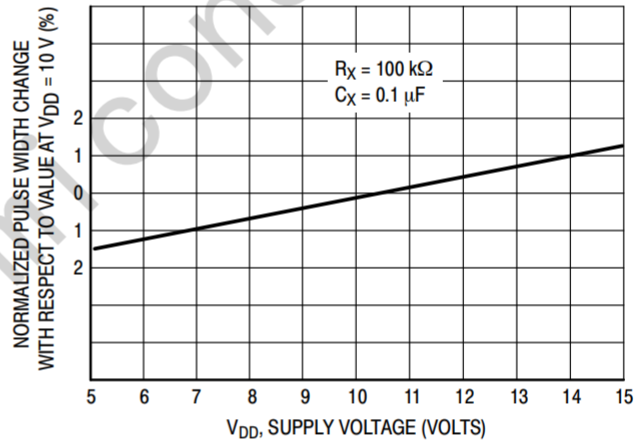


Figure 6. Typical Pulse Width Variation as a Function of Supply Voltage  $V_{DD}$

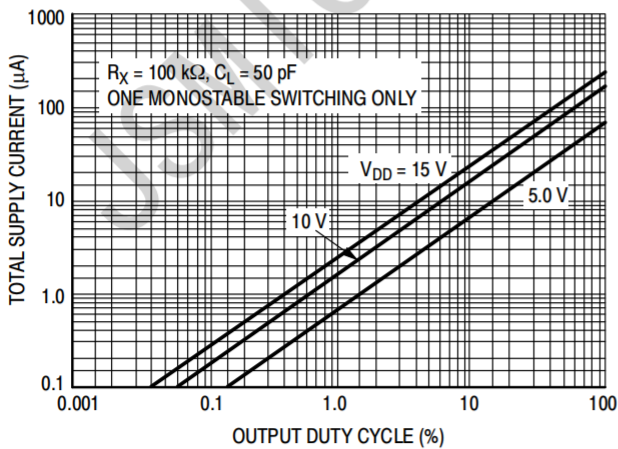
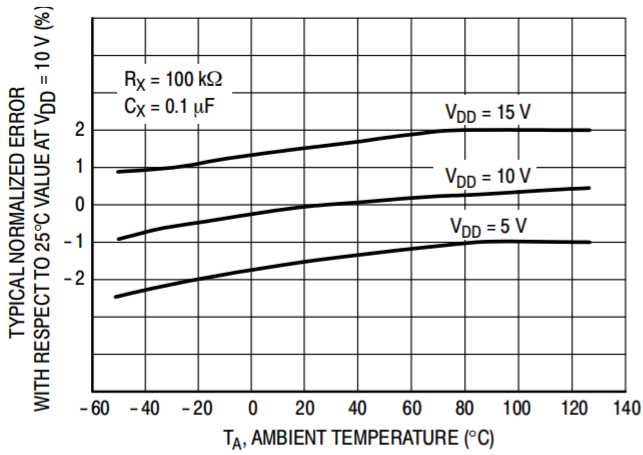


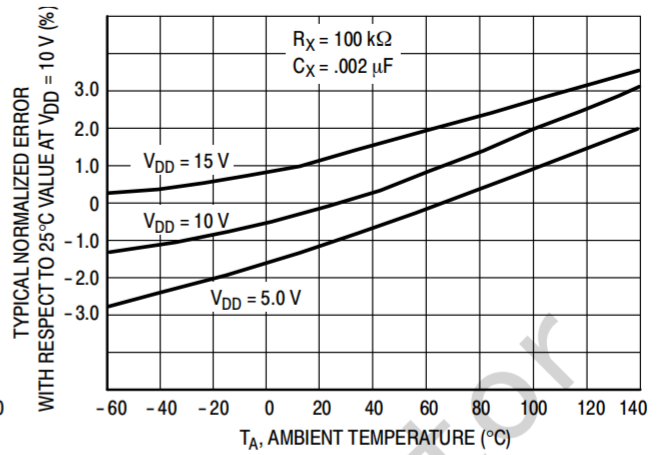
Figure 7. Typical Total Supply Current versus Output Duty Cycle

FUNCTION TABLE

Inputs		Outputs	
Reset	A	B	Q Q̄
H		H	
H	L		
H		L	Not Triggered
H	H		Not Triggered
H	L, H,	H	Not Triggered
H	L	L, H,	Not Triggered
L	X	X	L H
	X	X	Not Triggered

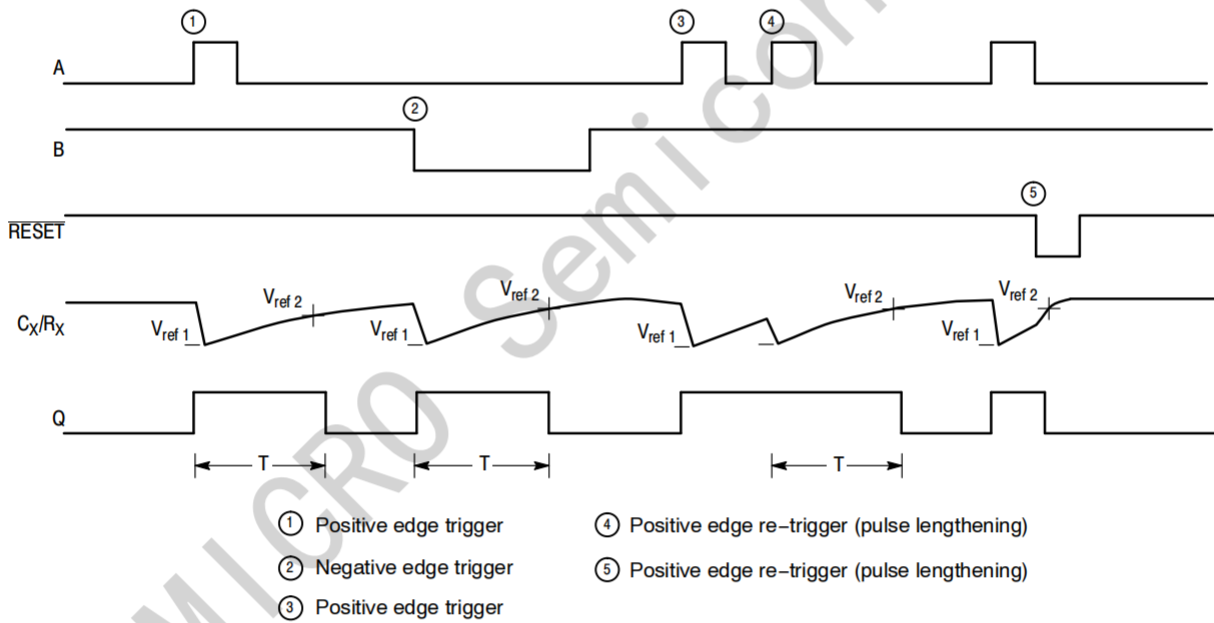


**Figure 8. Typical Error of Pulse Width Equation versus Temperature**



**Figure 9. Typical Error of Pulse Width Equation versus Temperature**

**THEORY OF OPERATION**



**Figure 10. Timing Operation**

### TRIGGER OPERATION

The block diagram of the CD14538 is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor  $C_X$  completely charged to  $V_{DD}$ . When the trigger input A goes from  $V_{SS}$  to  $V_{DD}$  (while inputs B and Reset are held to  $V_{DD}$ ) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor  $C_X$  rapidly discharges toward  $V_{SS}$  until  $V_{ref1}$  is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor  $C_X$  begins to charge through the timing resistor,  $R_X$ , toward  $V_{DD}$ . When the voltage across  $C_X$  equals  $V_{ref2}$ , comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 ②. This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state,  $C_X$  is fully charged to  $V_{DD}$  causing the current through resistor  $R_X$  to be zero. Both comparators are “off” with total device current due only to reverse junction leakages. An added feature of the CD14538 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of  $C_X$ ,  $R_X$ , or the duty cycle of the input waveform.

### RETRIGGER OPERATION

The CD14538 is retriggered if a valid trigger occurs ③ followed by another valid trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from  $V_{ref1}$ , but has not yet reached  $V_{ref2}$ , will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at  $C_X/R_X$  will again drop to  $V_{ref1}$  before progressing along the RC charging curve toward  $V_{DD}$ . The Q output will remain high until time T, after the last valid retrigger.

### RESET OPERATION

The CD14538 may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse

on  $\overline{\text{Reset}}$  sets the reset latch and causes the capacitor to be fast charged to  $V_{DD}$  by turning on transistor P1 ⑤. When the voltage on the capacitor reaches  $V_{ref2}$ , the reset latch will clear, and will then be ready to accept another pulse. If the  $\overline{\text{Reset}}$  input is held low, any trigger inputs that occur will be inhibited and the Q and  $\overline{Q}$  outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the  $\overline{\text{Reset}}$  input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

### POWER-DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the CD14538 is powered down, the capacitor voltage may discharge from  $V_{DD}$  through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the  $V_{DD}$  supply must not be faster than  $(V_{DD}) \cdot (C)/(10 \text{ mA})$ . For example, if  $V_{DD} = 10 \text{ V}$  and  $C_X = 10 \mu\text{F}$ , the  $V_{DD}$  supply should discharge no faster than  $(10 \text{ V}) \times (10 \mu\text{F})/(10 \text{ mA}) = 10 \text{ ms}$ . This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of  $V_{DD}$  to zero volts occurs, the CD14538 can sustain damage. To avoid this possibility use an external clamping diode,  $D_X$ , connected as shown in Fig. 11.

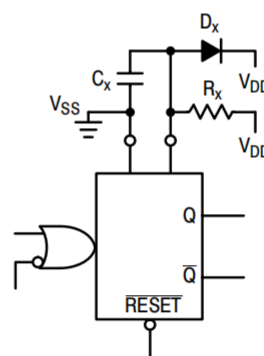
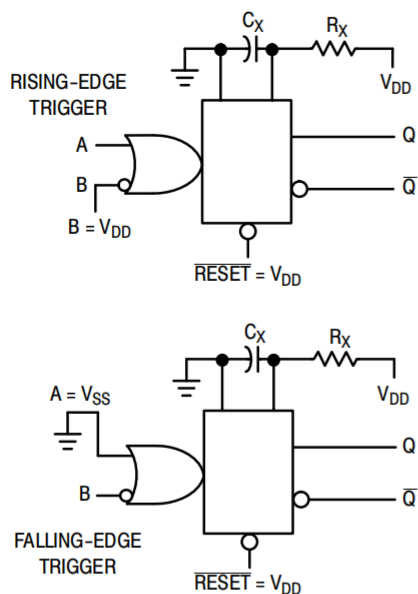
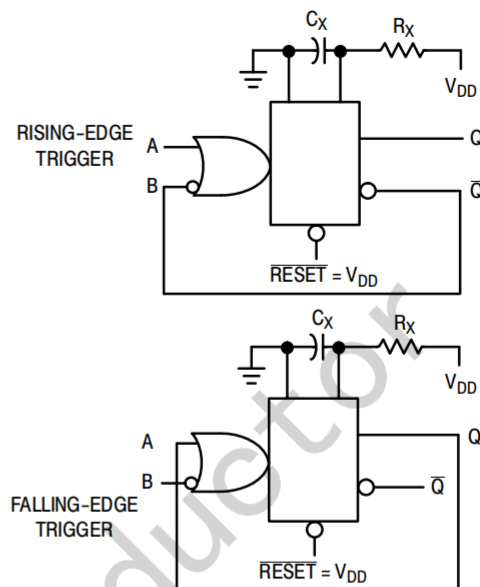


Figure 11. Use of a Diode to Limit Power Down Current Surge

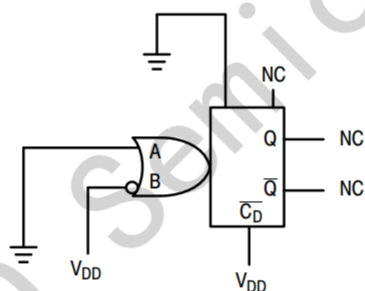
TYPICAL APPLICATIONS



**Figure 12. Retriggerable Monostables Circuitry**



**Figure 13. Non-Retriggerable Monostables Circuitry**

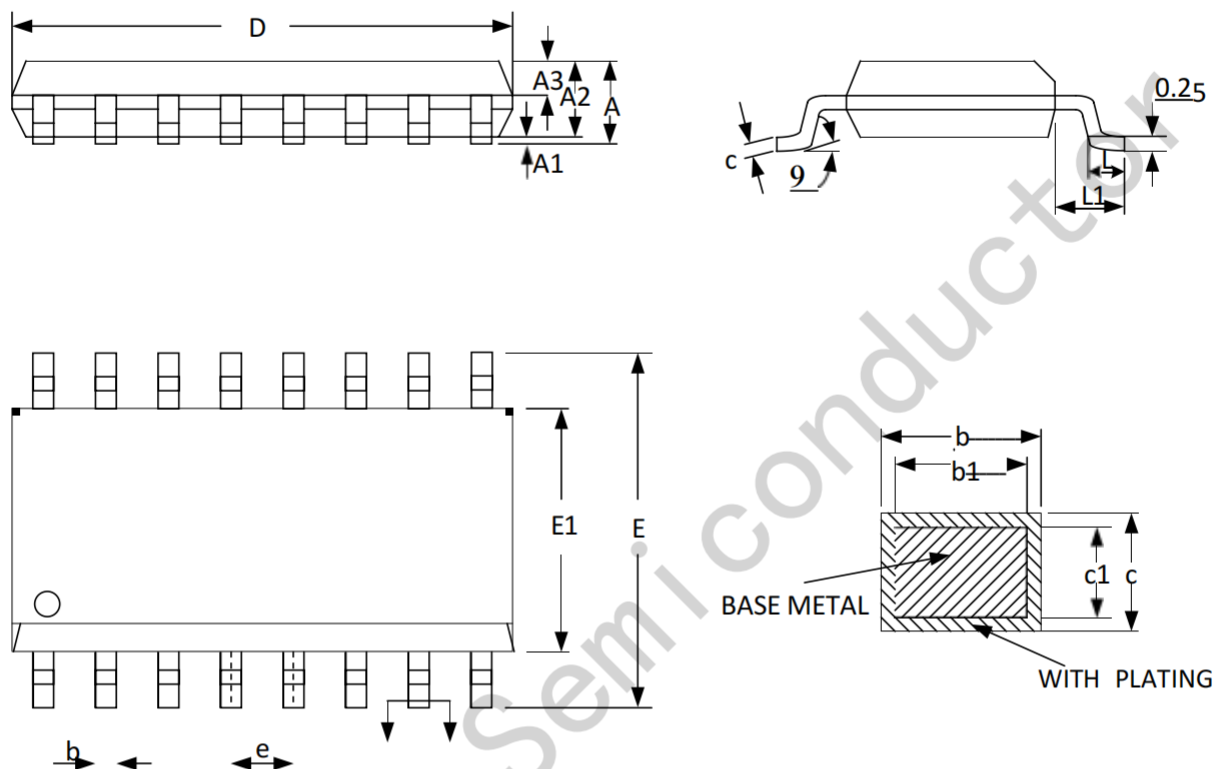


**Figure 14. Connection of Unused Sections**



## Package Information

SOP-16



SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	-	0.48
b1	0.38	0.41	0.43
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.5	0.65	0.80
L1	1.05BSC		
9	0°	-	8°