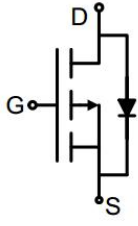
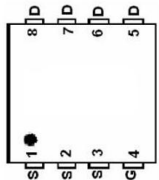
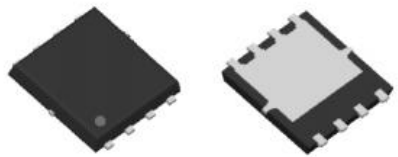


## P-Channel Enhancement Mode Power MOSFET

<p><b>Description</b></p> <p>The GT750P10D5 uses advanced trench technology to provide excellent <math>R_{DS(ON)}</math>, low gate charge. It can be used in a wide variety of applications.</p> <p><b>General Features</b></p> <ul style="list-style-type: none"> <li>● <math>V_{DS}</math> -100V</li> <li>● <math>I_D</math> (at <math>V_{GS} = -10V</math>) -24A</li> <li>● <math>R_{DS(ON)}</math> (at <math>V_{GS} = -10V</math>) &lt; 60m<math>\Omega</math></li> <li>● <math>R_{DS(ON)}</math> (at <math>V_{GS} = -4.5V</math>) &lt; 75m<math>\Omega</math></li> <li>● 100% Avalanche Tested</li> <li>● RoHS Compliant</li> </ul> <p><b>Application</b></p> <ul style="list-style-type: none"> <li>● Power switch</li> <li>● DC/DC converters</li> </ul>	 <p>Schematic diagram</p>  <p>pin assignment</p>  <p>DFN5X6-8L</p>
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### Ordering Information

Device	Package	Marking	Packaging
GT750P10D5	DFN5X6-8L	GT750P10	5000pcs/Reel

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-100	V
Continuous Drain Current	$I_D$	-24	A
Pulsed Drain Current (note1)	$I_{DM}$	-96	A
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation	$P_D$	79	W
Single pulse avalanche energy (note2)	$E_{AS}$	272	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 To 150	$^\circ\text{C}$

### Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{thJC}$	1.58	$^\circ\text{C/W}$

Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static Parameters</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-100	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100V, V_{GS} = 0V$	--	--	-1	$\mu A$
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.8	-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -10A$	--	50	60	m $\Omega$
		$V_{GS} = -4.5V, I_D = -10A$	--	62	75	
Forward Transconductance	$g_{FS}$	$V_{DS} = -5V, I_D = -10A$	--	22	--	S
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = -50V,$ $f = 1.0MHz$	--	1930	--	pF
Output Capacitance	$C_{oss}$		--	154	--	
Reverse Transfer Capacitance	$C_{rss}$		--	20	--	
Total Gate Charge	$Q_g$	$V_{DD} = -50V,$ $I_D = -10A,$ $V_{GS} = -10V$	--	40	--	nC
Gate-Source Charge	$Q_{gs}$		--	7.8	--	
Gate-Drain Charge	$Q_{gd}$		--	8.6	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -50V,$ $I_D = -10A,$ $R_G = 6\Omega$	--	13	--	ns
Turn-on Rise Time	$t_r$		--	39	--	
Turn-off Delay Time	$t_{d(off)}$		--	100	--	
Turn-off Fall Time	$t_f$		--	105	--	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	-24	A
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = -10A, V_{GS} = 0V$	--	--	-1.2	V
Reverse Recovery Charge	$Q_{rr}$	$I_F = -10A, V_{GS} = 0V$ $di/dt = -100A/\mu s$	--	280	--	nC
Reverse Recovery Time	$T_{rr}$		--	104	--	ns

### Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition :  $T_J = 25^\circ\text{C}, V_{DD} = -50V, V_{GS} = -10V, L = 0.5mH, R_G = 25\Omega$
3. Identical low side and high side switch with identical  $R_G$

### Gate Charge Test Circuit



### Switch Time Test Circuit

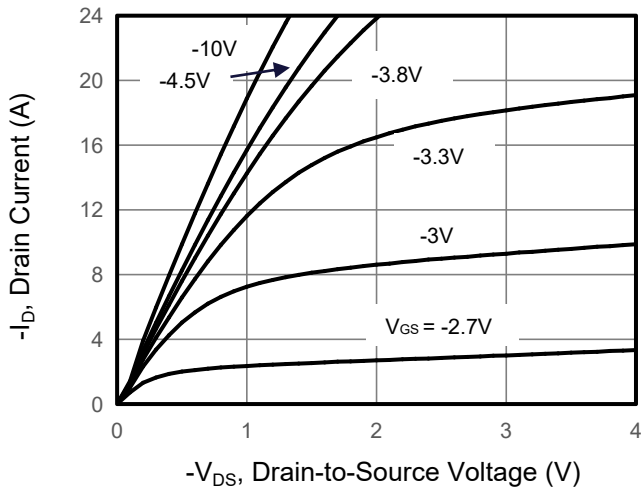


### EAS Test Circuit

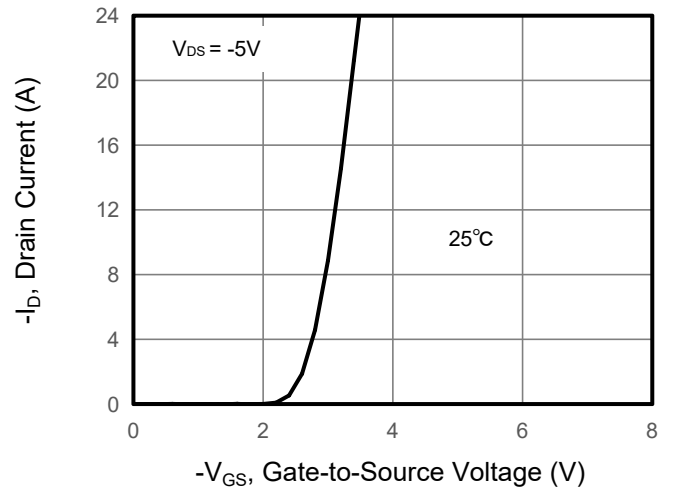


Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

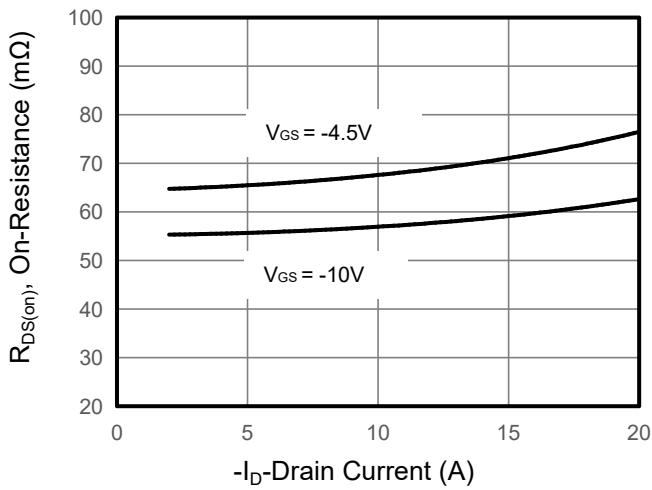
**Figure 1. Output Characteristics**



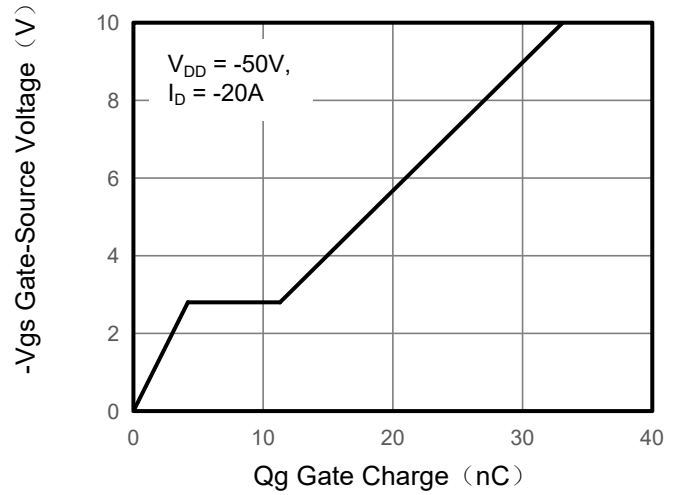
**Figure 2. Transfer Characteristics**



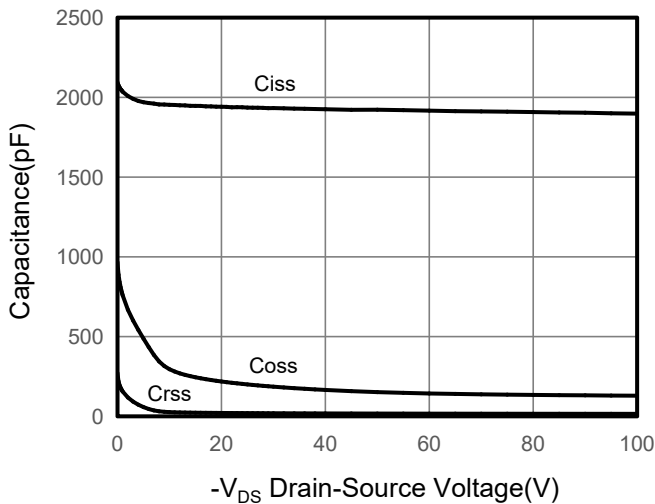
**Figure 3. Drain Source On Resistance**



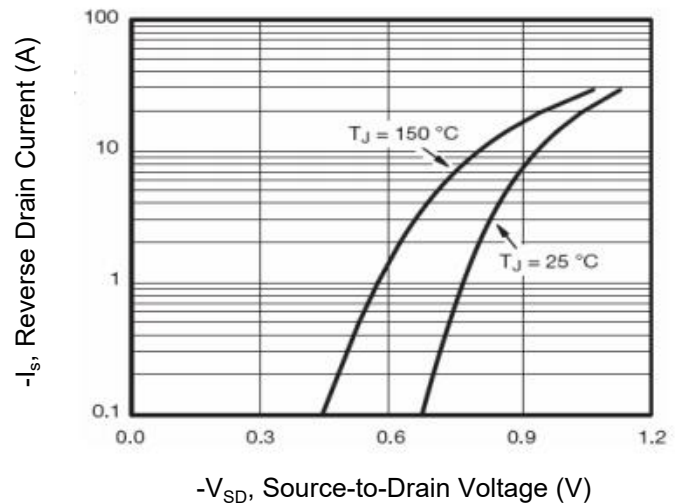
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Source-Drain Diode Forward**



Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 7. Drain-Source On-Resistance

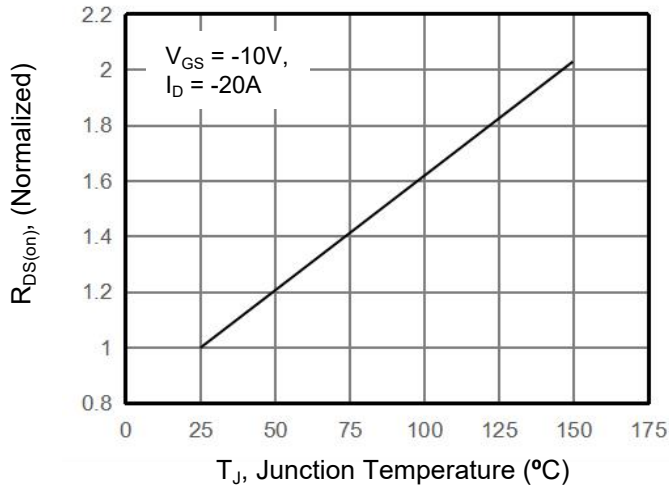


Figure 10. Safe Operation Area

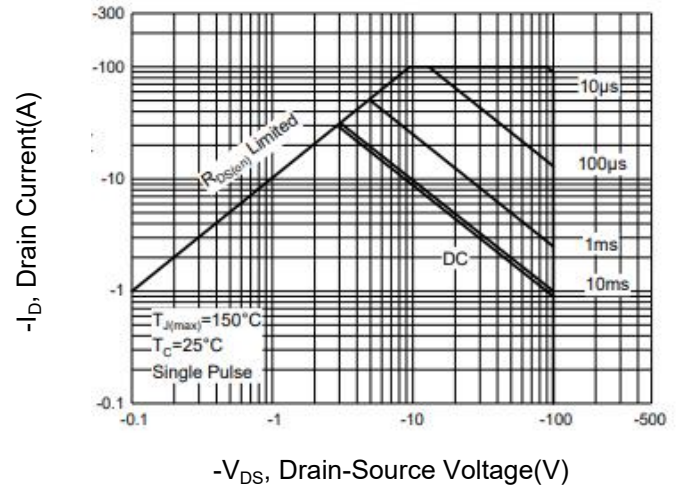
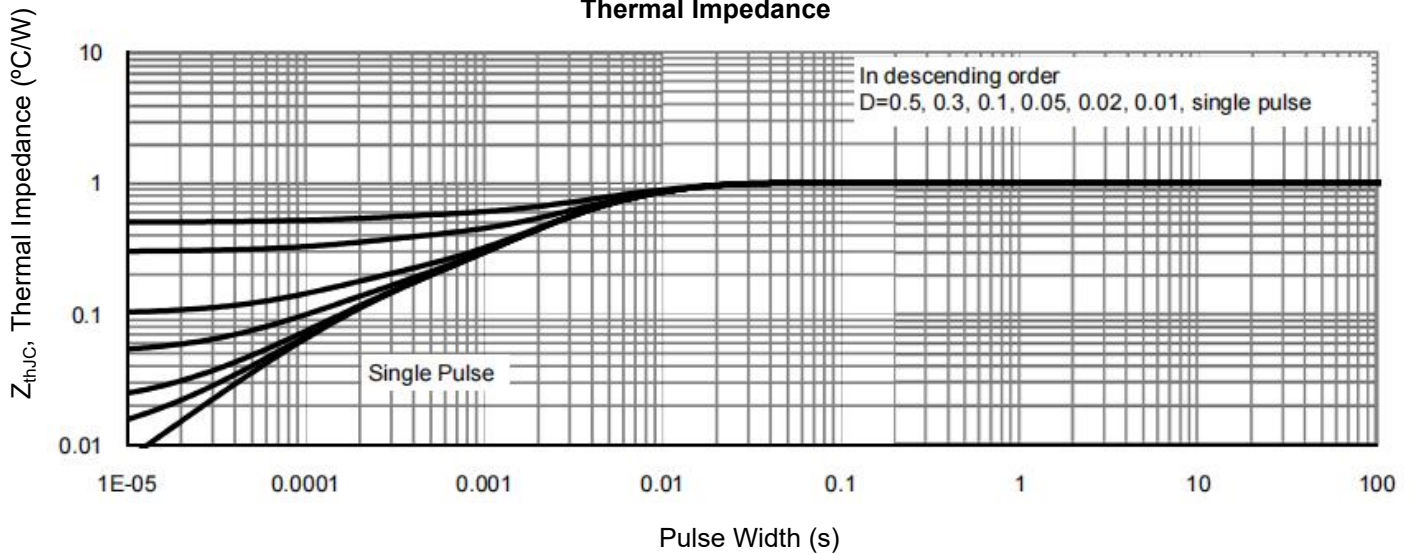
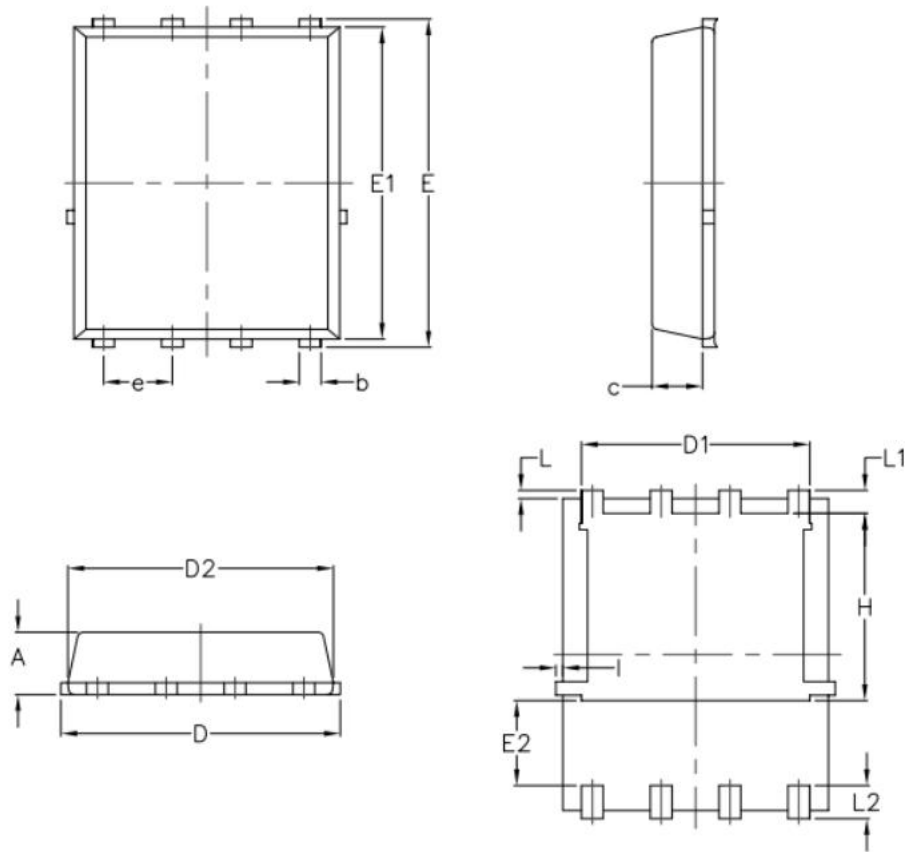


Figure 9. Normalized Maximum Transient Thermal Impedance



## DFN5X6-8L Package Information



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
⚠ D	4.80	5.40	0.1890	0.2126
⚠ D1	4.11	4.31	0.1618	0.1697
⚠ D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
⚠ E2	1.40	—	0.0551	—
e	1.27 BSC		0.05 BSC	
⚠ L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
⚠ L2	0.38	0.71	0.0150	0.0280
⚠ H	3.30	3.50	0.1299	0.1378
I	—	0.18	—	0.0070