N and P Channel Enhancement Mode Power MOSFET

Description

The G300C03L6 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

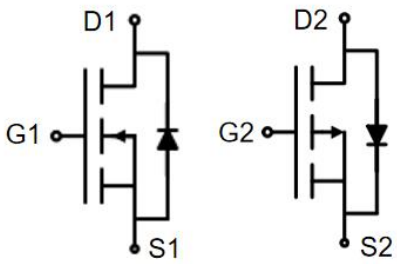
General Features

- NMOS
- V_{DS} 30V
- I_D (at V_{GS} = 10V) 5.6A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 27mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 30mΩ
- $R_{DS(ON)}$ (at V_{GS} = 2.5V) < 65mΩ
- 100% Avalanche Tested
- RoHS Compliant

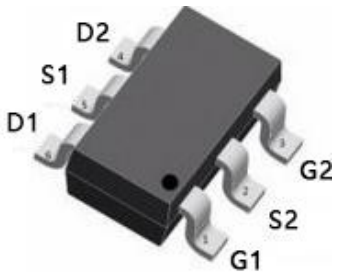
- PMOS
- V_{DS} -30V
- I_D (at V_{GS} = -10V) -4.2A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 55mΩ
- $R_{DS(ON)}$ (at V_{GS} = -4.5V) < 65mΩ
- $R_{DS(ON)}$ (at V_{GS} = -2.5V) < 90mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



SOT-23-6L Dual

Ordering Information

Device	Package	Marking	Packaging
G300C03L6	SOT-23-6L Dual	G300C03	3000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Continuous Drain Current	I_D	5.6	-4.2	A
Pulsed Drain Current (note1)	I_{DM}	22.4	-16.8	A
Gate-Source Voltage	V_{GS}	±12	±12	V
Power Dissipation	P_D	1.4	1.2	W
Single pulse avalanche energy （note2）	E_{AS}	10	14	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	ºC

Thermal Resistance

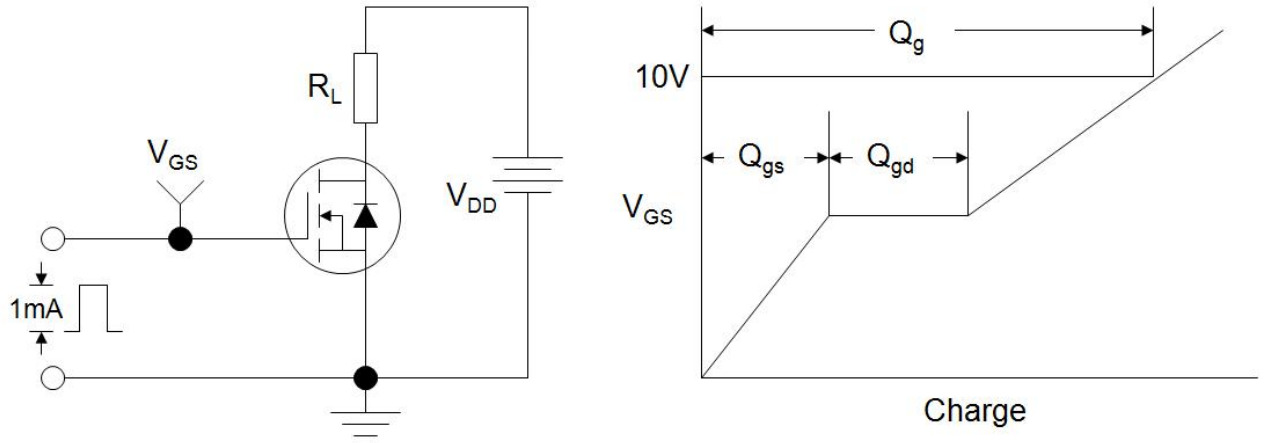
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	89	104	ºC/W

NMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±12V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.7	1.0	1.3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 3A	--	22	27	mΩ
		V_{GS} = 4.5V, I_D = 3A	--	25	30	
		V_{GS} = 2.5V, I_D = 2A	--	38	65	
Forward Transconductance	g_{FS}	V_{GS} = 5V, I_D = 3A	--	10	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz	--	547	--	pF
Output Capacitance	C_{oss}		--	69	--	
Reverse Transfer Capacitance	C_{rss}		--	57	--	
Total Gate Charge	Q_g	V_{DD} = 15V, I_D = 3A, V_{GS} = 10V	--	16	--	nC
Gate-Source Charge	Q_{gs}		--	2	--	
Gate-Drain Charge	Q_{gd}		--	1.8	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15V, I_D = 3A, R_G = 3Ω	--	4	--	ns
Turn-on Rise Time	t_r		--	26	--	
Turn-off Delay Time	$t_{d(off)}$		--	15	--	
Turn-off Fall Time	t_f		--	24	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	5.6	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} =3A, V_{GS} = 0V	--	--	1.2	V
Reverse Recovery Charge	Qrr	I_F = 3A, V_{GS} = 0V di/dt=100A/us	--	1	--	nC
Reverse Recovery Time	T_{rr}		--	12	--	ns

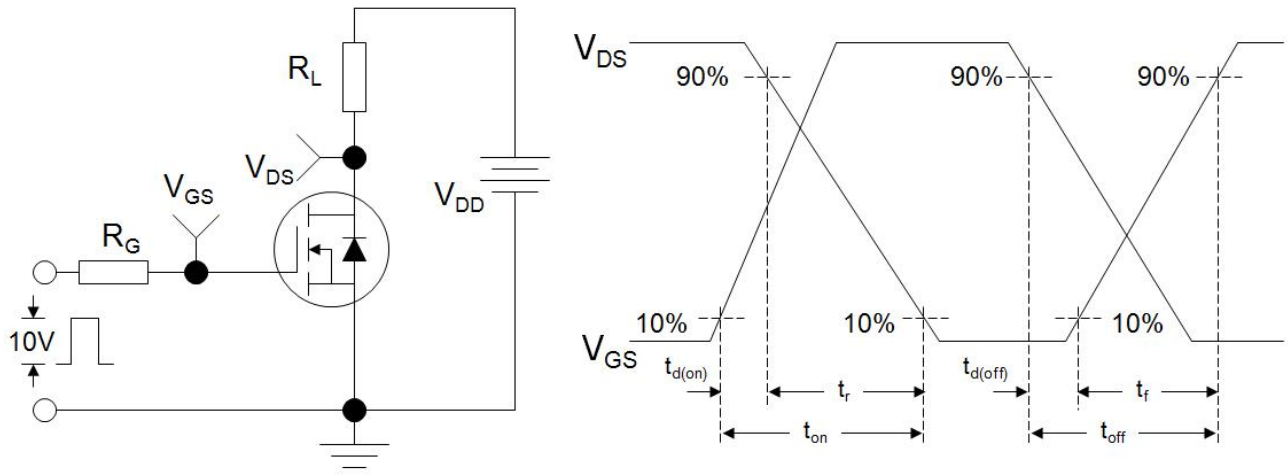
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=30V,VGS=10V,L=0.5mH,Rg=25Ω
   The table shows the minimum avalanche energy, which is 25mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

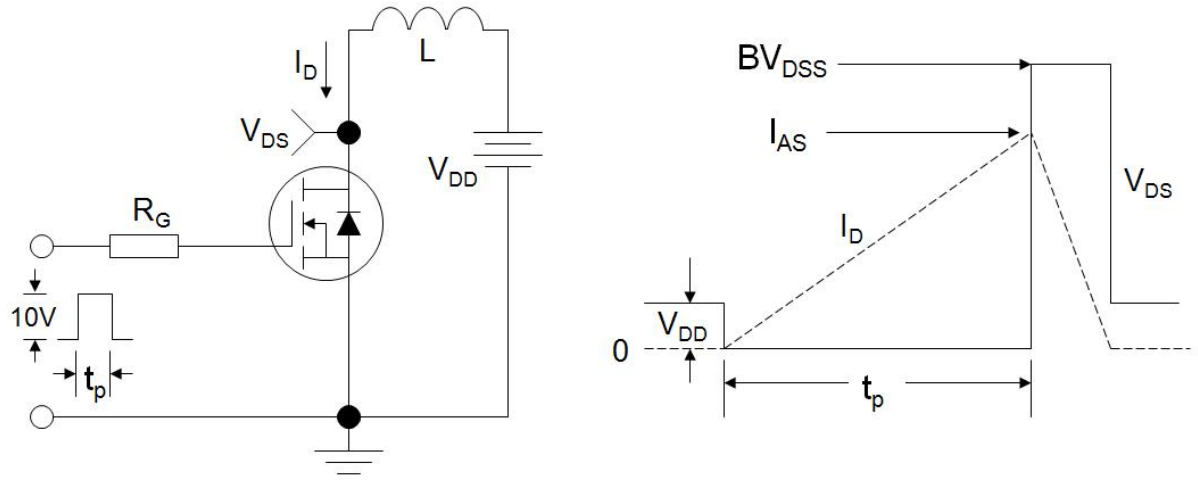
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

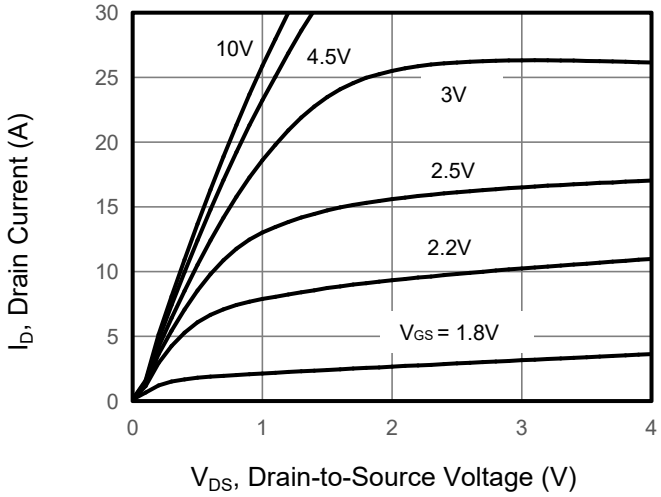


Figure 2. Transfer Characteristics

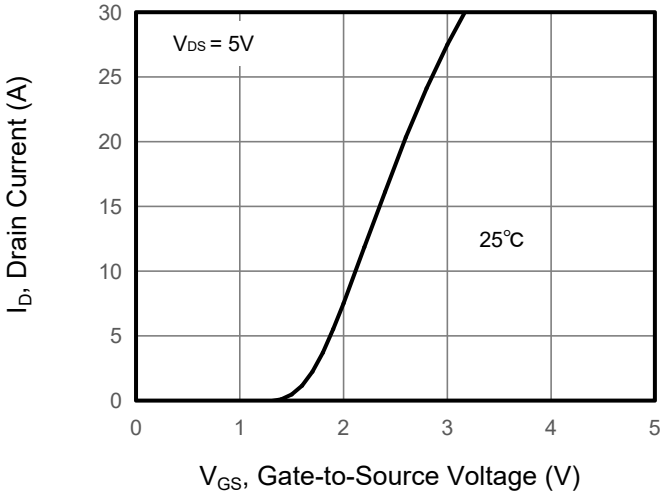


Figure 3. Drain Source On Resistance

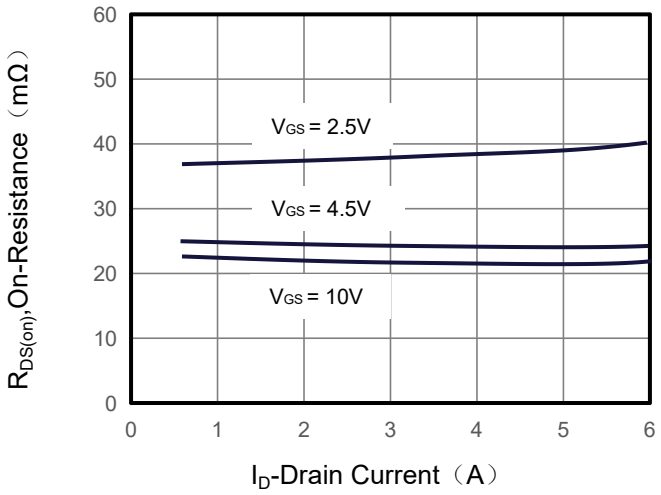


Figure 4. Gate Charge

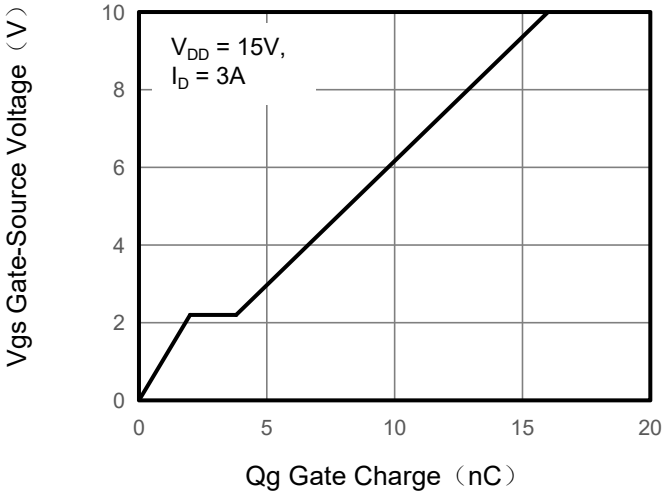


Figure 5. Capacitance

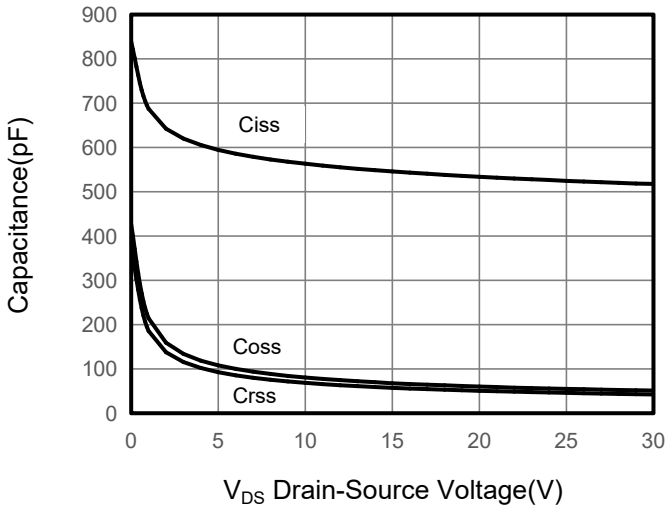
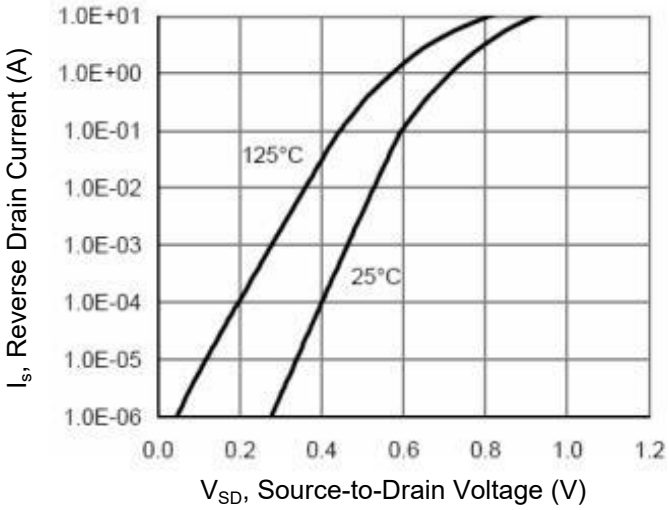


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

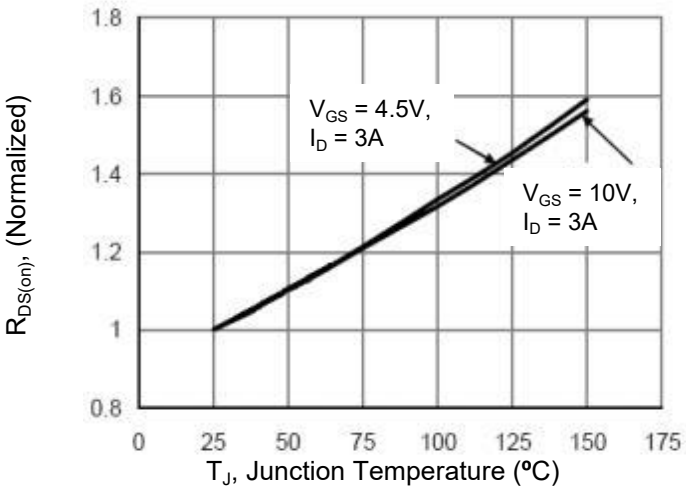


Figure 8. Safe Operation Area

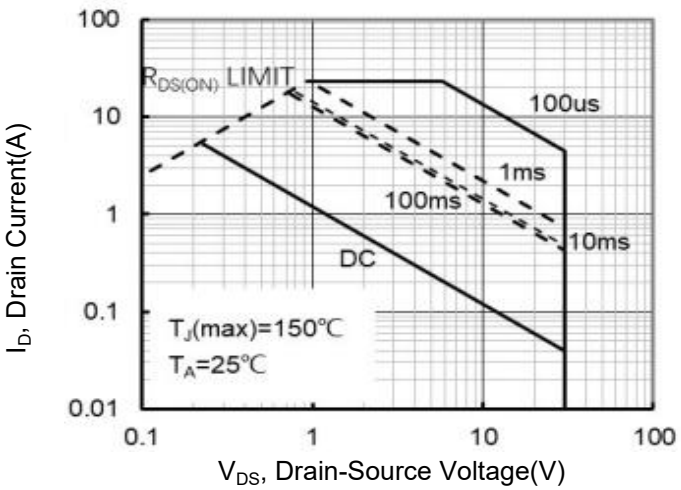
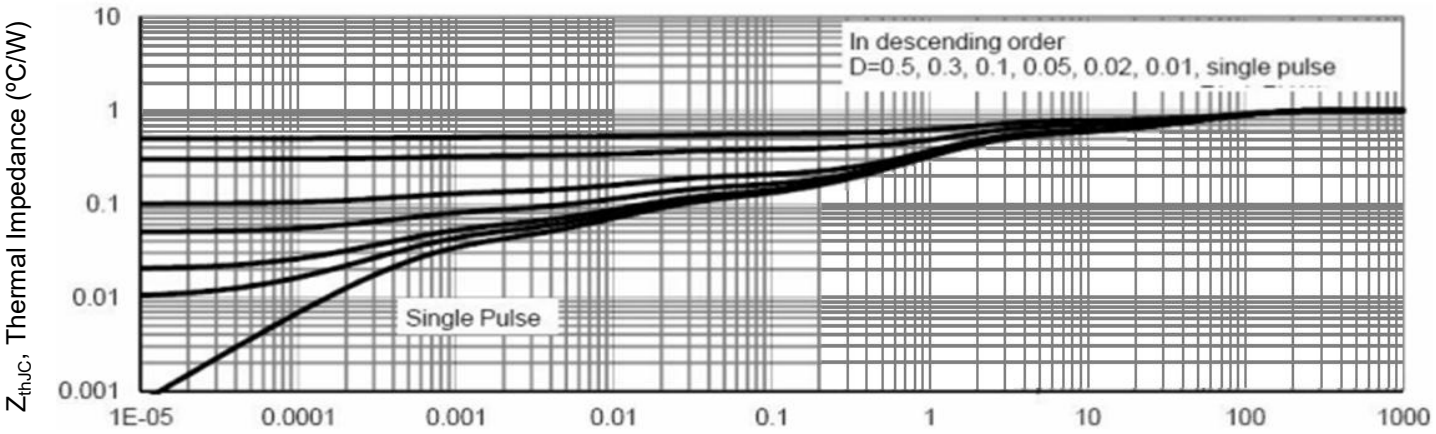


Figure 9. Normalized Maximum Transient Thermal Impedance

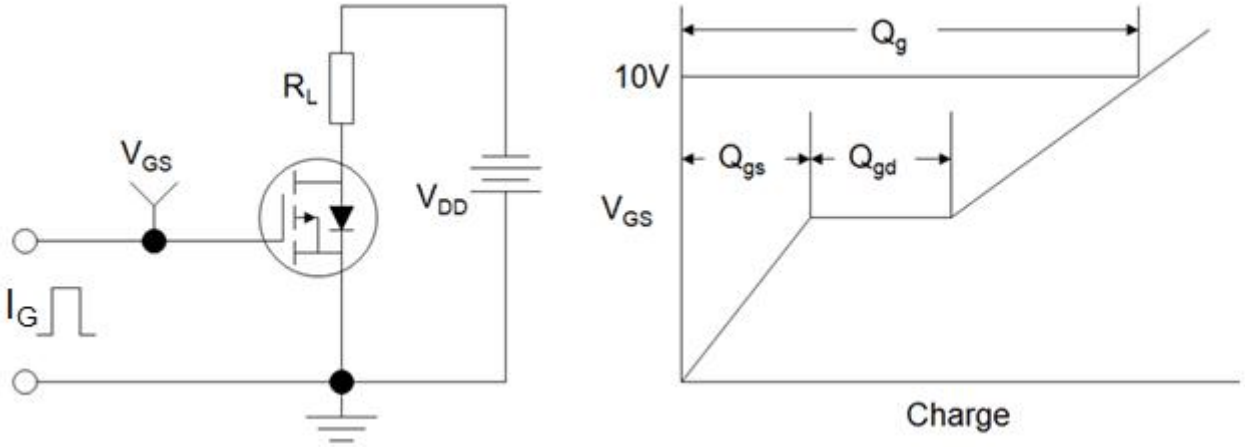


PMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±12V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.6	-0.8	-1.3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -3A	--	43	55	mΩ
		V_{GS} = -4.5V, I_D = -3A	--	51	65	
		V_{GS} = -2.5V, I_D = -2A	--	68	90	
Forward Transconductance	g_{FS}	V_{DS} = -5V,I_D = -3A	--	10	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz	--	693	--	pF
Output Capacitance	C_{oss}		--	79	--	
Reverse Transfer Capacitance	C_{rss}		--	68	--	
Total Gate Charge	Q_g	V_{DD} = -15V, I_D = -4A, V_{GS} = -4.5V	--	8.5	--	nC
Gate-Source Charge	Q_{gs}		--	1.8	--	
Gate-Drain Charge	Q_{gd}		--	2.7	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -15V, I_D = -4A, R_G = 6Ω	--	7	--	ns
Turn-on Rise Time	t_r		--	3	--	
Turn-off Delay Time	$t_{d(off)}$		--	30	--	
Turn-off Fall Time	t_f		--	12	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-4.2	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -4A, V_{GS} = 0V	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	I_F = -4A, V_{GS} = 0V di/dt=-100A/us	--	8	--	nC
Reverse Recovery Time	T_{rr}		--	14	--	ns

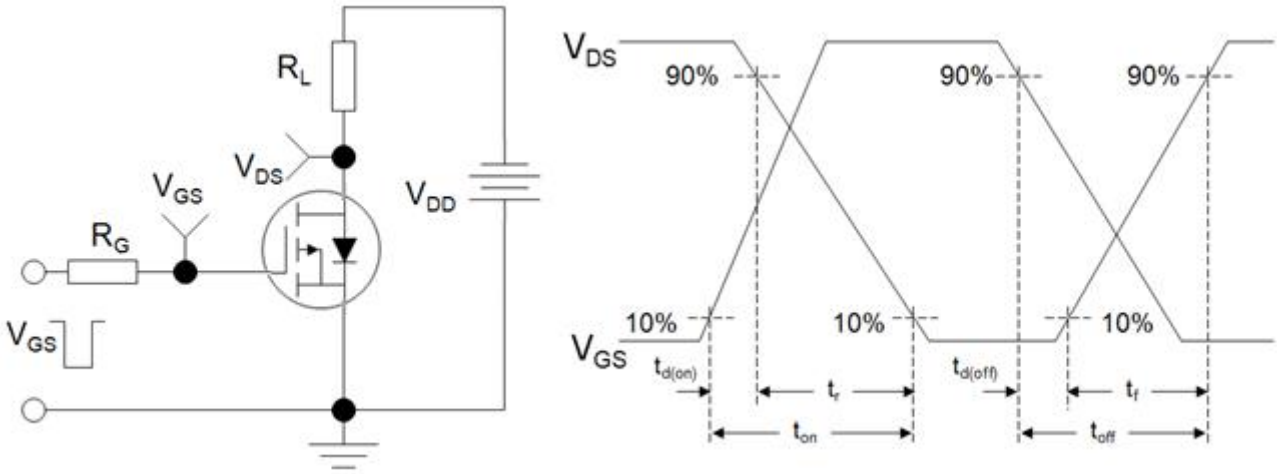
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=-30V,VGS=-10V,L=0.5mH,Rg=25Ω
   The table shows the minimum avalanche energy, which is 36mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

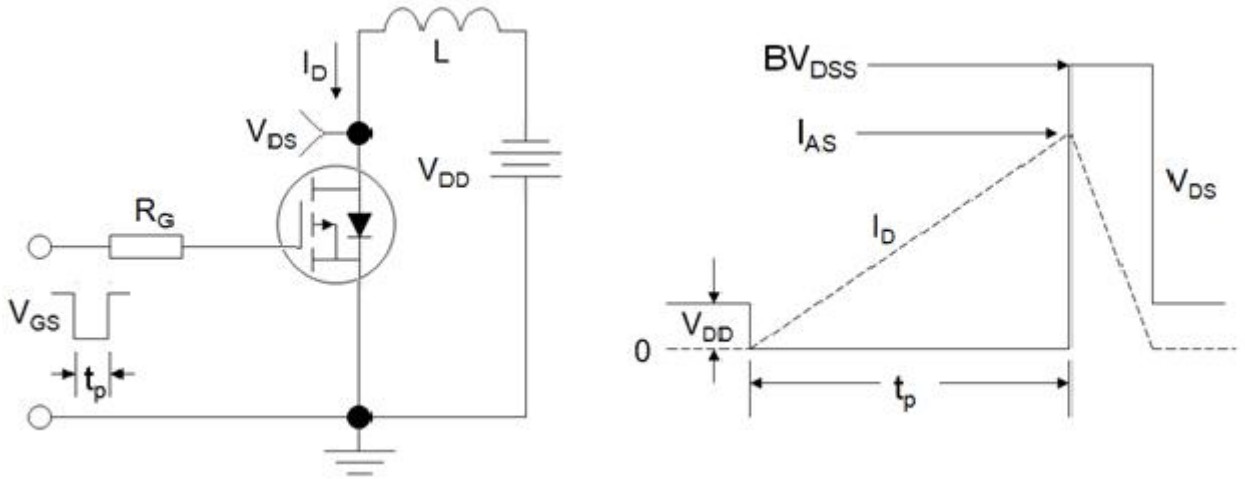
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

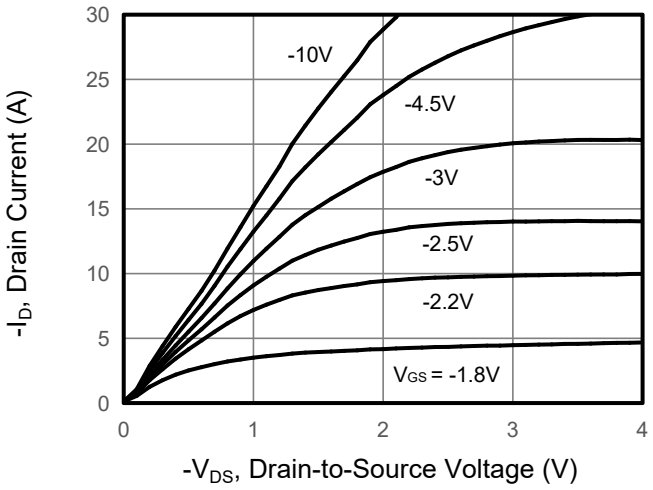


Figure 2. Transfer Characteristics

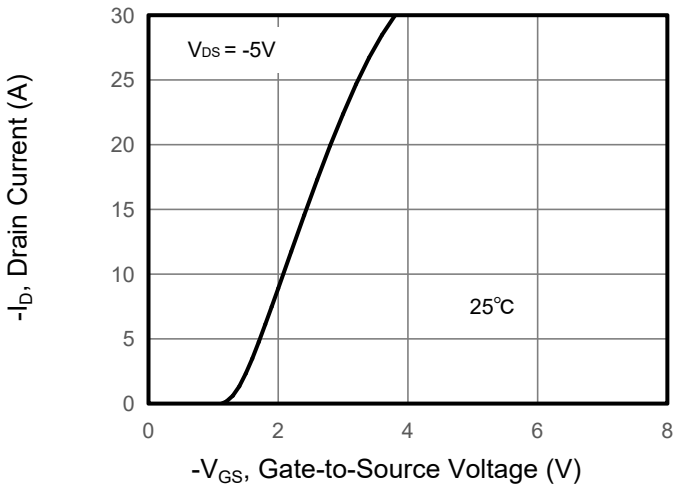


Figure 3.Drain Source On Resistance

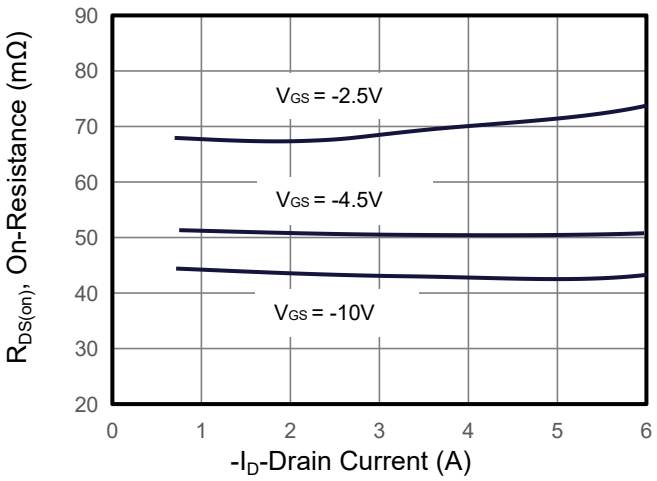


Figure 4. Gate Charge

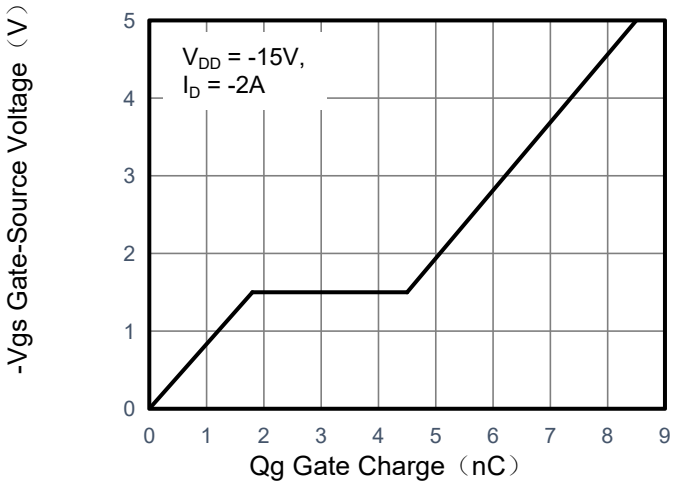


Figure 5. Capacitance

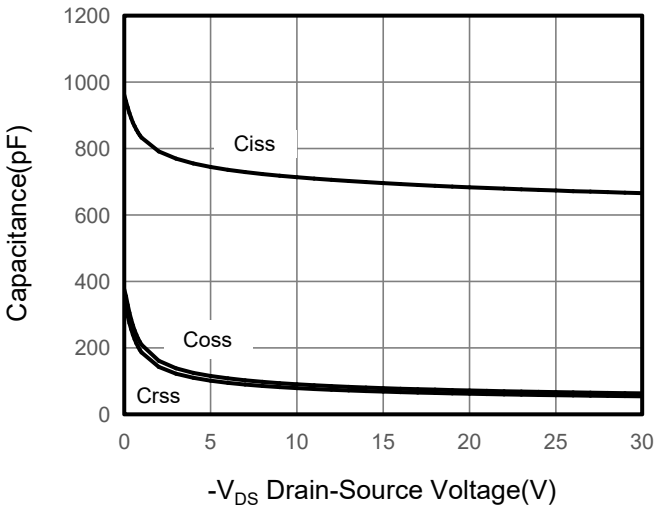
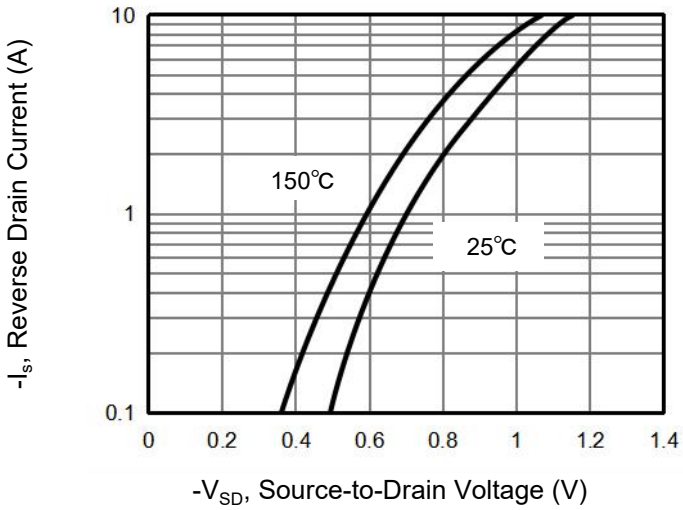


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

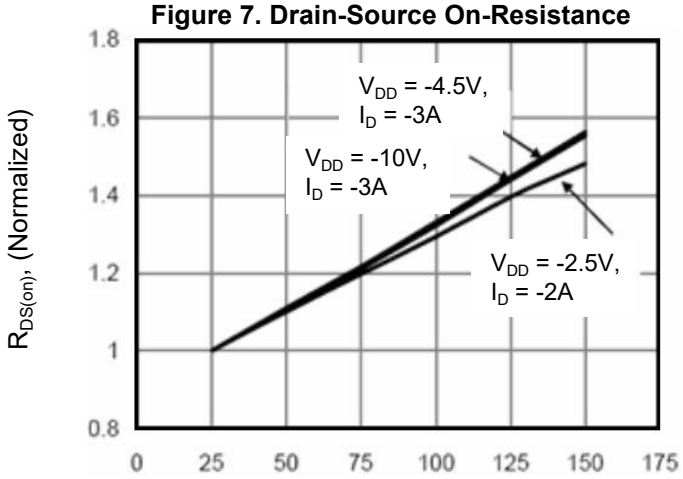


Figure 10. Safe Operation Area

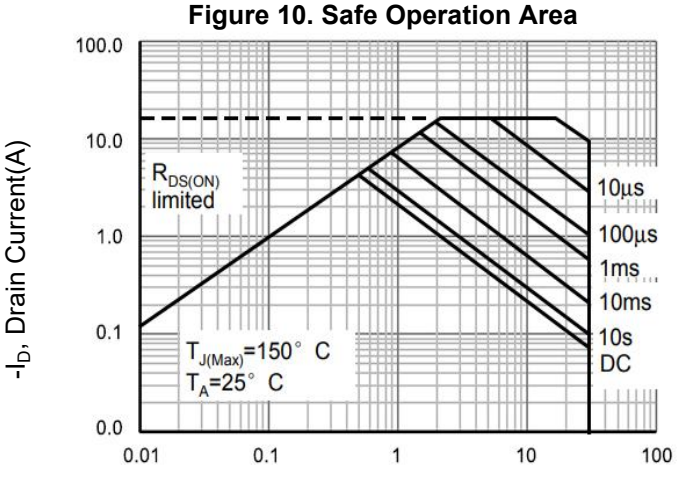
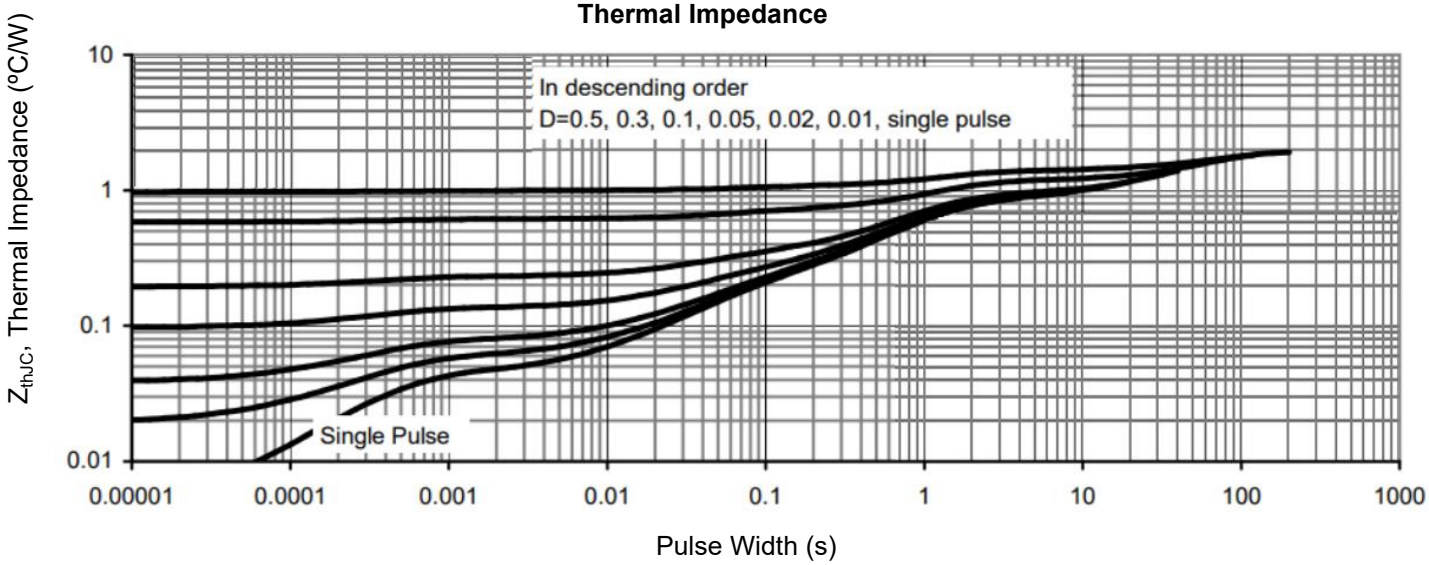
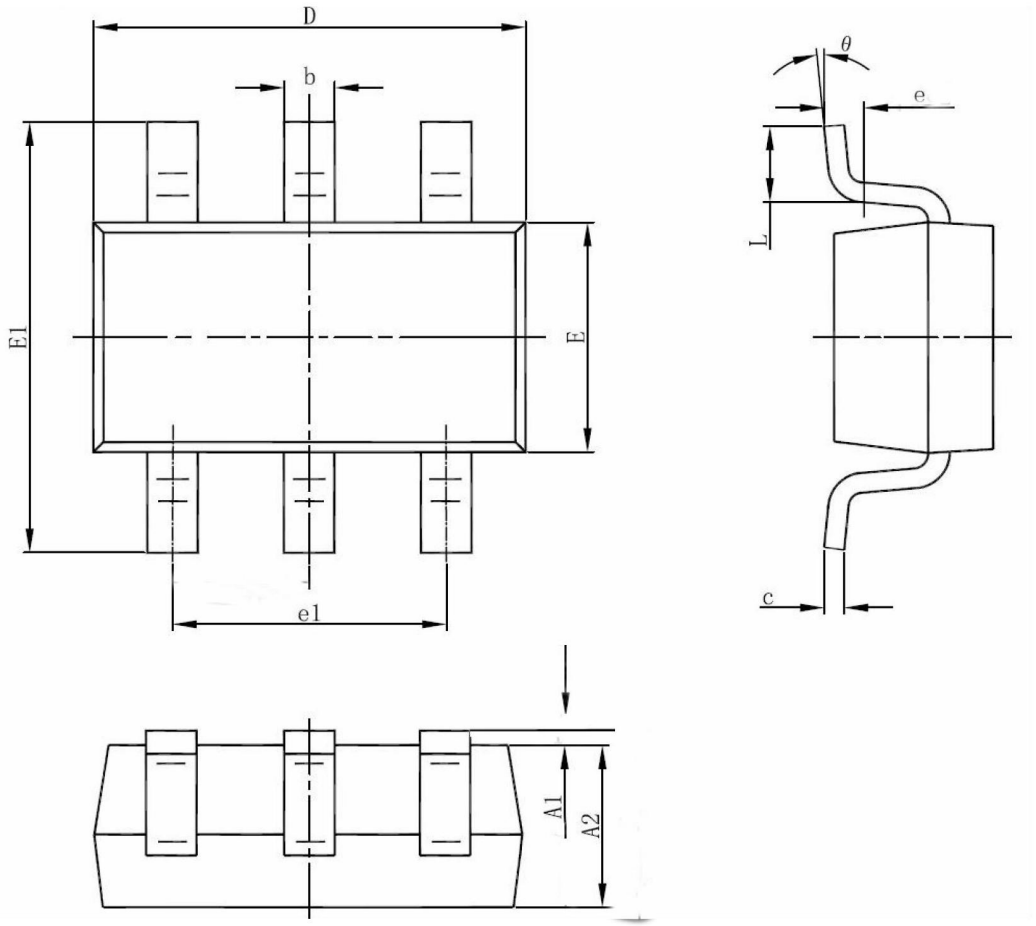


Figure 9. Normalized Maximum Transient Thermal Impedance



SOT-23-6L DUAL Package Information



DIM	MIN	NOM	MAX
A1	0.00	-	0.10
A2	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.10	0.15	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
E1	2.60	2.80	3.00
e	0.2GAUGE PLANE		
e1	-	1.90	-
L	0.30	0.45	0.60
θ	0°	-	8°
All Dimensions in mm			