Features

- ±250mV input voltage range optimized for current measurement using shunt resistors
- Low offset error and drift:
  ±0.2mV (max), ±0.9µV/°C (max)
- Fixed gain: 8.2
- Low gain error and drift:
  ±0.3% (max), ±30ppm/°C (max)
- Low nonlinearity and drift:
  0.03%, ±1ppm/°C (typical)
- 3.3V to 5V operation on high side
- System-level diagnostic features
- Safety-related certifications:
  7071V$_{PK}$ reinforced isolation per DIN VDE V 0884-17: 2021-10
  5.0kV$_{RMS}$ isolation for 1 minute per UL1577
- High CMTI: 150kV/µs (typical)

Applications

- Shunt-resistor-based current sensing in:
  - Motor drives
  - Frequency inverters
  - Uninterruptible power supplies

Description

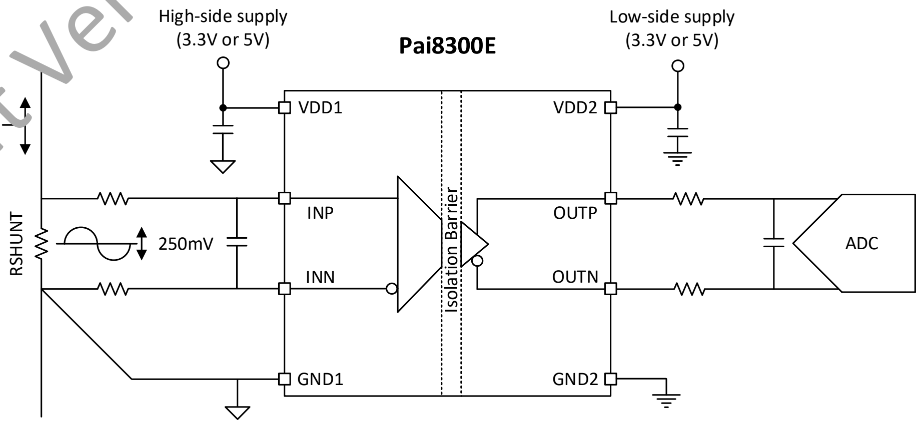
The Pai8300E is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5kV$_{RMS}$ according to VDE V 0884-17 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The input of the Pai8300E is optimized for direct connection to shunt resistors or other low voltage level signal sources. The excellent performance of the device supports accurate current control resulting in system-level power savings. The integrated missing high-side supply voltage detection and input common mode overvoltage detection simplify system-level design and diagnostics.

The Pai8300E is specified over the extended industrial temperature range of -40°C to +125°C.

PART NUMBER	PACKAGE	BODY SIZE
Pai8300E-W5R	WB SOIC-8	5.85mm*7.5mm

Simplified Schematic



1 Pin Configurations and Functions

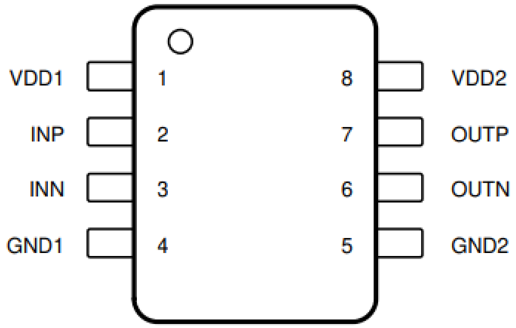


Figure 1. Pin Configuration, Top View

Pin Functions and Descriptions

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	VDD1	High-side power	High-side power supply, 3.0V to 5.5V relative to GND1.
2	INP	Analog input	Noninverting analog input.
3	INN	Analog input	Inverting analog input.
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply, 3.0V to 5.5V relative to GND2.

2 Specifications

2.1 Absolute Maximum Ratings (1)

Parameter	Symbol	MIN	MAX	UNIT
Power supply	VDD1 to GND1	-0.3	6.5	V
	VDD2 to GND2	-0.3	6.5	V
Input voltage	INP, INN	GND1-6	VDD1+0.5	V
Output voltage	OUTP, OUTN	GND2-0.5	VDD2+0.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Junction temperature, T_J	T_J	-40	150	°C
Storage temperature, T_{stg}	T_{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

2.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Description	MIN	MAX	UNIT
High side power supply	VDD1 to GND1	3.0	5.5	V
Low side power supply	VDD2 to GND2	3.0	5.5	V
Differential input voltage before clipping output	VIN = VINP – VINN	-320	320	mV
Specified linear differential input full-scale	VIN = VINP – VINN	-250	250	mV
Absolute common-mode input voltage (1)	(VINP + VINN) / 2 to GND1	-2	VDD1	V
Operating common-mode input voltage	(VINP + VINN) / 2 to GND1	-0.16	VDD1-2.1	
T_A	Ambient Temperature	-40	125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See the specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the Absolute Maximum Ratings table.

2.4 Thermal Information

Symbol	Parameter	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85	°C/W
$R_{\theta JC\ (top)}$	Junction-to-case (top) thermal resistance	26	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43	°C/W

2.5 Insulation Specifications

Parameter	Description	Test condition	VALUE	UNIT
CLR	External clearance	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage	Shortest pin-to-pin distance across the package surface	≥ 8	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	

DIN V VDE V 0884-17 (VDE V 0884-17): 2021-10$^{(2)}$

Parameter	Description	Test condition	VALUE	UNIT
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave)	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 sec (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage $^{(3)}$	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	6250	V_{PK}
Vpd (m)	Input to Output Test Voltage, Method A After Environmental Tests Subgroup1	$V_{IORM} \times 1.875$ = Vpd (m), tini = 60 sec, tm = 10 sec, partial discharge < 5 pC	3977	V_{PK}
	After input and/or Safety Test Subgroup2 and Subgroup3	$V_{IORM} \times 1.6$ = Vpd (m), tini = 60 sec, tm = 10 sec, partial discharge < 5 pC	3394	V_{PK}
	Method b1; At routine test (100% production) and preconditioning (type test) $^{(4)}$	$V_{IORM} \times 1.2$ = Vpd (m), tini =1 sec, tm = 1 sec, partial discharge < 5 pC	2545	V_{PK}
C_{IO}	Barrier capacitance, input to output $^{(5)}$	$V_{IO} = 0.4 \sin(2\pi ft)$, f =1 MHz	1.2	pF
R_{IO}	Isolation resistance, input to output $^{(5)}$	V_{IO} = 500 V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	Ω
		V_{IO} = 500 V at T_S =150°C	$> 10^{9}$	Ω
	Pollution degree		2	
	Climatic category		40/125/21	

UL 1577

Parameter	Description	Test condition	VALUE	UNIT
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000V_{RMS}$, t = 60 sec.(qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000V_{RMS}$, t = 1 sec (100% production)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

2.6 Safety-Related Certifications

CQC	Certified according to GB 4943.1-2022	Basic insulation at $1118V_{RMS}$ ($1580V_{PK}$) Reinforced insulation at $557V_{RMS}$ ($788V_{PK}$)	Pending
UL	Recognized under UL 1577 Component Recognition Program	Single protection, $5kV_{RMS}$	Pending
VDE	Certified according to DIN V VDE V 0884-17:2021-10, and DIN EN 60950-1 (VDE 0805 Teil 1):2014-08	Reinforced Insulation Maximum Transient Isolation voltage, $7071V_{PK}$; Maximum Repetitive Peak Isolation Voltage, $2121V_{PK}$; Maximum Surge Isolation Voltage, $10kV_{PK}$	File: 40056491

2.7 Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

Symbol	Description	Test condition	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	$R_{\theta JA}$=85°C/W, T_J=150°C, T_A =25°C, VDD1=VDD2=5.5V	-	-	294	mA
		$R_{\theta JA}$=85°C/W, T_J=150°C, T_A=25°C, VDD1=VDD2=3.3V	-	-	445	mA
P_S	Safety supply power	$R_{\theta JA}$=85°C/W, T_J=150°C, T_A=25°C			1470	mW
T_S	Maximum Safety temperature				150	°C

The maximum safety temperature, TS, has the same value as the maximum junction temperature, TJ, specified for the device. The IS and PS parameters represent the safety current and safety power respectively. The maximum limits of IS and PS should not be exceeded. These limits vary with the ambient temperature, TA. The junction-to-air thermal resistance, RθJA, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: TJ = TA + RθJA × P, where P is the power dissipated in the device. TJ (max) = TS = TA + RθJA × PS, where TJ (max) is the maximum allowed junction temperature.PS = IS × VI, where VI is the maximum input voltage.

3 Specifications

3.1 Electrical Characteristics

Minimum and maximum specifications of the Pai8300E apply from TA=-40°C to +125°C, VDD1=3.0V to 5.5V, VDD2=3.0V to 5.5V, INP=-250mV to +250mV, and INN=GND1=0V; typical specifications are at TA=25°C, VDD1=5V, and VDD2=3.3V (unless otherwise noted)

Parameter		Test condition	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{CMov}	Common-mode overvoltage detection level		VDD1-2			V
	Hysteresis of common-mode overvoltage detection level			100		mV
V_{OS}	Input offset voltage (1)	initial, at TA = 25°C, $V_{INP} = V_{INN} = GND1$	-0.2	±0.01	0.2	mV
TCV_{OS}	Input offset drift (1)		-0.9	±0.1	0.9	µV/°C
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, V_{CM} min ≤ V_{CM} ≤ V_{CM} max		85		dB
		f_{IN} =10KHz, V_{CM} min ≤ V_{CM} ≤ V_{CM} max		85		dB
C_{IN}	Single-ended input capacitance	INN = GND1, f_{IN} = 275kHz		25		pF
C_{IND}	Differential input capacitance	f_{IN} = 275kHz		20		pF
R_{IN}	Single-ended input resistance	INN = GND1		33		kΩ
R_{IND}	Differential input resistance			39		kΩ
I_{IB}	Input bias current	INP = INN =GND1, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$	-13	-10	-7	uA
I_{IO}	Input offset current			±5		nA
ANALOG OUTPUT						
	Normal gain			8.2		V/V
E_G	Gain error (1)	Initial, at T_A = 25°C	-0.3%	±0.05%	0.3%	
TCE_G	Gain error drift (1)		-30	±5	30	ppm/°C
	Nonlinearity (1)		-0.03%	±0.01%	0.03%	
	Nonlinearity drift			±1		ppm/°C
THD	Total harmonic distortion	V_{IN} = 0.5V, f_{IN} = 10kHz, BW = 100kHz		-88		dB
	Output noise	$V_{INP} = V_{INN} = GND1$, BW = 100kHz		280		uV_{RMS}
SNR	Signal-to-noise ratio	V_{IN} = 0.5V, f_{IN} = 1kHz, BW = 10kHz		86		dB
		V_{IN} = 0.5V, f_{IN} = 10kHz, BW = 100kHz		77		dB
PSRR	Power-supply rejection ratio (2)	PSRR vs VDD1, at DC		-100		dB
		PSRR vs VDD1, 100mV and 10kHz ripple		-100		

Parameter		Test condition	MIN	TYP	MAX	UNIT
ANALOG INPUT						
		PSRR vs VDD2, at DC		-110		
		PSRR vs VDD2, 100mV and 10kHz ripple		-100		
V_{CMout}	Common-mode output voltage		1.40	1.44	1.49	V
$V_{FAILSAFE}$	Failsafe differential output voltage			-2.6	-2.5	V
BW	Output bandwidth		250	310		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		0.2		Ω
	Output short-circuit current			±13		mA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1kV	100	150		kV/us
POWER SUPPLY						
$VDD1_{UVLO}$	VDD1 undervoltage detection threshold voltage	VDD1 Rising	2.3	2.5	2.7	V
	VDD1 undervoltage hysteresis	Hysteresis		0.15		V
$VDD2_{UVLO}$	VDD2 undervoltage detection threshold voltage	VDD2 Rising	2.2	2.4	2.6	V
	VDD2 undervoltage hysteresis	Hysteresis		0.35		V
IDD1	High-side supply current	3.0V ≤ VDD1 ≤ 5.5V		4	6	mA
IDD2	Low-side supply current	3.0V ≤ VDD2 ≤ 5.5V		3	5	mA

(1) The typical value includes one sigma statistical variation.

(2) This parameter is output referred.

3.2 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_r	Rise time of OUTP, OUTN	See Fig2		1.0		us
t_f	Fall time of OUTP, OUTN	See Fig2		1.0		us
	INP, INN to OUTP, OUTN signal delay (50% – 50%)	unfiltered output, see Fig2		1.2	1.5	us
	INP, INN to OUTP, OUTN signal delay (50% – 10%)	unfiltered output, see Fig2		0.7	1	us
	INP, INN to OUTP, OUTN signal delay (50% – 90%)	unfiltered output, see Fig2		1.7	2	us
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0V, to OUTP, OUTN valid, 0.1% settling		350		us

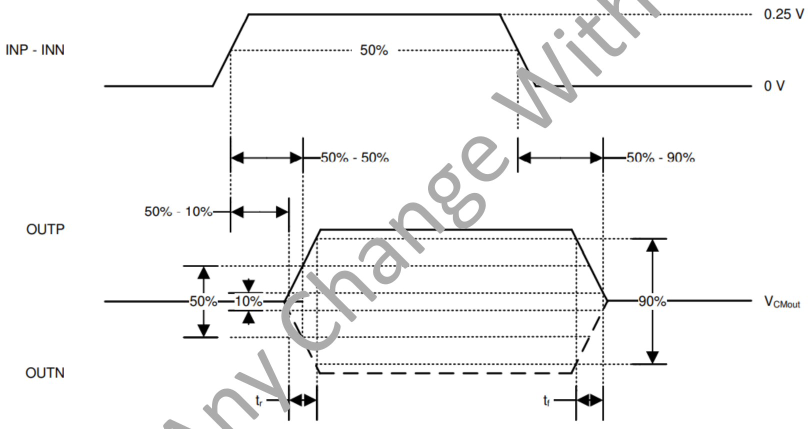


Figure 2. Rise, Fall, and Delay Time Waveforms

3.3 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, V_{INP} = –250 mV to 250 mV, V_{INN} = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

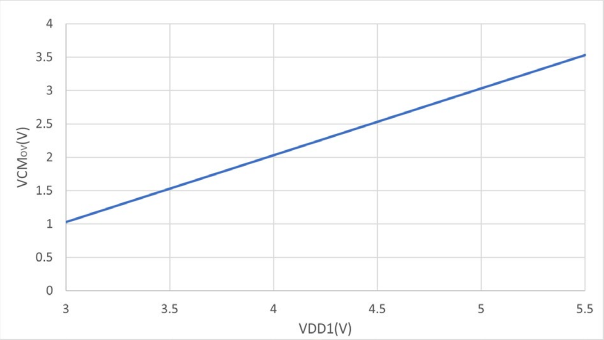


Figure 3. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage

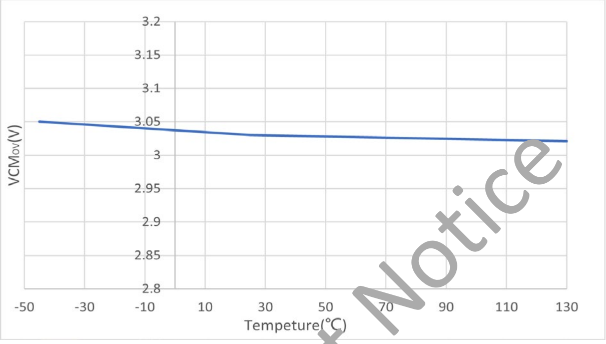


Figure 4. Common-Mode Overvoltage Detection Level vs Temperature

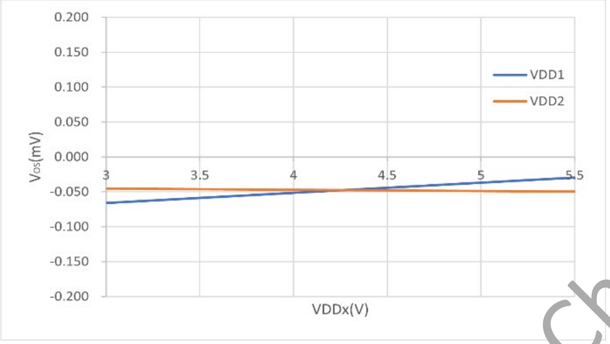


Figure 5. Input Offset Voltage vs Supply Voltage

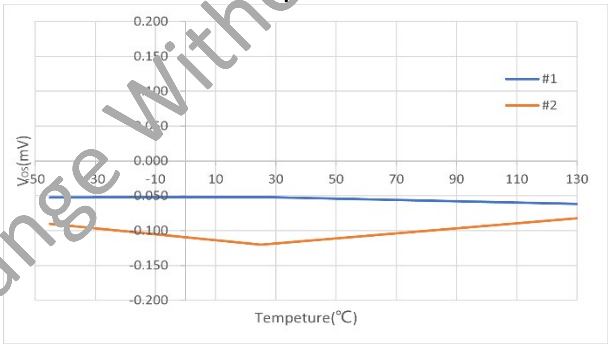


Figure 6. Input Offset Voltage vs Temperature

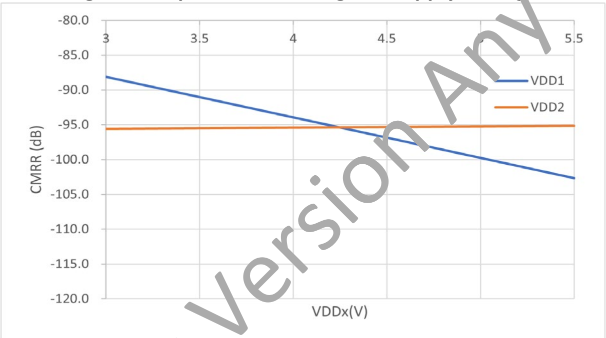


Figure 7. Common-Mode Rejection Ratio vs Supply Voltage

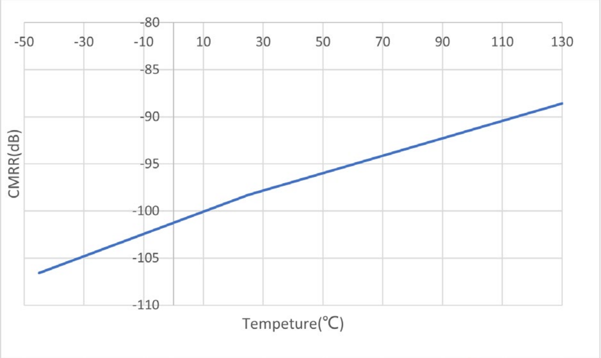


Figure 8. Common-Mode Rejection Ratio vs Temperature

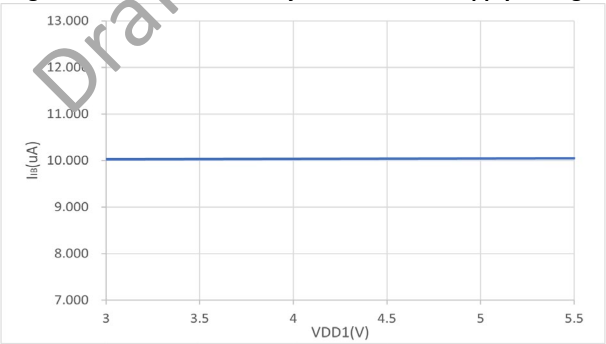


Figure 9. Input Bias Current vs High-Side Supply Voltage

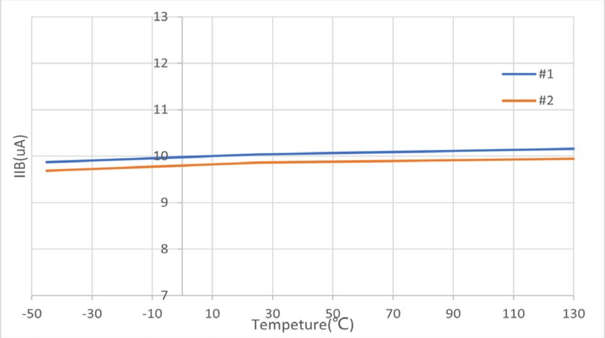


Figure 10. Input Bias Current vs Temperature

at VDD1 = 5 V, VDD2 = 3.3 V, V_{INP} = –250 mV to 250 mV, V_{INN} = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

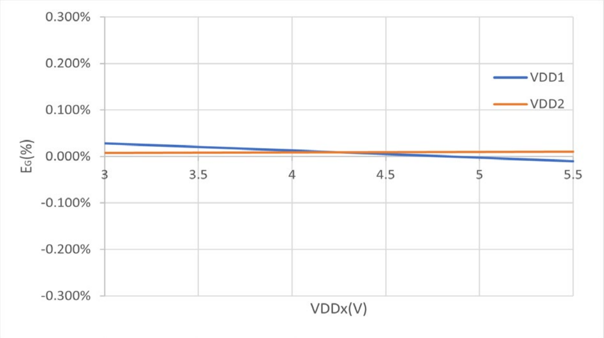


Figure 11. Gain Error vs Supply Voltage

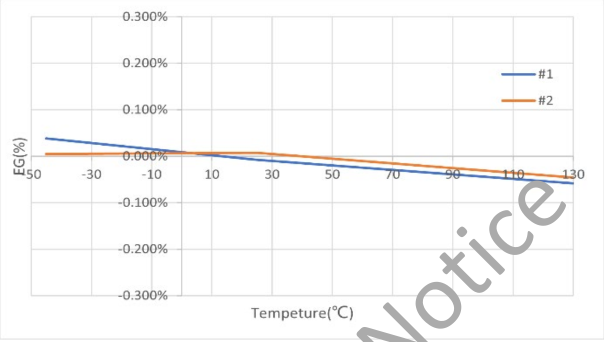


Figure 12. Gain Error vs Temperature

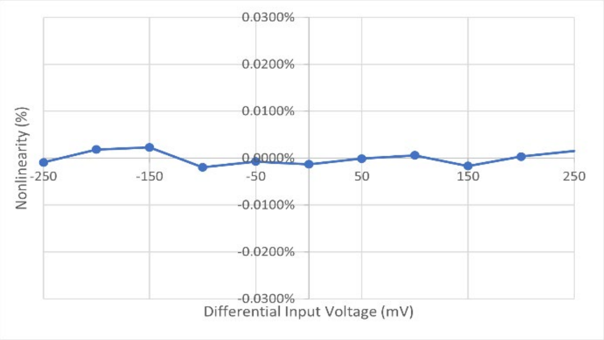


Figure 13. Nonlinearity vs Input Voltage

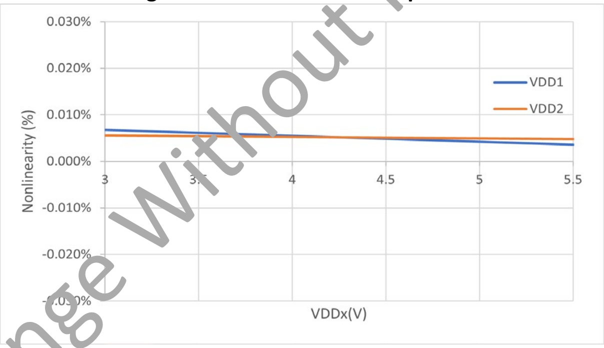


Figure 14. Nonlinearity vs Supply Voltage

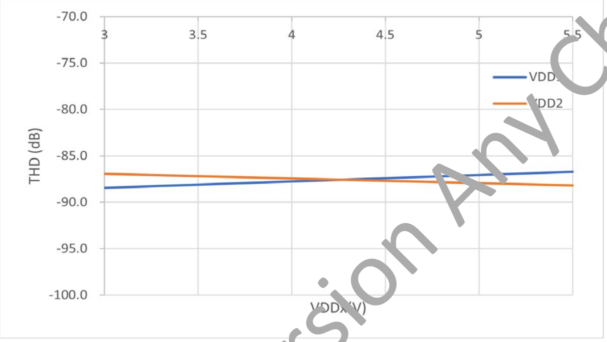


Figure 15. Total Harmonic Distortion vs Supply Voltage

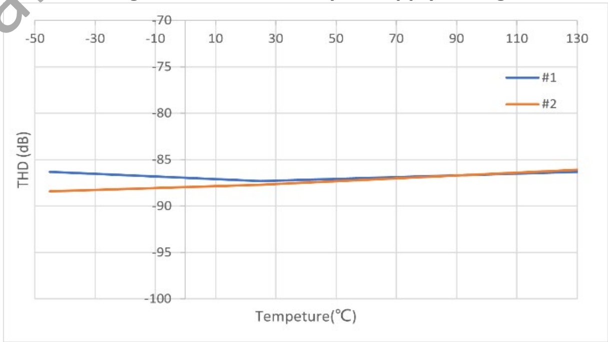


Figure 16. Total Harmonic Distortion vs Temperature

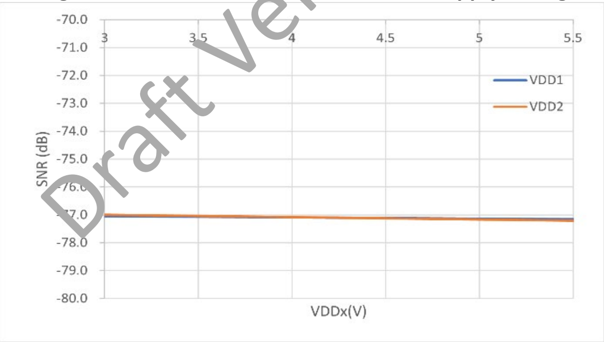


Figure 17. Signal-to-Noise Ratio (10kHz) vs Supply Voltage

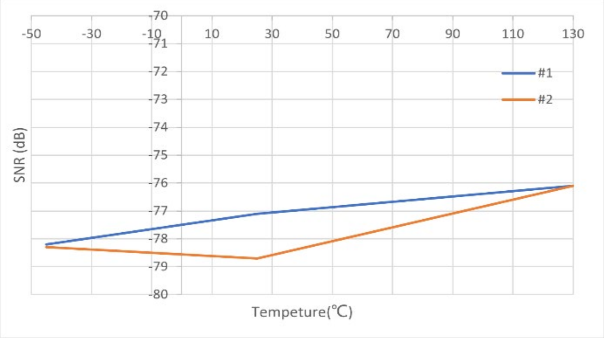


Figure 18. Signal-to-Noise Ratio (10kHz) vs Temperature

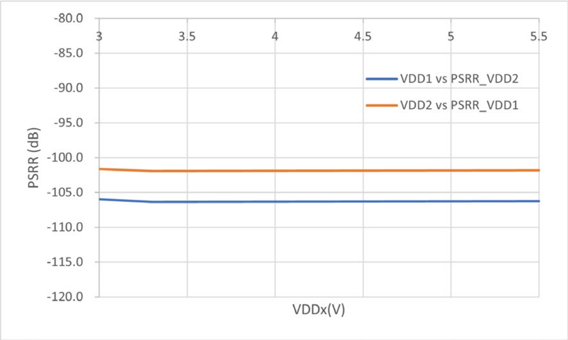


Figure 19. Power-Supply Rejection Ratio vs Supply Voltage

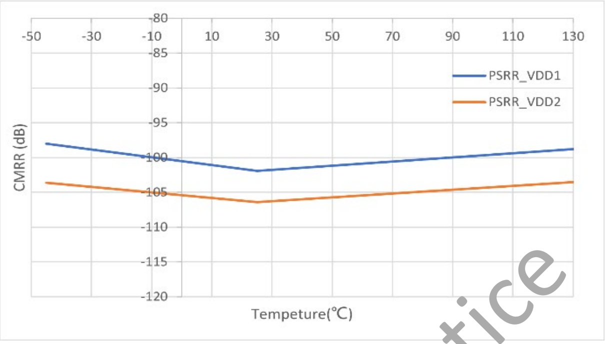


Figure 20. Power-Supply Rejection Ratio vs Temperature

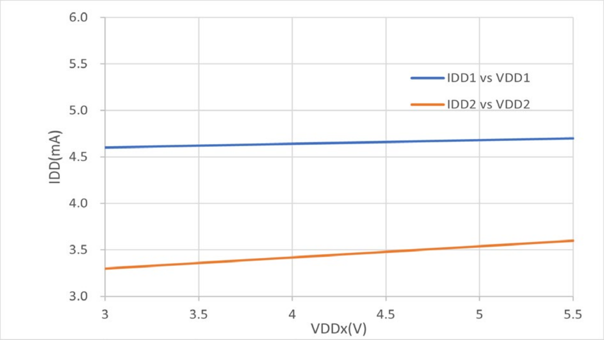


Figure 21. Supply Current vs Supply Voltage

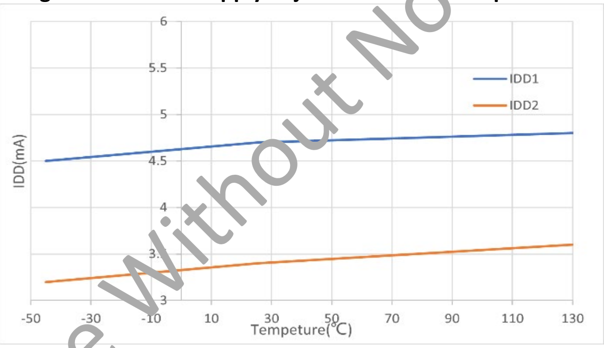


Figure 22. Supply Current vs Temperature

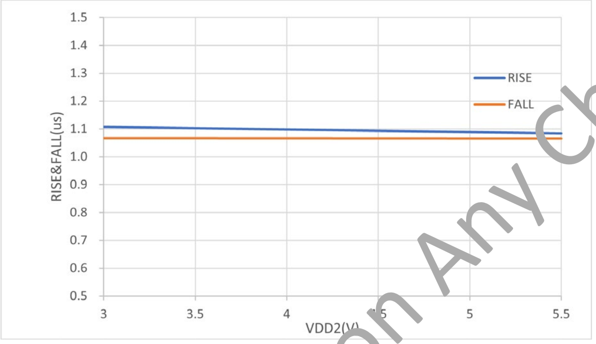


Figure 23. Output Rise and Fall Time vs Low-Side Supply

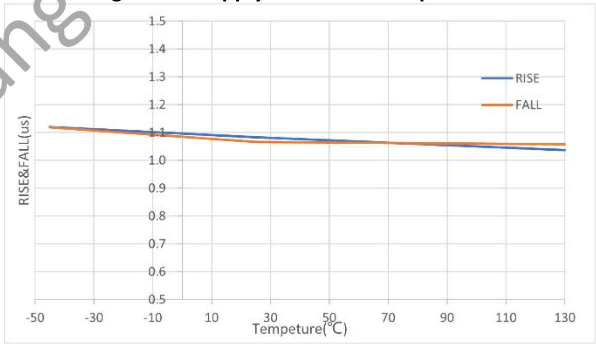


Figure 24. Output Rise and Fall Time vs Temperature

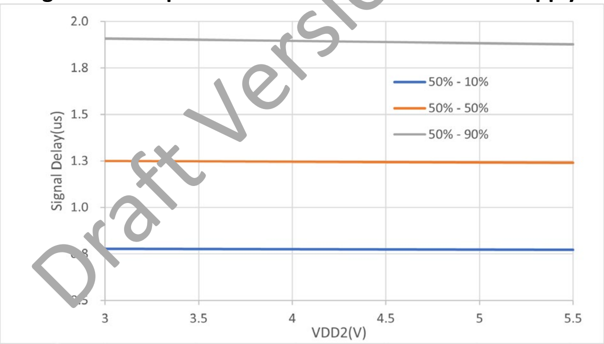


Figure 25. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

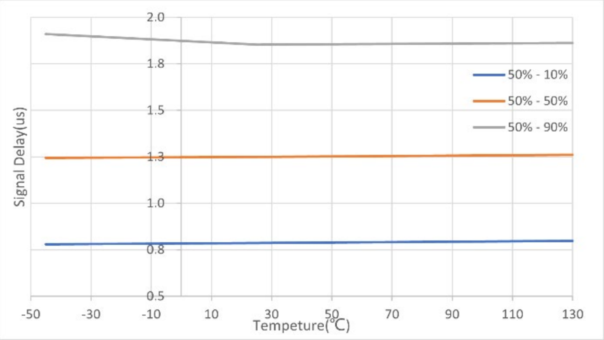


Figure 26. V_{IN} to V_{OUT} Signal Delay vs Temperature

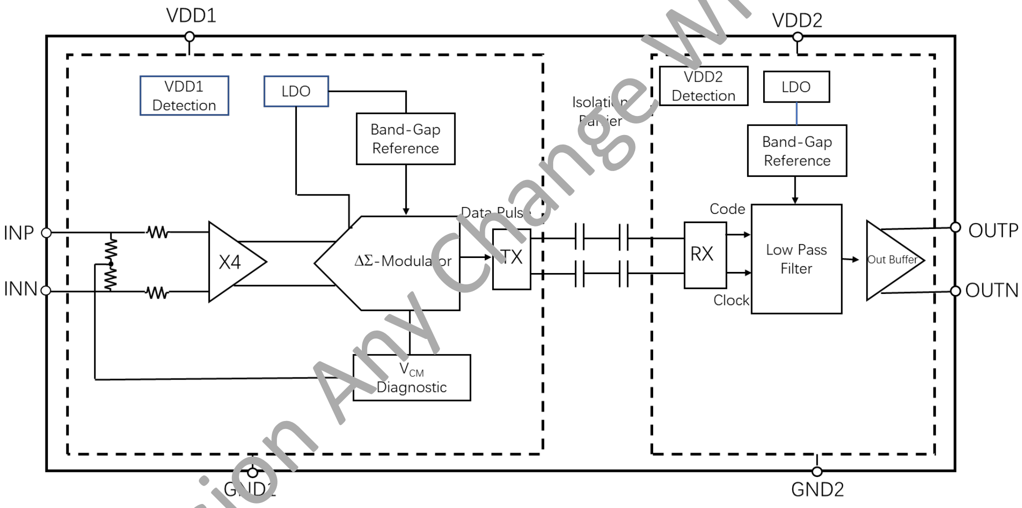
4 Detailed Description

4.1 Overview

The Pai8300E is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator generates data pulse. The drivers (called TX in the Functional Block Diagram) transfer the data pulse of the modulator across the isolation barrier. The received data pulse is synchronized and processed, as shown in the Functional Block Diagram, by a low pass filter and out buffer on the low-side and presented as a differential output of the device.

Pai8300E adopts single channel transfer architecture and saves one clock channel, compared with current other amplifiers products, Pai8300E has the lowest power consumption. Pai8300E also uses Intelligent voltage divider technology (iDivider® technology) which is a new generation digital isolator technology invented by 2PaiSEMI to support a high level of magnetic field immunity.

4.2 Function block diagram



4.3 Feature Description

4.3.1 Analog Input

The differential amplifier input stage of the Pai8300E feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 with a differential input impedance of 39kΩ. The modulator converts the analog signal into data pulse that is transferred across the isolation barrier, as described in patented iDivider® technology.

There are two restrictions on the analog input signals (VINP and VINN). First, if the input voltage exceeds the range GND1-6V to VDD1+0.5V, the input current must be limited to 10mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

4.3.2 Isolation Channel Signal Transmission

The Pai8300E uses the patented iDivider® technology to transmit the modulator output data pulse across the SiO_2 -based isolation barrier. The Pai8300E also uses special circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

4.3.3 Failsafe Output

The Pai8300E offers a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active in two cases:

- When the high-side supply VDD1 of the Pai8300E is missing.
- When the common-mode input voltage, that is $V_{CM} = (V_{INP} + V_{INN})/2$, exceeds the minimum common-mode overvoltage detection level V_{CMov} of VDD1–2V.

Figure 27 and Figure 28 show the fail-safe output of the Pai8300E as a negative differential output voltage value that does not occur under normal device operation. Use the $V_{FAILSAFE}$ voltage specified in the Electrical Characteristics table as a reference value for the fail-safe detection on a system level.

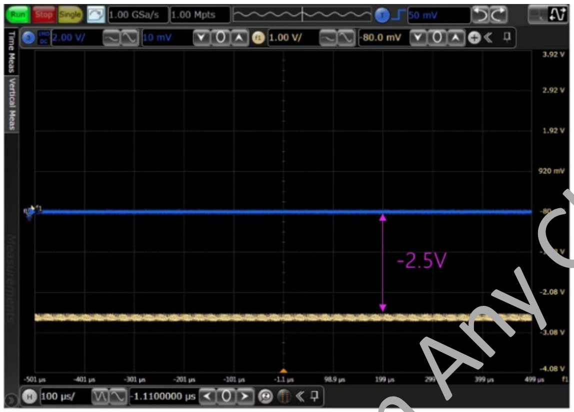


Figure 27. Typical Negative Clipping Output of Pai8300E

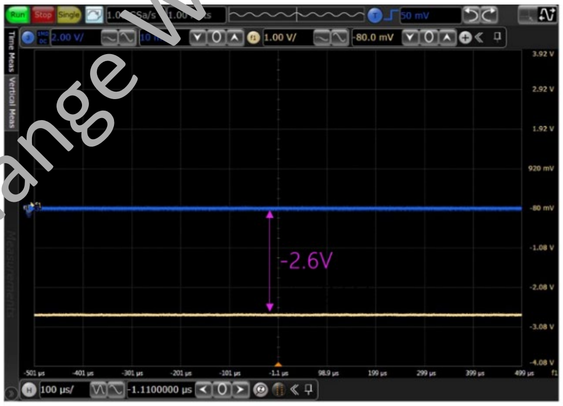


Figure 28. Typical Fail-Safe Output of Pai8300E

4.4 Device Functional Modes

The Pai8300E is operational when the power supplies VDD1 and VDD2 are applied, as specified in the Recommended Operating Conditions table in the Specifications section.

5 Application and Implementation

5.1 Application Information

The low input voltage range, very low nonlinearity, and temperature drift make the Pai8300E a high-performance solution for industrial applications where shunt-based current sensing with high common-mode voltage levels is required.

5.2 Typical Application

Isolated amplifiers are widely used in frequency inverters, which are critical parts of industrial motor drives, photovoltaic inverters, uninterruptible power supplies, and other industrial applications. The input structure of the Pai8300E is optimized for use with low-value shunt resistors in current sensing applications.

Figure 29 depicts a typical operation of the Pai8300E for current sensing in a frequency inverter application. Phase current measurement is accomplished through the shunt resistors, R_{SHUNT} (in this case, a two-pin shunt). The differential input and the high common-mode transient immunity of the Pai8300E ensure reliable and accurate operation even in high-noise environments (such as the power stage of the motor drive). The high impedance input and wide input voltage range make the Pai8300E suitable for DC bus voltage sensing.

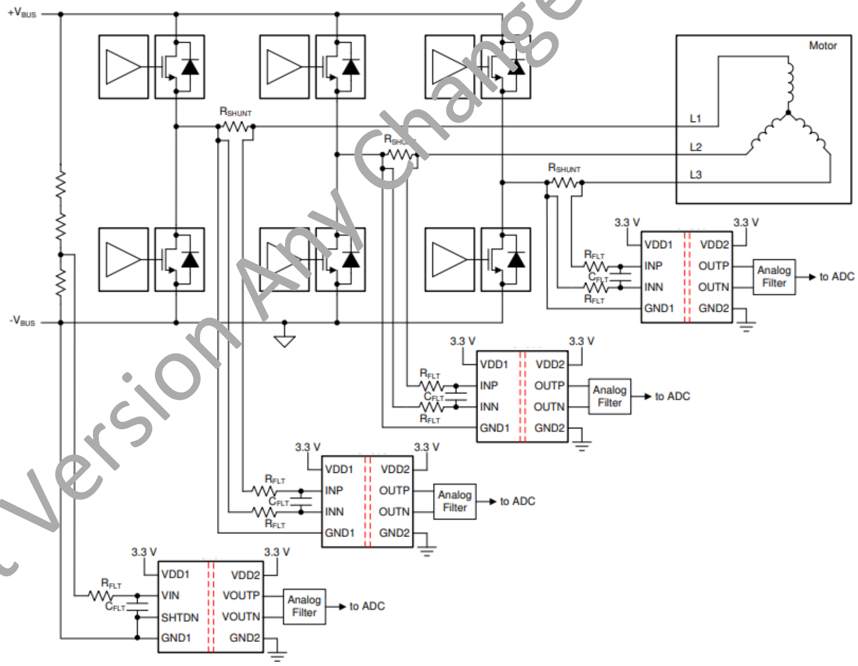


Figure 29. Using the Pai8300E for Current Sensing in Frequency Inverters

5.2.1 Design Requirements

Table1 lists the parameters for this typical application.

Table1 Design Requirement

PARAMETER	VALUE
High-side supply voltage	3.3V or 5V
Low-side supply voltage	3.3V or 5V
Voltage drop across the shunt for a linear response	± 250mV (maximum)
Signal delay (50% VIN to 90% OUTP, OUTN)	2µs (maximum)

5.2.2 Detailed Design Procedure

The high-side power supply (VDD1) for the Pai8300E is derived from the power supply of the upper gate driver. Further details are provided in the Power Supply Recommendations section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the Pai8300E (INN). If a four-pin shunt is used, the inputs of the Pai8300E device are connected to the inner leads and GND1 is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250mV$

- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$. For systems using single-ended input ADC, Figure 30 shows an example of an amplifier-based signal conversion and filter circuit as used for recommended example. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

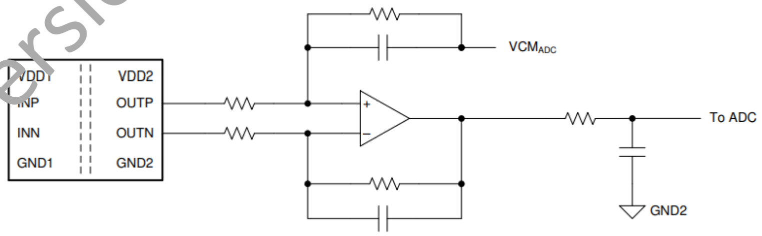


Figure 30. Connecting the Pai8300E Output to a Single-Ended Input ADC

5.2.3 Application Curves

In frequency inverter applications, the power switches must be protected in case of an overcurrent condition. To allow for fast powering-off of the system, a low delay caused by the isolated amplifier is required. Figure 31 shows the typical full-scale step response of the Pai8300E. Consider the delay of the required window comparator and the micro control unit (MCU) to calculate the overall response time of the system.

Figure 31. Step Response of the Pai8300E

The high linearity and low temperature drift of offset and gain errors of the Pai8300E, as shown in Figure 32, allow design of motor drives with low torque ripple.

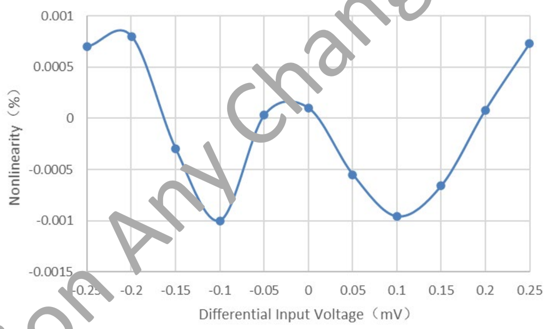


Figure 32. Typical Nonlinearity of the Pai8300E

5.3 What to Do and What Not to Do

Do not leave the inputs of the Pai8300E unconnected (floating) when the device is powered up. If both device inputs are left floating, the input bias current drives these inputs to the output common mode of the analog frontend approximately 2V. If the high-side supply voltage VDD1 is below 4 V, the internal common-mode overvoltage detector turns on and makes output -2.5V as described in the Fail-Safe Output section, which may lead to an undesired reaction on the system level.

5.4 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply (VDD1) for the device is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5V or 3.3V ± 10%. Alternatively, a low-cost low-dropout (LDO) regulator may be used to minimize noise on the power supply. A low-ESR decoupling capacitor of 0.1 µF to filter this power-supply path is recommended. Place this capacitor (C2 in Figure 33) as close as possible to the VDD1 pin of the Pai8300E for best performance. If better filtering is required, an additional 2.2 µF capacitor may be used. The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads, and GND1 is connected to one of the outer leads of the shunt. To decouple the low-side power supply on the controller side, use a 0.1 µF capacitor placed as close to the VDD2 pin of the Pai8300E as possible, followed by an additional capacitor from 1 µF to 10 µF.

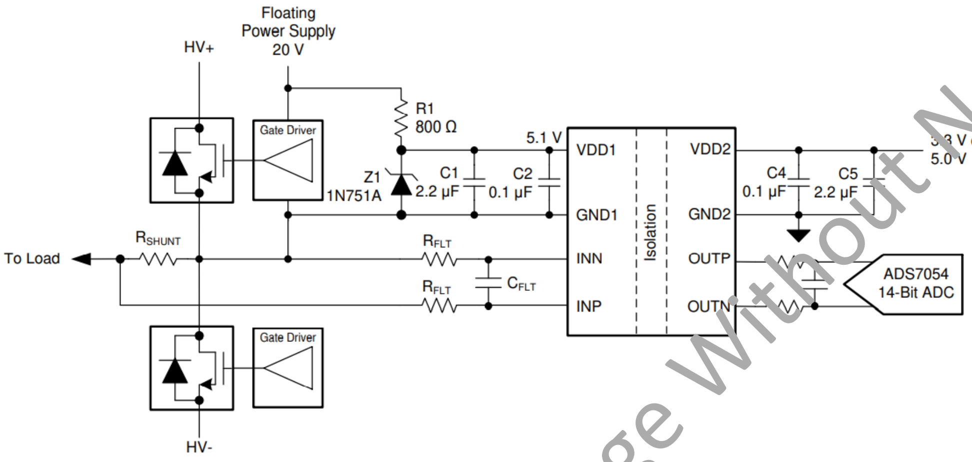


Figure 33. Zener-Diode-Based, High-Side Power Supply

5.5 Layout

Figure34 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the Pai8300E supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the Pai8300E and keep the layout of both connections symmetrical.

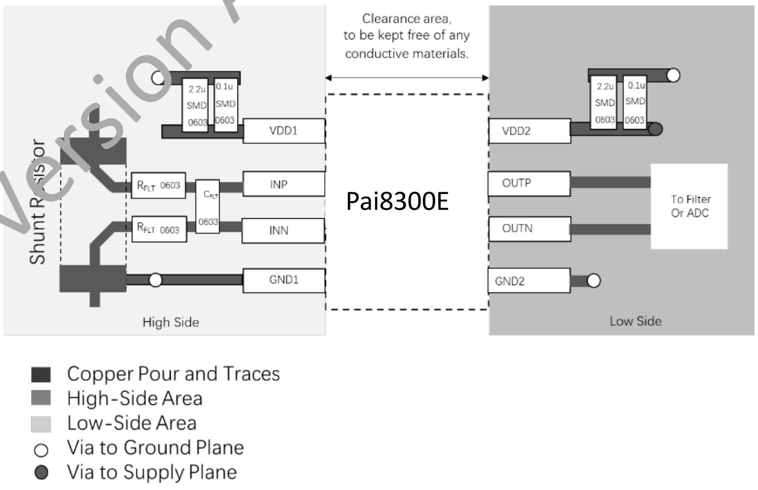
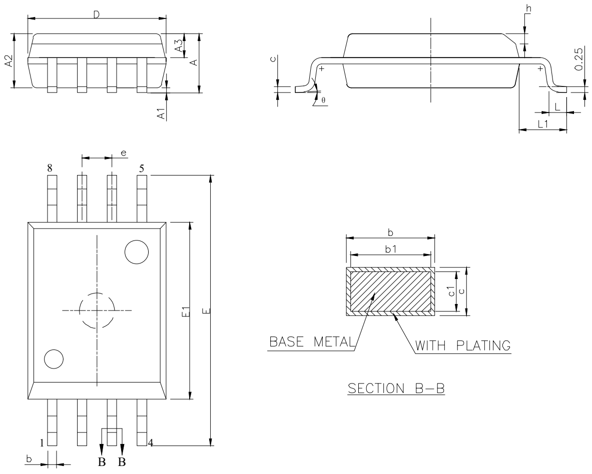


Figure 34. Recommended Layout of the Pai8300

6 Outline Dimensions



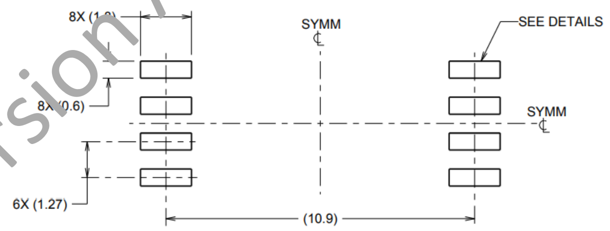
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	__	__	2.65
A1	0.10	__	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	__	0.47
b1	0.38	0.41	0.44
c	0.25	__	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	__	0.50
L	0.50	__	1.00
L1	2.[illegible]0REF		
θ	0°	__	8°

Figure 35. Outline Package

7 Land Patterns

The Fig36 illustrates the recommended land pattern details for the Pai8300E in a wide-body SOIC-8 package.

Figure 36. WB-SOIC-8 Land Pattern



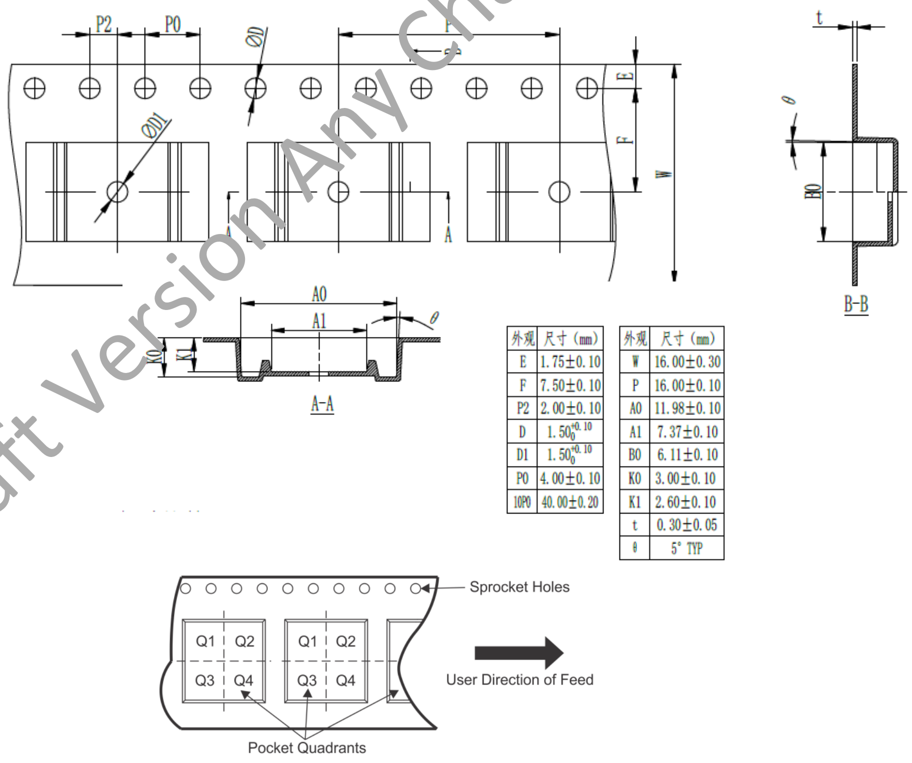
Note: All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

8 Top Marking

Figure 37. Top Marking

Line 1	XXXXXXXX=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXXX, no special meaning

9 Reel Information



外观	尺寸（mm）
E	1.75±0.10
F	7.50±0.10
P2	2.00±0.10
D	$1.50^{+0.10}_{0}$
D1	$1.50^{+0.10}_{0}$
P0	4.00±0.10
10P0	40.00±0.20

外观	尺寸（mm）
W	16.00±0.30
P	16.00±0.10
A0	11.98±0.10
A1	7.37±0.10
B0	6.11±0.10
K0	3.00±0.10
K1	2.60±0.10
t	0.30±0.05
θ	5° TYP

Figure 38. Reel Information

Note: The Pin 1of the chip is in the quadrant Q1

10 Ordering Guide

Model Name [1]	Temperature Range	Withstand Voltage Rating (kVRMS)	Package	MSL Peak Temp 1	Quantity per Reel
Pai8300E-W5R	−40~125°C	5.0	WB SOIC-8	Level-3-260C-168 HR	1000

(1) The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

11 Important Notice and Disclaimer

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12 Revision History

Ver	Date	Page	Change Record
0.1	2022-06-09	All	Initial version.
0.2	2022-08-20	All	Add figures.
0.3	2022-09-19	All	Increase application items, package information.
0.4	2022-12-05	All	Update some format and modify figure sequence.
0.5	2023-07-11	All	Update Certifications, Input offset drift, gain error drift, CMRR, RIN, CIN, and some descriptions.