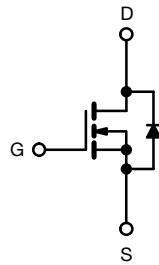


## Power MOSFET

**TO-220AB**


N-Channel MOSFET

### FEATURES

- Low gate charge  $Q_g$  results in simple drive requirement
- Improved gate, avalanche, and dynamic  $dV/dt$  ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective  $C_{oss}$  specified
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


 Available  
**RoHS\***  
 Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

### APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptable power supply
- High speed power switching

### TYPICAL SMPS TOPOLOGIES

- Two transistor forward
- Half bridge
- Full bridge

### PRODUCT SUMMARY

$V_{DS}$ (V)	500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.85
$Q_g$ max. (nC)	38	
$Q_{gs}$ (nC)	9.0	
$Q_{gd}$ (nC)	18	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF840APbF
Lead (Pb)-free and halogen-free	IRF840APbF-BE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	500	V	
Gate-source voltage	$V_{GS}$	$\pm 30$		
Continuous drain current	$V_{GS}$ at 10 V	$T_C = 25$ °C	8.0	A
		$T_C = 100$ °C	5.1	
Pulsed drain current <sup>a</sup>	$I_{DM}$	32		
Linear derating factor		1.0	W/°C	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	510	mJ	
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	8.0	A	
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	13	mJ	
Maximum power dissipation	$T_C = 25$ °C	$P_D$	125	W
Peak diode recovery $dV/dt$ <sup>c</sup>		$dV/dt$	5.0	V/ns
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s		300	
Mounting torque	6-32 or M3 screw		10	
			1.1	N · m

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 16$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 8.0$  A (see fig. 12)
- $I_{SD} \leq 8.0$  A,  $dI/dt \leq 100$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C
- 1.6 mm from case



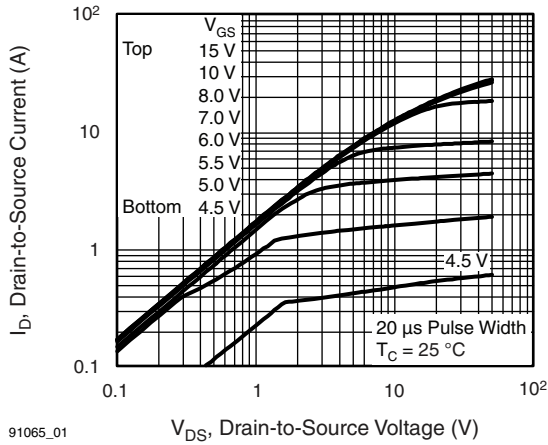
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62	°C/W
Case-to-sink, flat, greased surface	R <sub>thCS</sub>	0.50	-	
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	1.0	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		500	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.58	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.8 A <sup>b</sup>	-	-	0.85	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 4.8 A <sup>b</sup>		3.7	-	-	S
<b>Dynamic</b>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	1018	-	pF
Output capacitance	C <sub>oss</sub>			-	155	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	8.0	-	
Output capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 1.0 V, f = 1.0 MHz		-	1490	-	
Output capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 400 V, f = 1.0 MHz		-	42	-	
Effective output capacitance	C <sub>oss eff.</sub>	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 0 V to 400 V <sup>c</sup>		-	56	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 8 A, V <sub>DS</sub> = 400 V, see fig. 6 and 13 <sup>b</sup>	-	-	38	nC
Gate-source charge	Q <sub>gs</sub>			-	-	9.0	
Gate-drain charge	Q <sub>gd</sub>			-	-	18	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 8 A R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 31 Ω, see fig. 10 <sup>b</sup>		-	11	-	ns
Rise time	t <sub>r</sub>			-	23	-	
Turn-off delay time	t <sub>d(off)</sub>			-	26	-	
Fall time	t <sub>f</sub>			-	19	-	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.7	-	3.7	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	8.0	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	32	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 8 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.0	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 8 A, dI/dt = 100 A/μs <sup>b</sup>		-	422	633	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	2.16	3.24	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

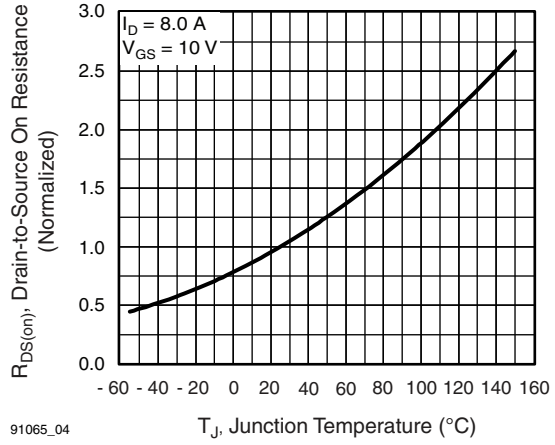
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
- c. C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DS</sub>

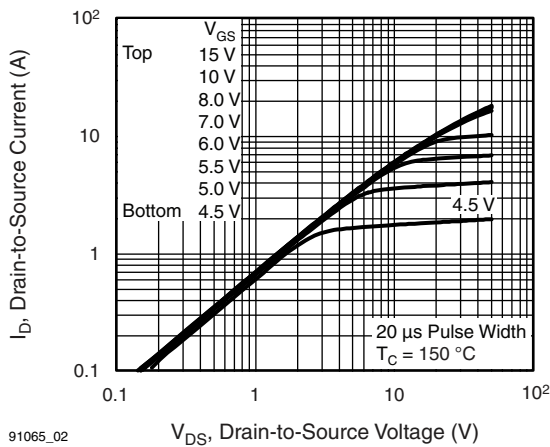
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



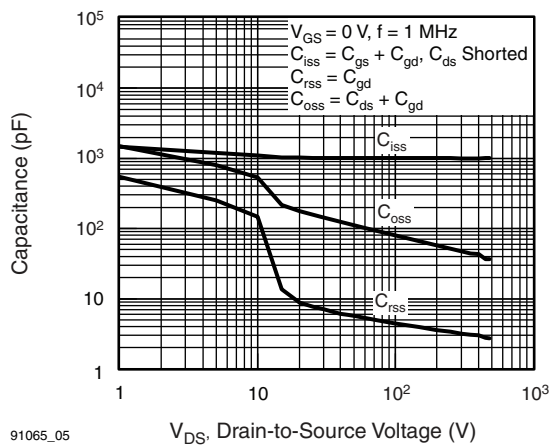
**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



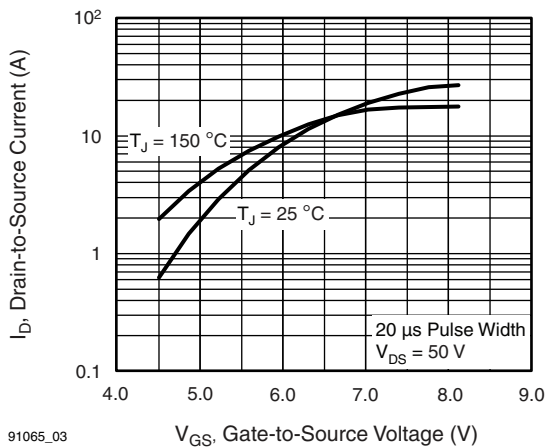
**Fig. 4 - Normalized On-Resistance vs. Temperature**



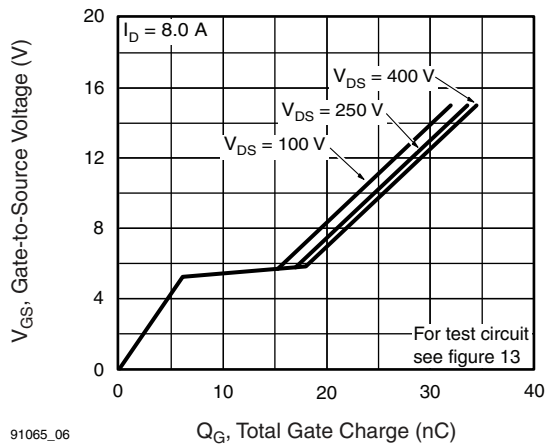
**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**



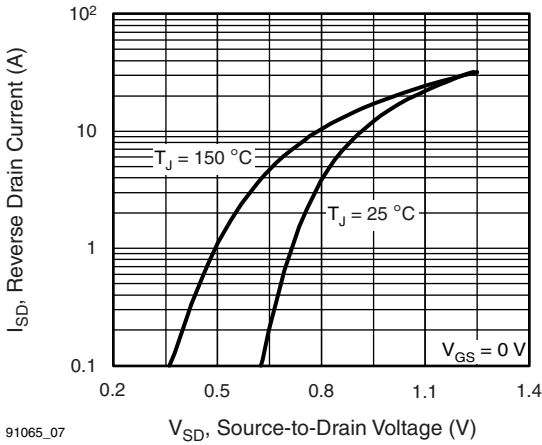
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**

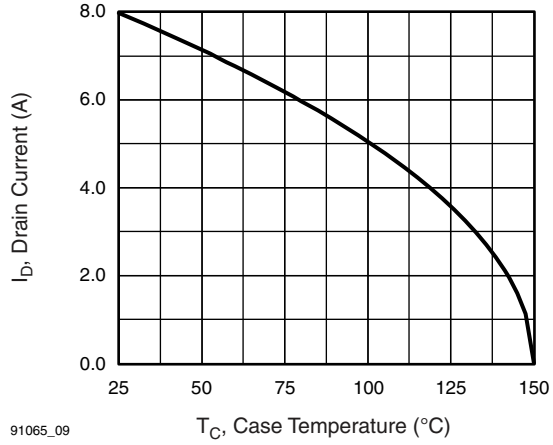


**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



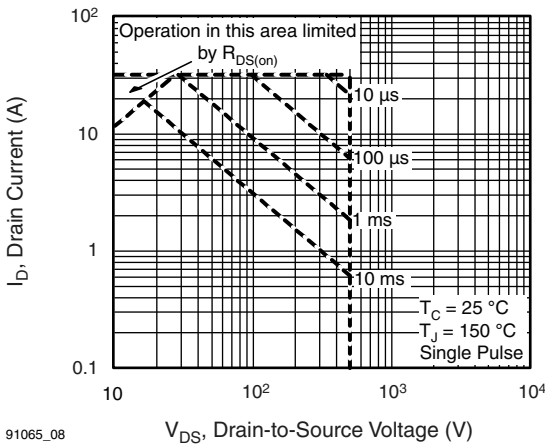
91065\_07

Fig. 7 - Typical Source-Drain Diode Forward Voltage



91065\_09

Fig. 9 - Maximum Drain Current vs. Case Temperature



91065\_08

Fig. 8 - Maximum Safe Operating Area

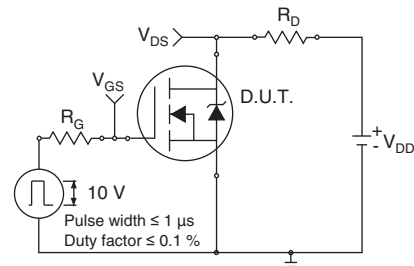


Fig. 10a - Switching Time Test Circuit

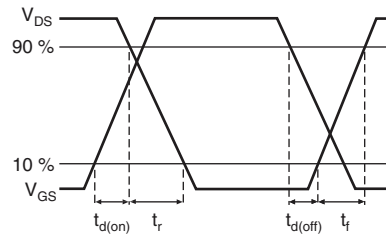
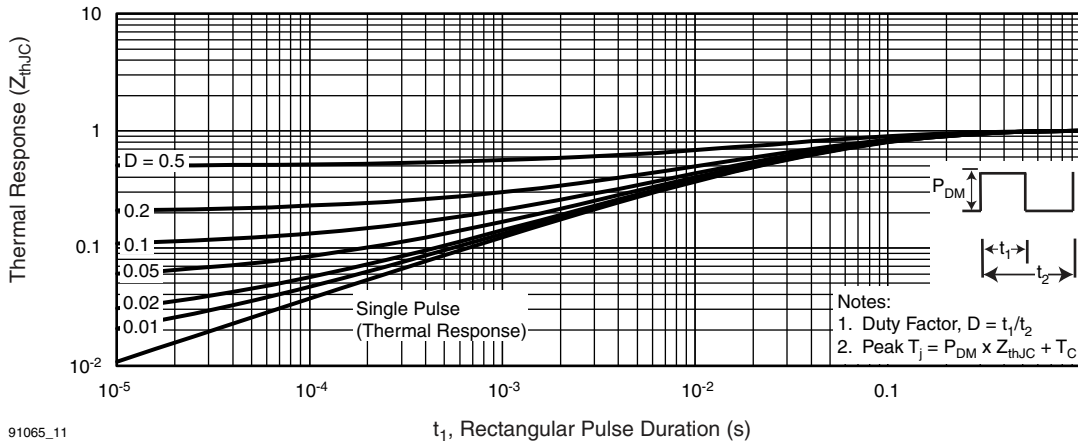


Fig. 10b - Switching Time Waveforms



91065\_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

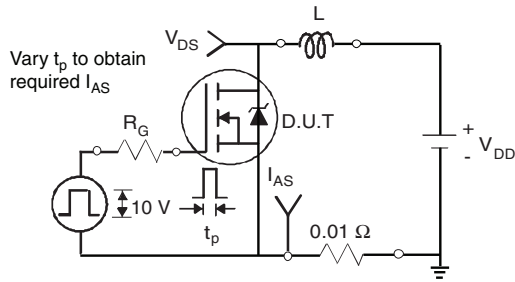


Fig. 12a - Unclamped Inductive Test Circuit

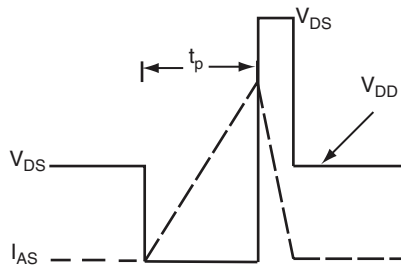


Fig. 12b - Unclamped Inductive Waveforms

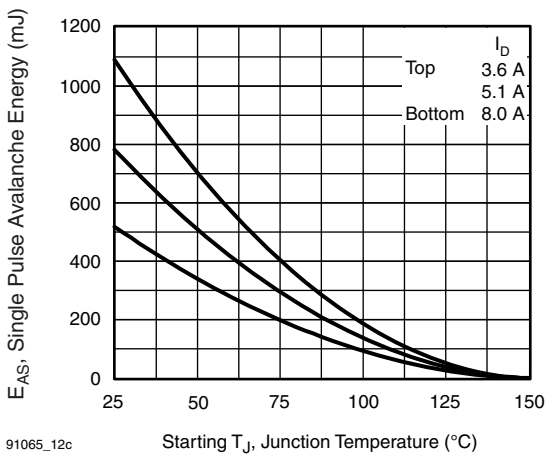


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

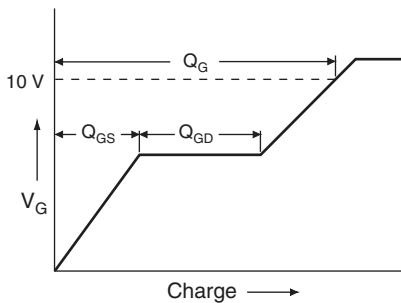


Fig. 12d - Basic Gate Charge Waveform

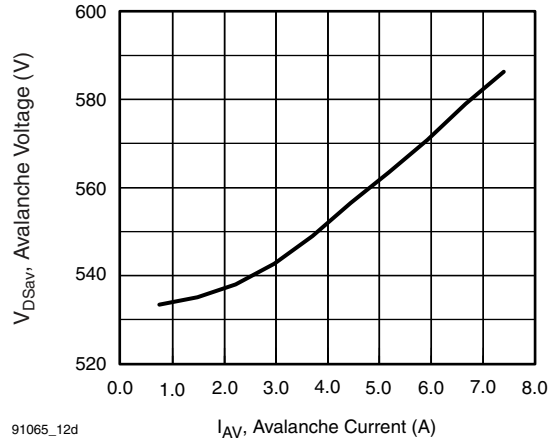


Fig. 13a - Typical Drain-to-Source Voltage vs. Avalanche Current

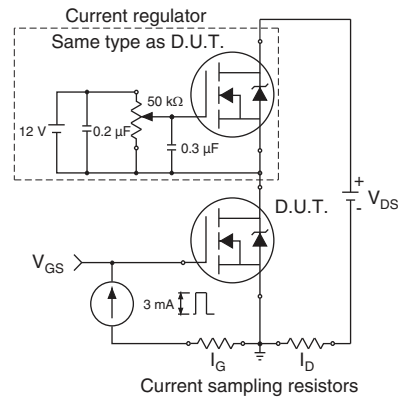
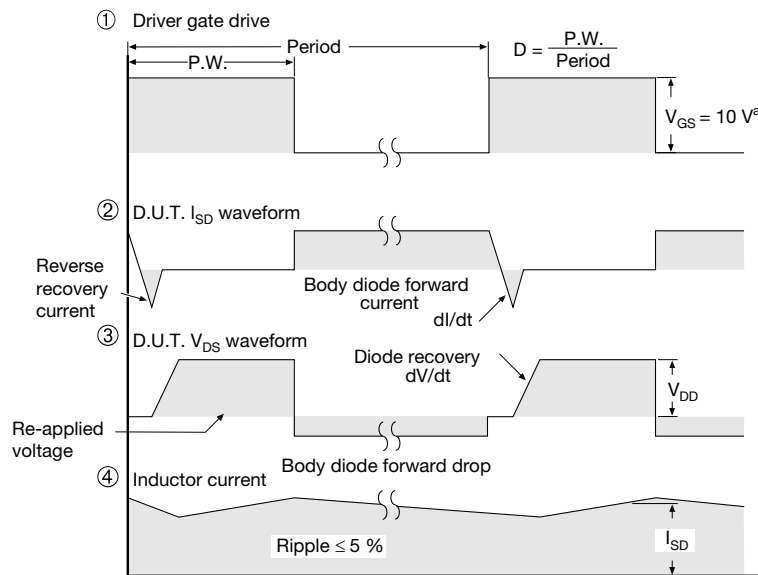
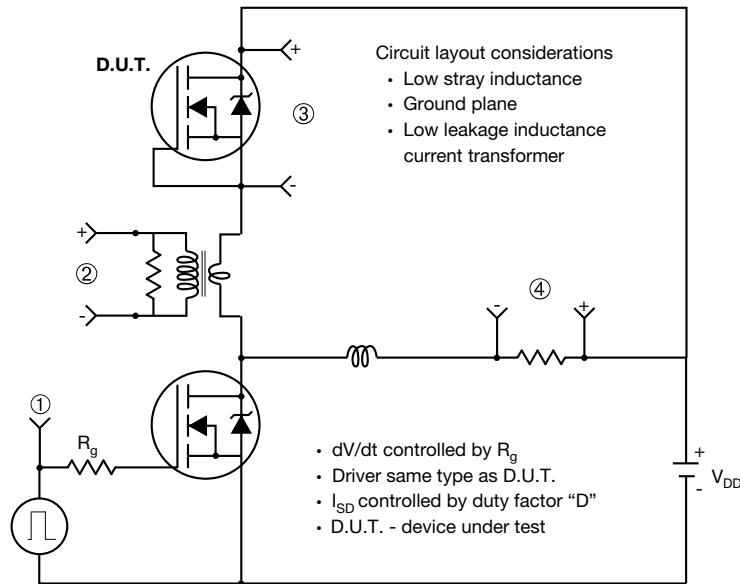


Fig. 13b - Gate Charge Test Circuit

91065\_12c

91065\_12d

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel

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