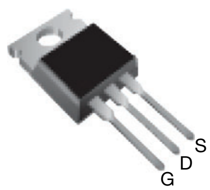
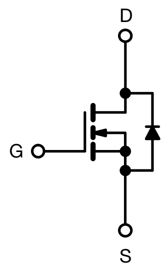
Power MOSFET

TO-220AB





N-Channel MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	250	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	1.1
Q_g max. (nC)	14	
Q_{gs} (nC)	2.7	
Q_{gd} (nC)	7.8	
Configuration	Single	

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb Available
RoHS* Available
HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF624PbF
Lead (Pb)-free and halogen-free	IRF624PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	250	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	T_C = 25 °C	I_D	4.4	A
		T_C = 100 °C		2.8	
Pulsed drain current [a]			I_{DM}	14	
Linear derating factor				0.40	W/°C
Single pulse avalanche energy [b]			E_{AS}	100	mJ
Repetitive avalanche current [a]			I_{AR}	4.4	A
Repetitive avalanche energy [a]			E_{AR}	5.0	mJ
Maximum power dissipation	T_C = 25 °C		P_D	50	W
Peak diode recovery dV/dt [c]			dV/dt	4.8	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d]	For 10 s			300	
Mounting torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

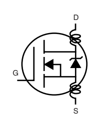
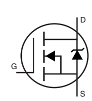
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = 50 V, starting T_J = 25 °C, L = 8.3 mH, R_g = 25 Ω, I_{AS} = 4.4 A (see fig. 12)

c. $I_{SD} \leq 4.4$ A, dI/dt ≤ 90 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C

d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	2.5	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		250	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.36	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V		-	-	25	μA
		V_{DS} = 200 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 2.6 A [b]	-	-	1.1	Ω
Forward transconductance	g_{fs}	V_{DS} = 50 V, I_D = 2.6 A [b]		1.5	-	-	S
Dynamic							
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	260	-	pF
Output capacitance	C_{oss}			-	77	-	
Reverse transfer capacitance	C_{rss}			-	15	-	
Total gate charge	Q_g	V_{GS} = 10 V	I_D = 4.4 A, V_{DS} = 200 V, see fig. 6 and 13 [b]	-	-	14	nC
Gate-source charge	Q_{gs}			-	-	2.7	
Gate-drain charge	Q_{gd}			-	-	7.8	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 125 V, I_D = 4.4 A, R_g = 18 Ω, R_D = 28 Ω, see fig. 10 [b]		-	7.0	-	ns
Rise time	t_r			-	13	-	
Turn-off delay time	$t_{d(off)}$			-	20	-	
Fall time	t_f			-	12	-	
Gate input resistance	R_g	f = 1 MHz, open drain		0.7	-	5.4	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.4	A
Pulsed diode forward current [a]	I_{SM}			-	-	14	
Body diode voltage	V_{SD}	T_J = 25 °C, I_S = 4.4 A, V_{GS} = 0 V [b]		-	-	1.8	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = 4.4 A, dI/dt = 100 A/μs [b]		-	200	400	ns
Body diode reverse recovery charge	Q_{rr}			-	0.93	1.9	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

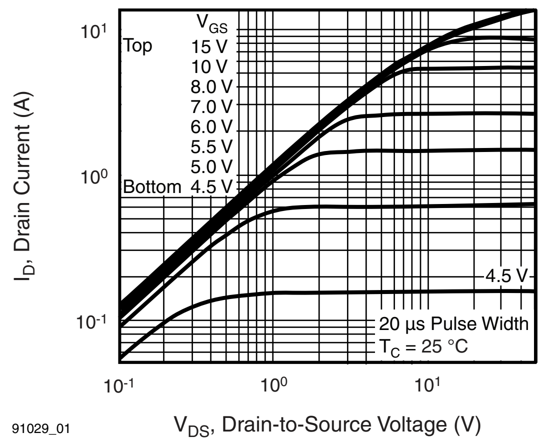


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

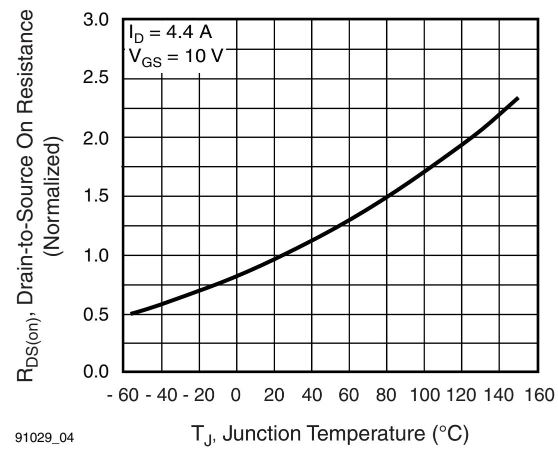


Fig. 4 - Normalized On-Resistance vs. Temperature

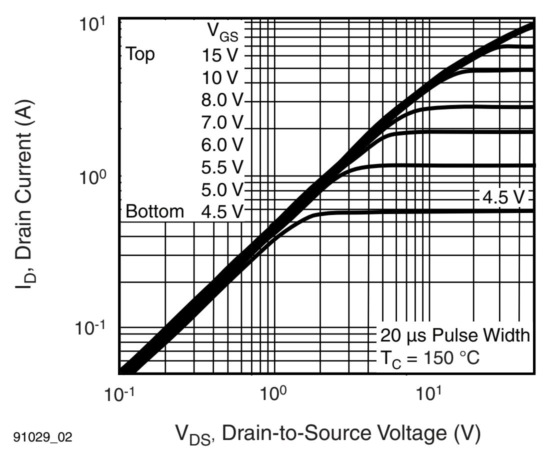


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

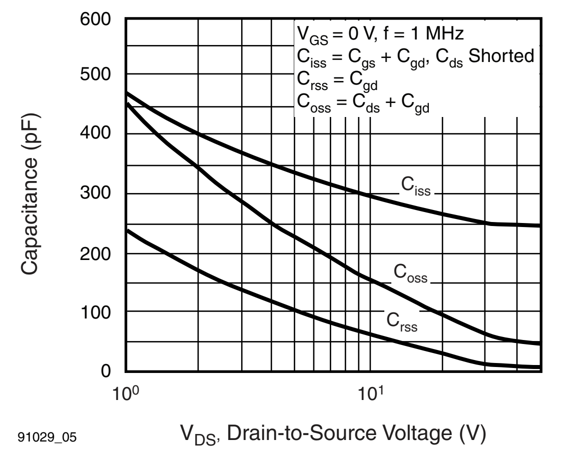


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

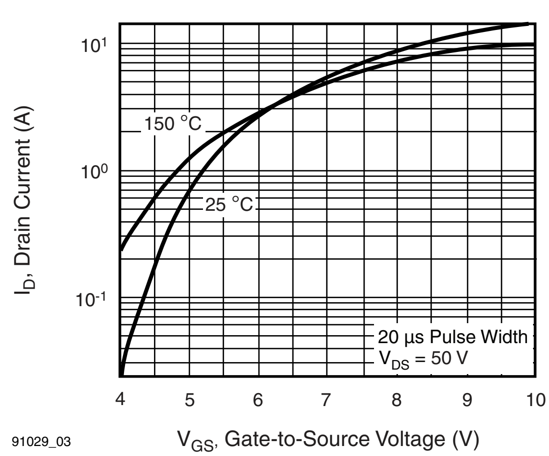


Fig. 3 - Typical Transfer Characteristics

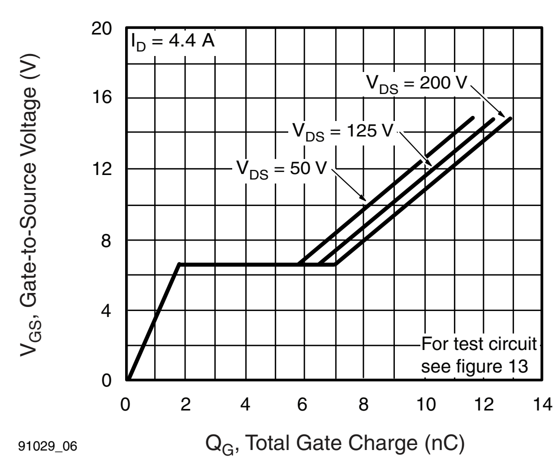


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

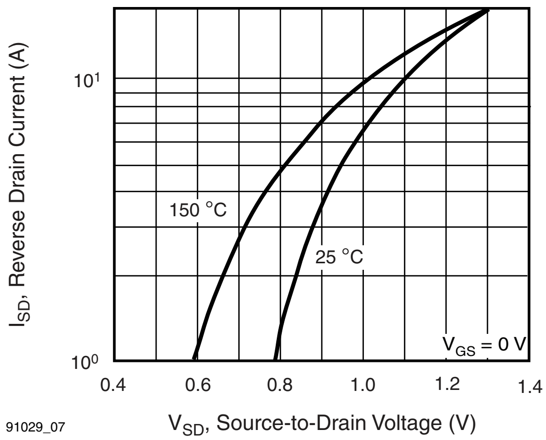


Fig. 7 - Typical Source-Drain Diode Forward Voltage

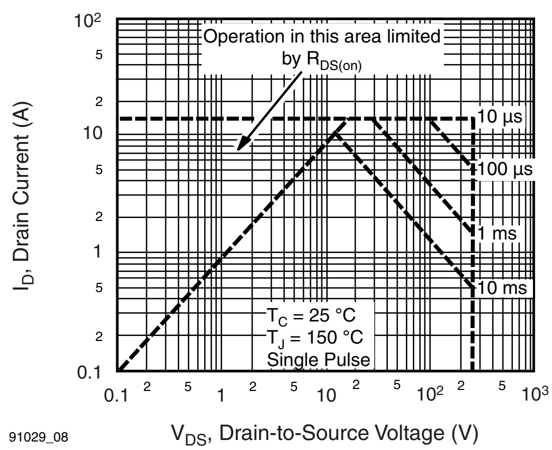


Fig. 8 - Maximum Safe Operating Area

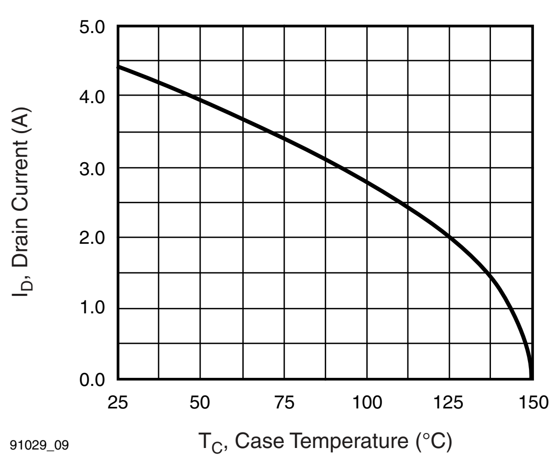


Fig. 9 - Maximum Drain Current vs. Case Temperature

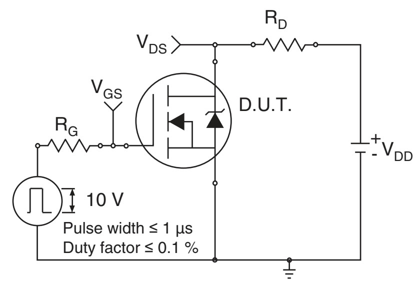


Fig. 10a - Switching Time Test Circuit

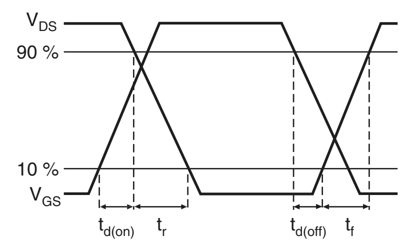


Fig. 10b - Switching Time Waveforms

For technical questions, contact: hvm@vishay.com

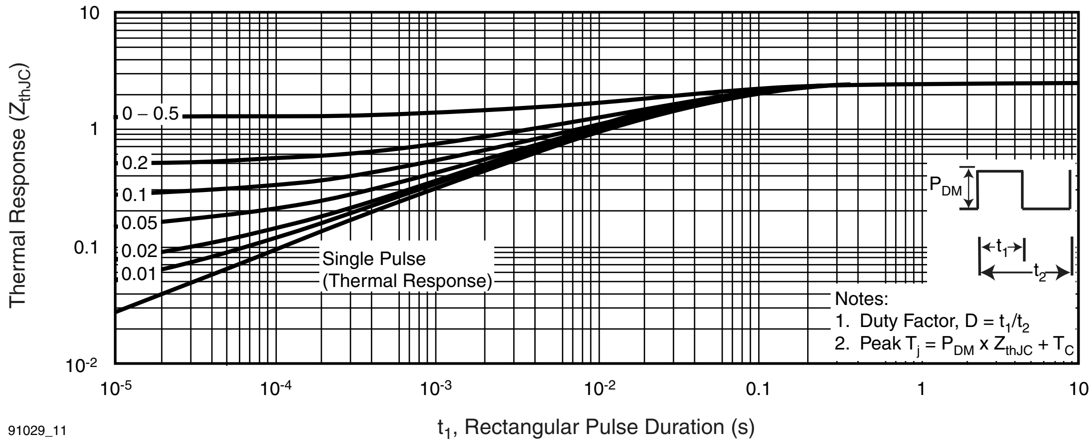


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

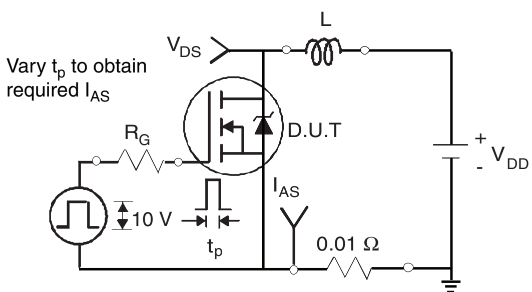


Fig. 12a - Unclamped Inductive Test Circuit

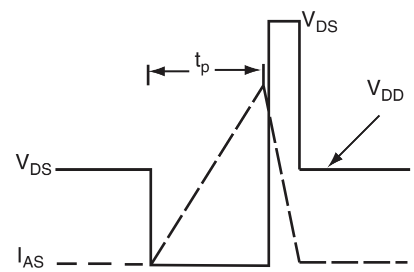


Fig. 12b - Unclamped Inductive Waveforms

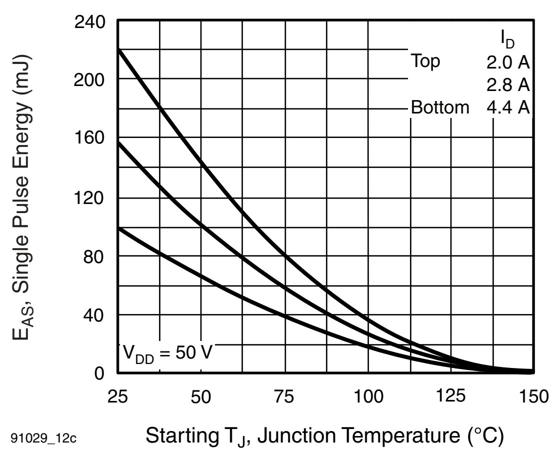


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

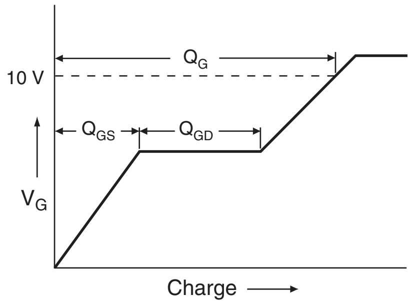


Fig. 13a - Basic Gate Charge Waveform

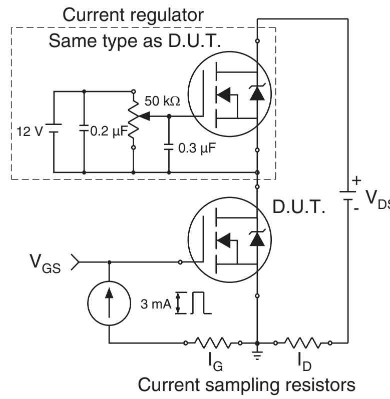
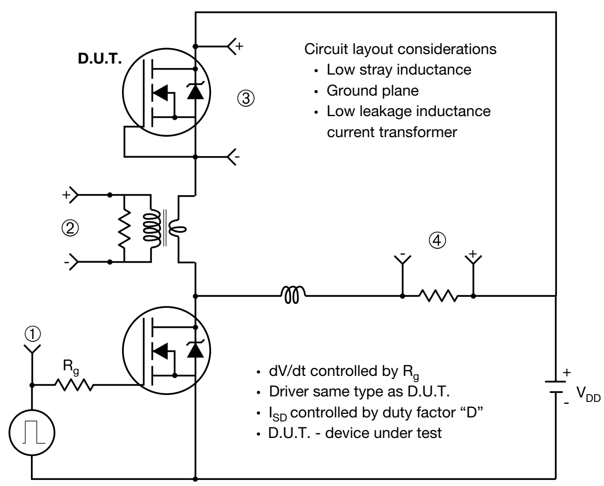
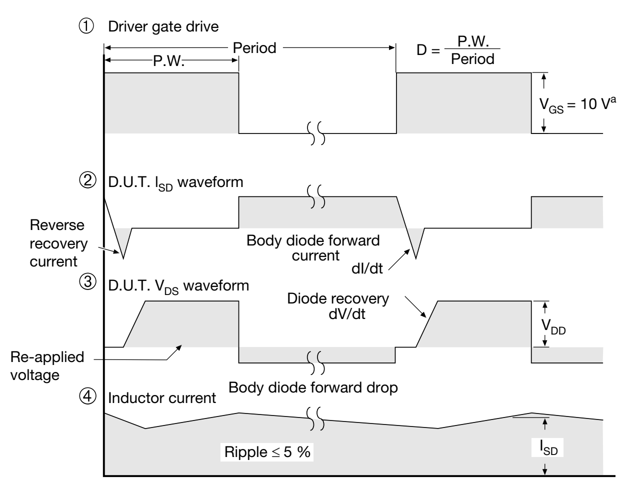


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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