

Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET



RoHS*
Available
HALOGEN FREE
Available

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the D²PAK (TO-263) contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY

V _{DS} (V)	900	
R _{DS(on)} (Ω)	V _{GS} = 10 V	3.7
Q _g max. (nC)	78	
Q _{gs} (nC)	10	
Q _{gd} (nC)	42	
Configuration	Single	

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF30S-GE3	-
Lead (Pb)-free	IRFBF30STRLPbF	IRFBF30STRRPbF

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V _{DS}	900	V	
Gate-source voltage	V _{GS}	± 20		
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C	A	
		T _C = 100 °C		2.3
Pulsed drain current ^a	I _{DM}	14		
Linear derating factor		1.0	W/°C	
Single pulse avalanche energy ^b	E _{AS}	250	mJ	
Repetitive avalanche current ^a	I _{AR}	3.6	A	
Repetitive avalanche energy ^a	E _{AR}	13	mJ	
Maximum power dissipation	T _C = 25 °C	P _D	125	W
Peak diode recovery dV/dt ^c		dV/dt	1.5	V/ns
Operating junction and storage temperature range	T _J , T _{stg}		-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s		300	

Notes

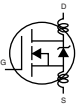

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = 50 V, starting T_J = 25 °C, L = 36 mH, R_g = 25 Ω, I_{AS} = 3.6 A (see fig. 12)
- I_{SD} ≤ 3.6 A, dI/dt ≤ 70 A/μs, V_{DD} ≤ 600, T_J ≤ 150 °C
- 1.6 mm from case



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-ambient (PCB mount) ^a	R_{thJA}	-	40	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	900	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	1.1	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}$	-	-	100	μA
		$V_{DS} = 720\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 2.2\text{ A}^b$	-	-	3.7	Ω
Forward transconductance	g_{fs}	$V_{DS} = 100\text{ V}, I_D = 2.2\text{ A}^b$	2.3	-	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$	-	1200	-	μF
Output capacitance	C_{oss}		-	320	-	
Reverse transfer capacitance	C_{rss}		-	200	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 3.6\text{ A}, V_{DS} = 360\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	78	nC
Gate-source charge	Q_{gs}		-	-	10	
Gate-drain charge	Q_{gd}		-	-	42	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 450\text{ V}, I_D = 3.6\text{ A}, R_g = 12\text{ }\Omega, R_D = 120\text{ }\Omega, \text{ see fig. 10}^b$	-	14	-	ns
Rise time	t_r		-	25	-	
Turn-off delay time	$t_{d(off)}$		-	90	-	
Fall time	t_f		-	30	-	
Gate input resistance	R_g	$f = 1\text{ MHz}, \text{ open drain}$	0.4	-	2.0	Ω
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	3.6	A
Pulsed diode forward current ^a	I_{SM}		-	-	14	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 3.6\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.8	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 3.6\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	430	650	ns
Body diode reverse recovery charge	Q_{rr}		-	1.4	2.1	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\text{ }\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

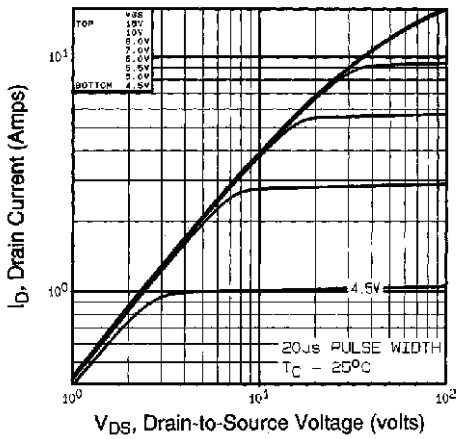


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

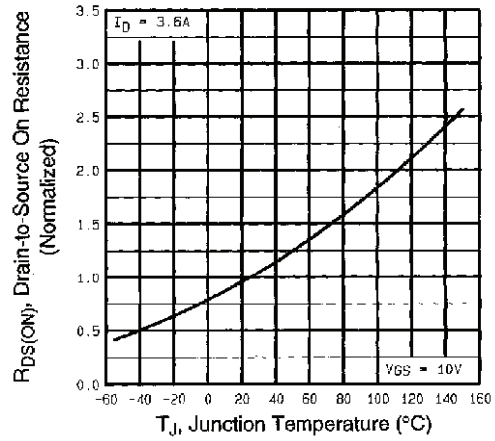


Fig. 4 - Normalized On-Resistance vs. Temperature

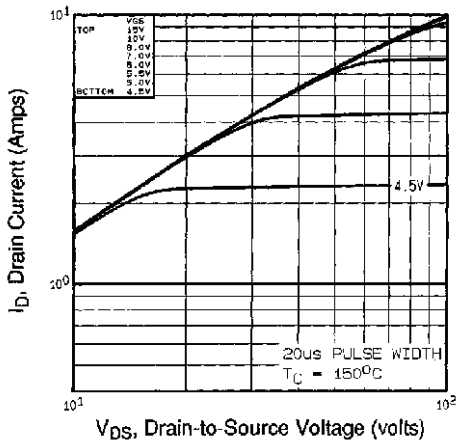


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

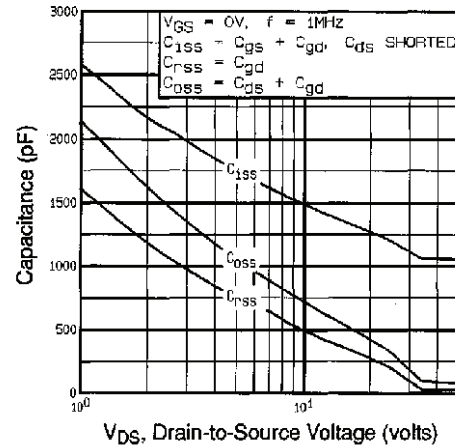


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

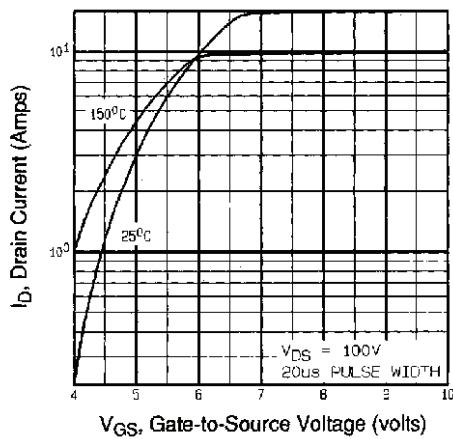


Fig. 3 - Typical Transfer Characteristics

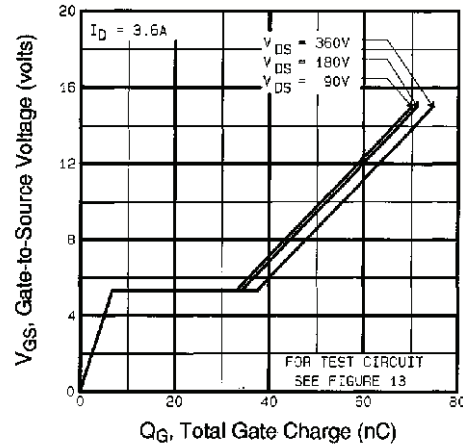


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

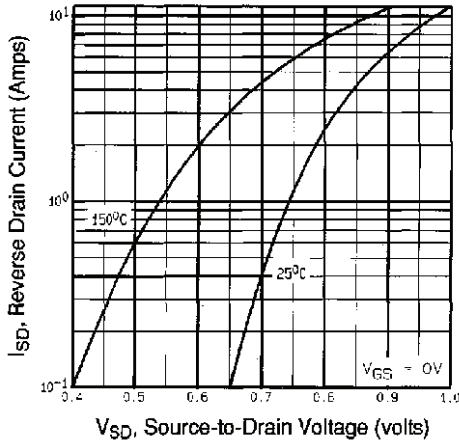


Fig. 7 - Typical Source-Drain Diode Forward Voltage

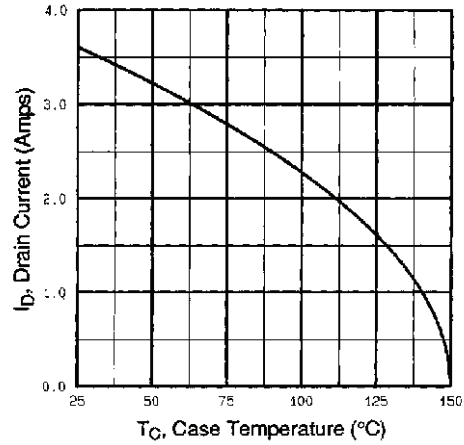


Fig. 9 - Maximum Drain Current vs. Case Temperature

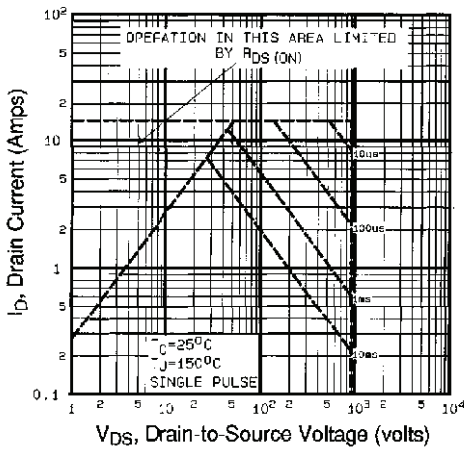


Fig. 8 - Maximum Safe Operating Area

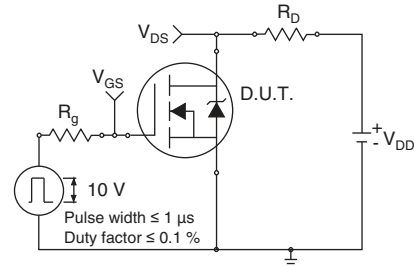


Fig. 10 - Switching Time Test Circuit

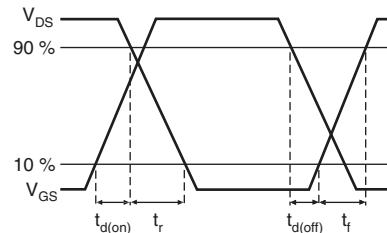


Fig. 11 - Switching Time Waveforms

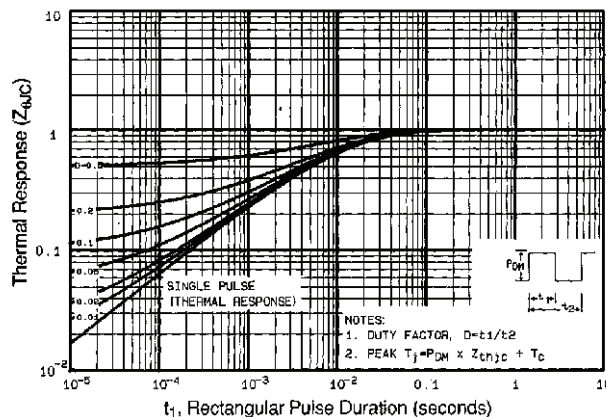


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

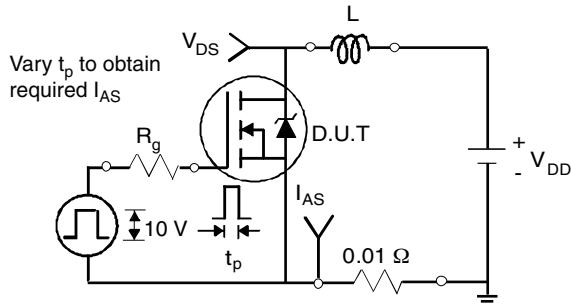


Fig. 13 - Unclamped Inductive Test Circuit

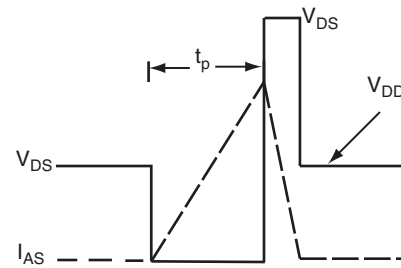


Fig. 14 - Unclamped Inductive Waveforms

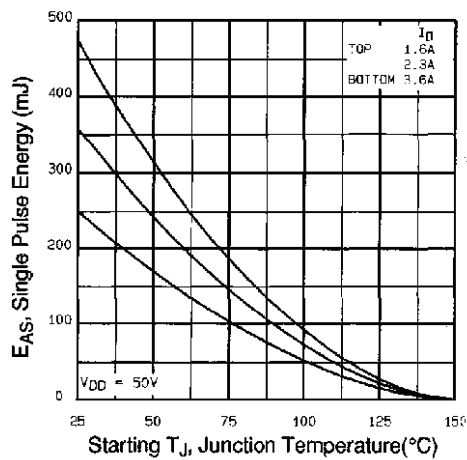


Fig. 15 - Maximum Avalanche Energy vs. Drain Current

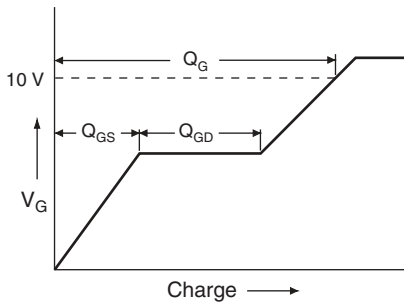


Fig. 16 - Basic Gate Charge Waveform

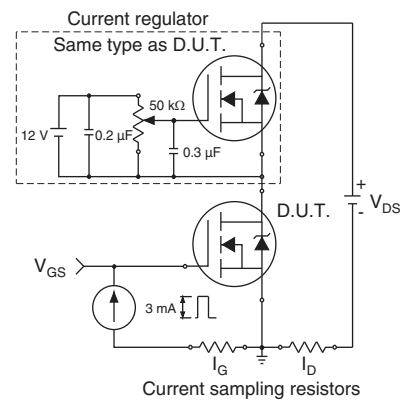
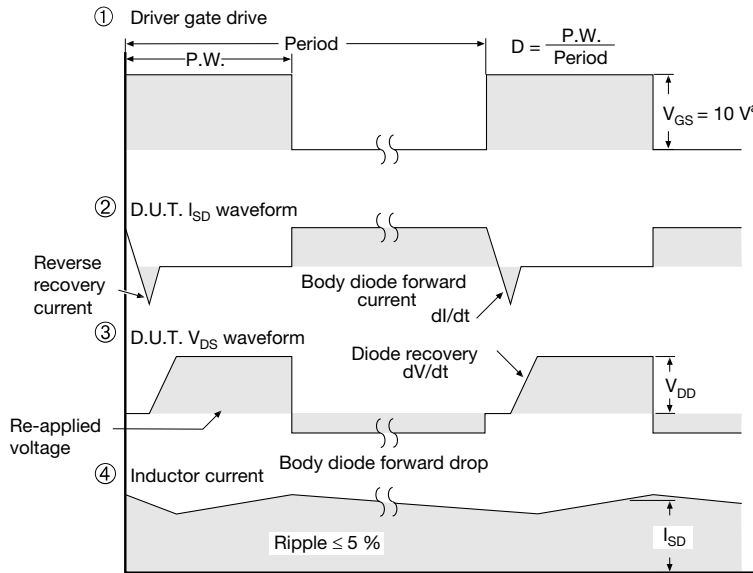
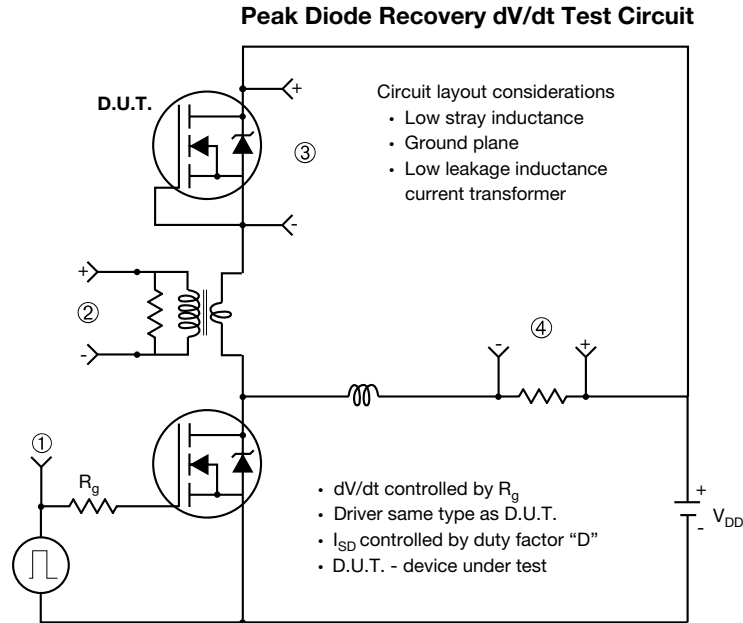


Fig. 17 - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 18 - For N-Channel

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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