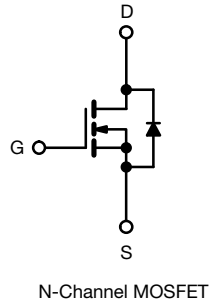
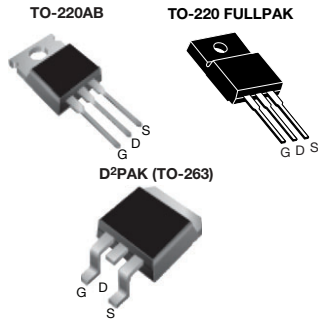


Power MOSFET



FEATURES

- Low figure-of-merit $R_{on} \times Q_g$
- 100 % avalanche tested
- Gate charge improved
- t_{rr}/Q_{rr} improved
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY

| | | |
|----------------------------|-----------------|------|
| V_{DS} (V) at T_J max. | 560 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10$ V | 0.38 |
| Q_g (Max.) (nC) | 68 | |
| Q_{gs} (nC) | 17.6 | |
| Q_{gd} (nC) | 21.8 | |
| Configuration | Single | |

ORDERING INFORMATION

| Package | TO-220AB | D ² PAK (TO-263) | TO-220 FULLPAK |
|---------------------------------|----------------|-----------------------------|----------------|
| | SiHP16N50C-E3 | SiHB16N50C-E3 | SiHF16N50C-E3 |
| Lead (Pb)-free | - | SiHB16N50CTR-E3 | - |
| | - | SiHB16N50CTL-E3 | - |
| Lead (Pb)-free and halogen-free | SiHP16N50C-BE3 | - | - |

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

| PARAMETER | SYMBOL | LIMIT | UNIT | |
|---|---------------------------------------|----------------|------|---|
| Drain-source voltage | V_{DS} | 500 | V | |
| Gate-source voltage | V_{GS} | ± 30 | | |
| Continuous drain current ($T_J = 150$ °C) ^a | V_{GS} at 10 V | $T_C = 25$ °C | 16 | A |
| | | $T_C = 100$ °C | 10 | |
| Pulsed drain current ^c | I_{DM} | 40 | | |
| Linear derating factor | | 2 | W/°C | |
| Single pulse avalanche energy ^b | E_{AS} | 320 | mJ | |
| Maximum power dissipation | TO220-AB, D ² PAK (TO-263) | 250 | W | |
| | TO-220 FULLPAK | 38 | | |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +150 | °C | |
| Soldering recommendations (peak temperature) ^d | For 10 s | 300 | | |

Notes


- Limited by maximum junction temperature
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.5$ mH, $R_g = 25$ Ω , $I_{AS} = 16$ A
- Repetitive rating; pulse width limited by maximum junction temperature
- 1.6 mm from case



| THERMAL RESISTANCE RATINGS | | | | |
|--|-------------------|--------------------------------------|----------------|------|
| PARAMETER | SYMBOL | TO220-AB D ² PAK (TO-263) | TO-220 FULLPAK | UNIT |
| Maximum junction-to-ambient | R _{thJA} | 62 | 65 | °C/W |
| Maximum junction-to-case (drain) | R _{thJC} | 0.5 | 3.3 | |
| Junction-to-ambient (PCB mount) ^a | R _{thJA} | 40 | - | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|---|----------------------------------|---|------|------|-------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-source breakdown voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | 500 | - | - | V |
| V _{DS} temperature coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | - | 0.6 | - | V/°C |
| Gate-source threshold voltage (N) | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 3.0 | - | 5.0 | V |
| Gate-source leakage | I _{GSS} | V _{GS} = ± 30 V | - | - | ± 100 | nA |
| Zero gate voltage drain current | I _{DSS} | V _{DS} = 500 V, V _{GS} = 0 V | - | - | 50 | μA |
| | | V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C | - | - | 250 | |
| Drain-source on-state resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 8 A | - | 0.31 | 0.38 | Ω |
| Forward transconductance ^a | g _{fs} | V _{DS} = 50 V, I _D = 3 A | - | 3 | - | S |
| Dynamic | | | | | | |
| Input capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz | - | 1900 | - | pF |
| Output capacitance | C _{oss} | | - | 230 | - | |
| Reverse transfer capacitance | C _{rss} | | - | 24 | - | |
| Total gate charge | Q _g | V _{GS} = 10 V, I _D = 16 A, V _{DS} = 400 V | - | 45 | 68 | nC |
| Gate-source charge | Q _{gs} | | - | 18 | - | |
| Gate-drain charge | Q _{gd} | | - | 22 | - | |
| Turn-on delay time | t _{d(on)} | V _{DD} = 250 V, I _D = 16 A, R _g = 9.1 Ω, V _{GS} = 10 V | - | 27 | - | ns |
| Rise time | t _r | | - | 156 | - | |
| Turn-off delay time | t _{d(off)} | | - | 29 | - | |
| Fall time | t _f | | - | 31 | - | |
| Gate input resistance | R _g | f = 1 MHz, open drain | - | 1.6 | - | Ω |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous source-drain diode current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 16 | A |
| Pulsed diode forward current | I _{SM} | | - | - | 30 | |
| Body diode voltage | V _{SD} | T _J = 25 °C, I _S = 10 A, V _{GS} = 0 V | - | - | 1.8 | V |
| Body diode reverse recovery time | t _{rr} | T _J = 25 °C, I _F = I _S , dI/dt = 100 A/μs, V _R = 20 V | - | 555 | - | ns |
| Body diode reverse recovery charge | Q _{rr} | | - | 5.5 | - | μC |
| Body diode reverse recovery current | I _{RRM} | | - | 18 | - | A |

Note

- The information shown here is a preliminary product proposal, not a commercial product data sheet. Vishay Siliconix is not committed to produce this or any similar product. This information should not be used for design purposes, nor construed as an offer to furnish or sell such products



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

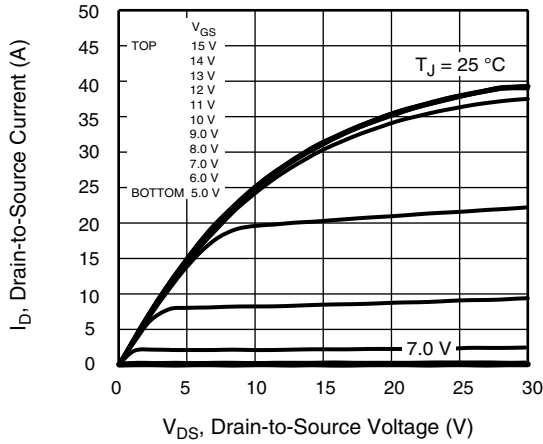


Fig. 1 - Typical Output Characteristics (TO-220)

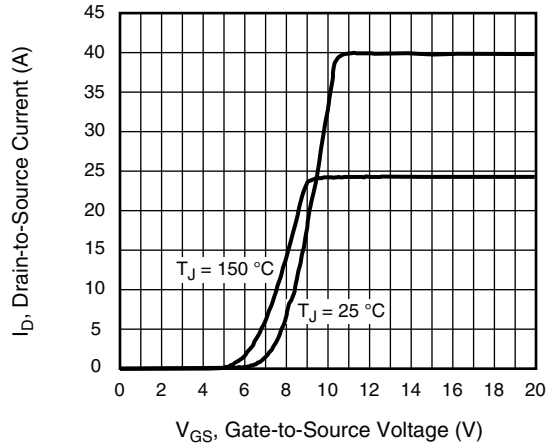


Fig. 3 - Typical Transfer Characteristics

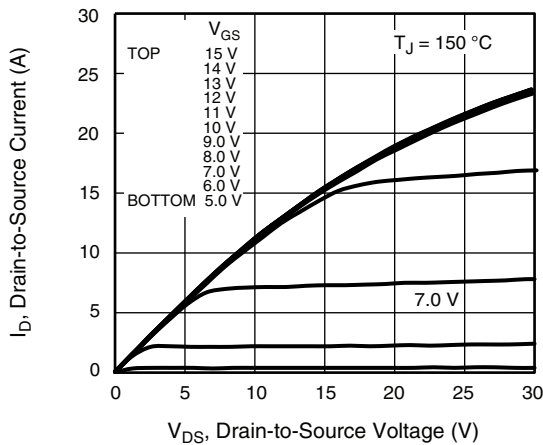


Fig. 2 - Typical Output Characteristics (TO-220)

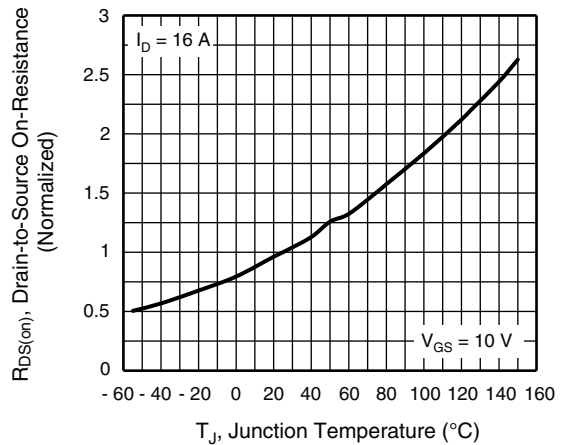


Fig. 4 - Normalized On-Resistance vs. Temperature

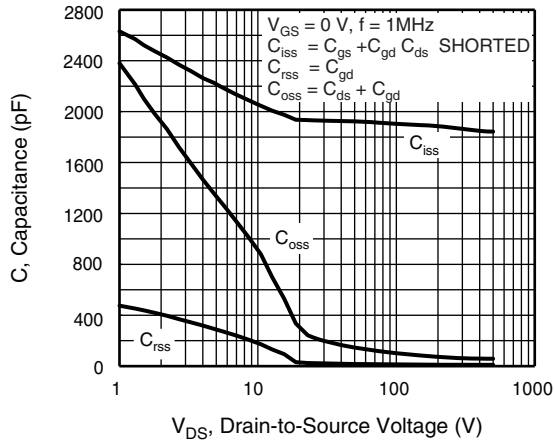


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

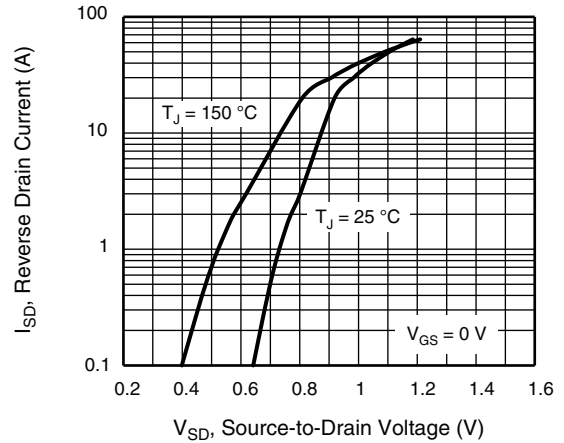


Fig. 7 - Typical Source-Drain Diode Forward Voltage

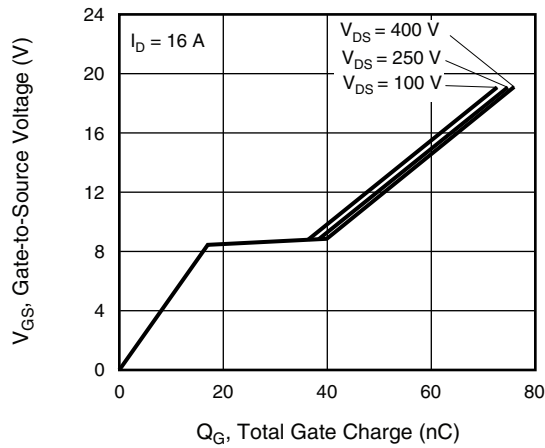


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

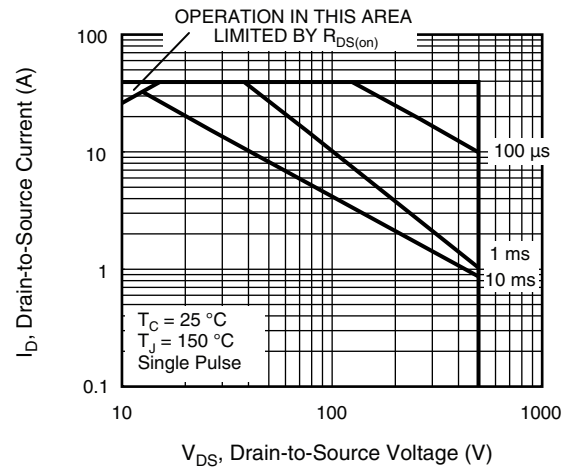


Fig. 1 - Maximum Safe Operating Area (TO-220AB, D²PAK)

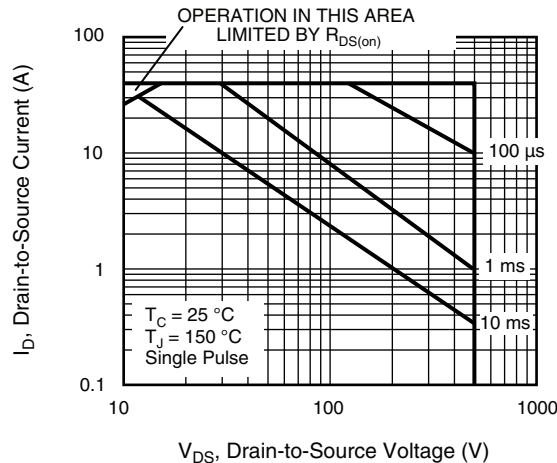


Fig. 2 - Maximum Safe Operating Area (TO-220 FULLPAK)

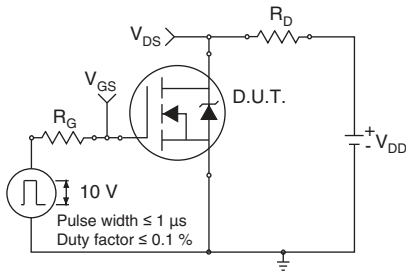


Fig. 10a - Switching Time Test Circuit

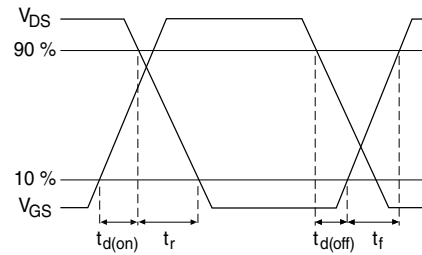


Fig. 10b - Switching Time Waveforms

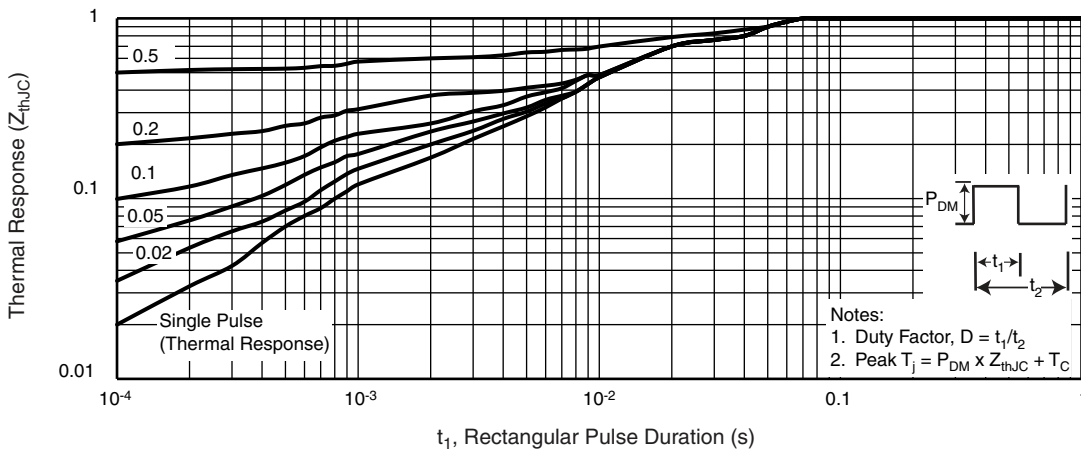


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220AB, D²PAK)

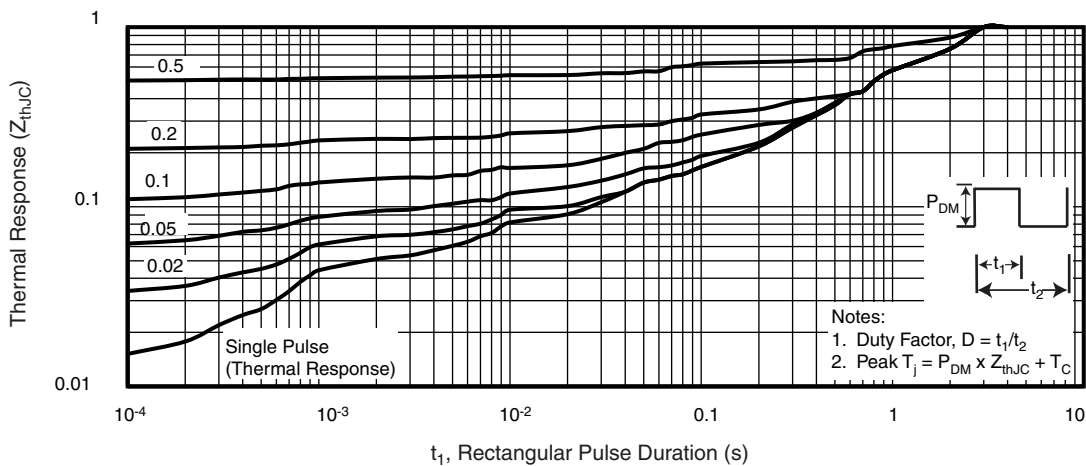


Fig. 3 - Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220 FULLPAK)

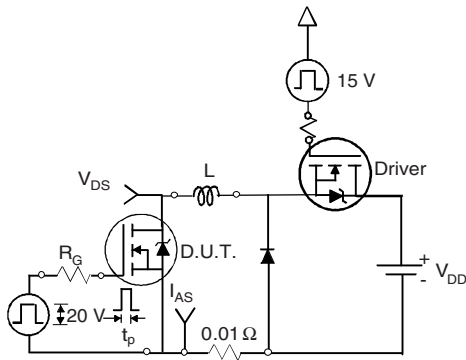


Fig. 13a - Unclamped Inductive Test Circuit

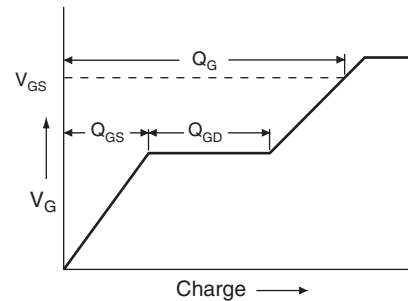


Fig. 14a - Basic Gate Charge Waveform

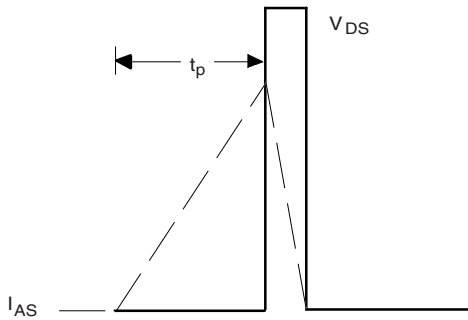


Fig. 13b - Unclamped Inductive Waveforms

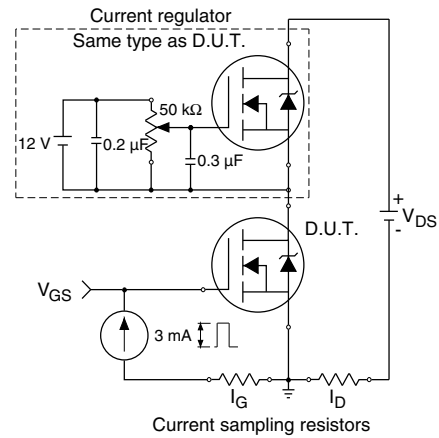
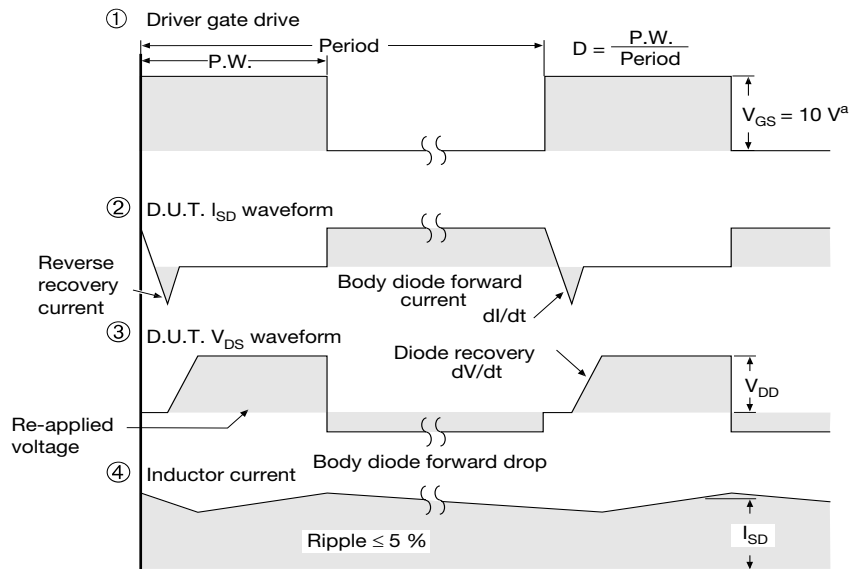
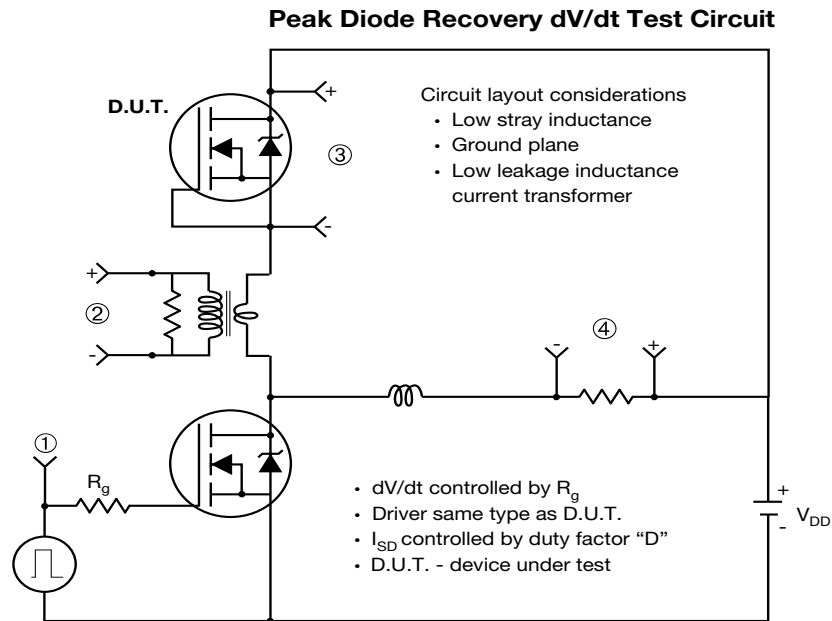


Fig. 14b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 15 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



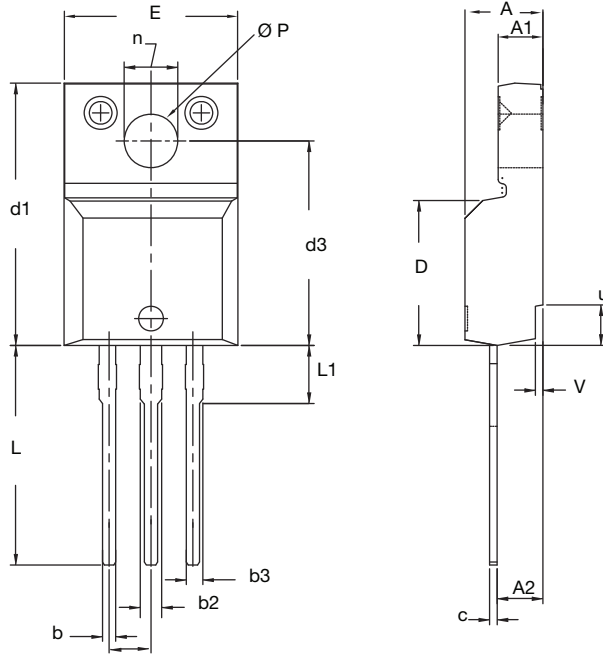
| DIM. | MILLIMETERS | | |
|-----------------|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 4.60 | 4.70 | 4.80 |
| b | 0.70 | 0.80 | 0.91 |
| b1 | 1.20 | 1.30 | 1.47 |
| b2 | 1.10 | 1.20 | 1.30 |
| C | 0.45 | 0.50 | 0.63 |
| D | 15.80 | 15.87 | 15.97 |
| e | 2.54 BSC | | |
| E | 10.00 | 10.10 | 10.30 |
| F | 2.44 | 2.54 | 2.64 |
| G | 6.50 | 6.70 | 6.90 |
| L | 12.90 | 13.10 | 13.30 |
| L1 | 3.13 | 3.23 | 3.33 |
| Q | 2.65 | 2.75 | 2.85 |
| Q1 | 3.20 | 3.30 | 3.40 |
| $\varnothing R$ | 3.08 | 3.18 | 3.28 |

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking



OPTION 2: FACILITY CODE = Y



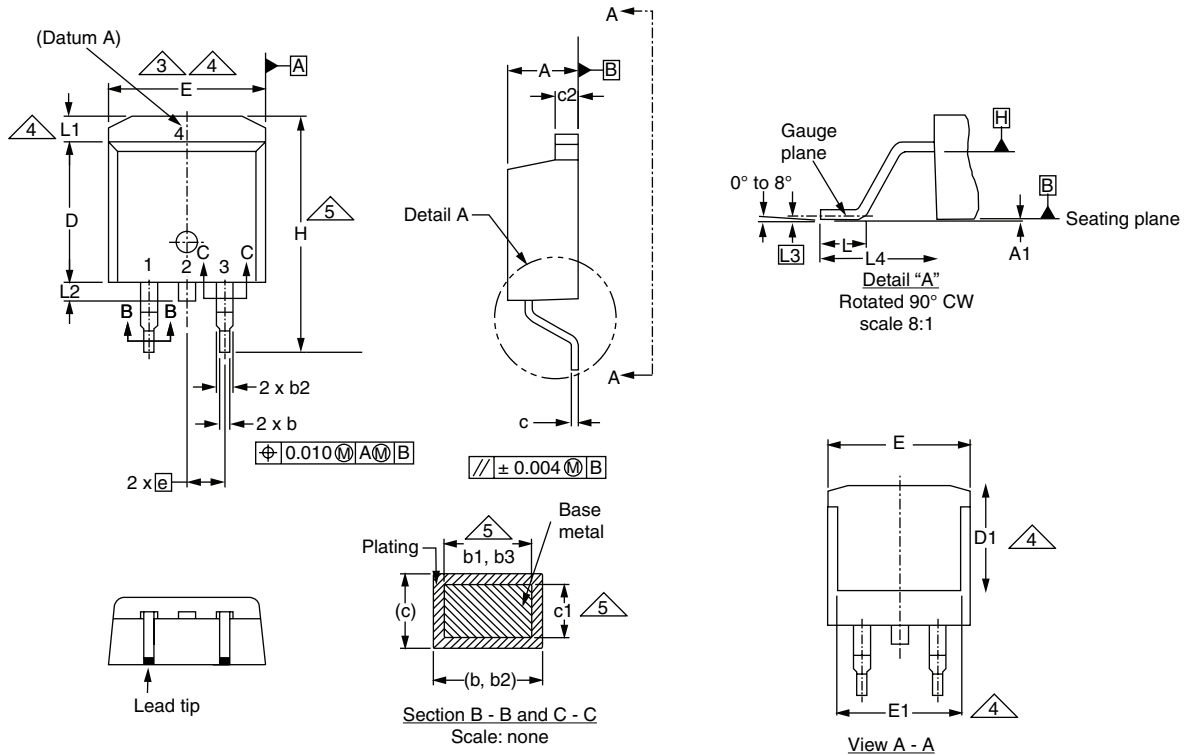
| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|--------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.570 | 4.830 | 0.180 | 0.190 |
| A1 | 2.570 | 2.830 | 0.101 | 0.111 |
| A2 | 2.510 | 2.850 | 0.099 | 0.112 |
| b | 0.622 | 0.890 | 0.024 | 0.035 |
| b2 | 1.229 | 1.400 | 0.048 | 0.055 |
| b3 | 1.229 | 1.400 | 0.048 | 0.055 |
| c | 0.440 | 0.629 | 0.017 | 0.025 |
| D | 8.650 | 9.800 | 0.341 | 0.386 |
| d1 | 15.88 | 16.120 | 0.622 | 0.635 |
| d3 | 12.300 | 12.920 | 0.484 | 0.509 |
| E | 10.360 | 10.630 | 0.408 | 0.419 |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.200 | 13.730 | 0.520 | 0.541 |
| L1 | 3.100 | 3.500 | 0.122 | 0.138 |
| n | 6.050 | 6.150 | 0.238 | 0.242 |
| Ø P | 3.050 | 3.450 | 0.120 | 0.136 |
| u | 2.400 | 2.500 | 0.094 | 0.098 |
| V | 0.400 | 0.500 | 0.016 | 0.020 |

ECN: E19-0180-Rev. D, 08-Apr-2019
DWG: 5972

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

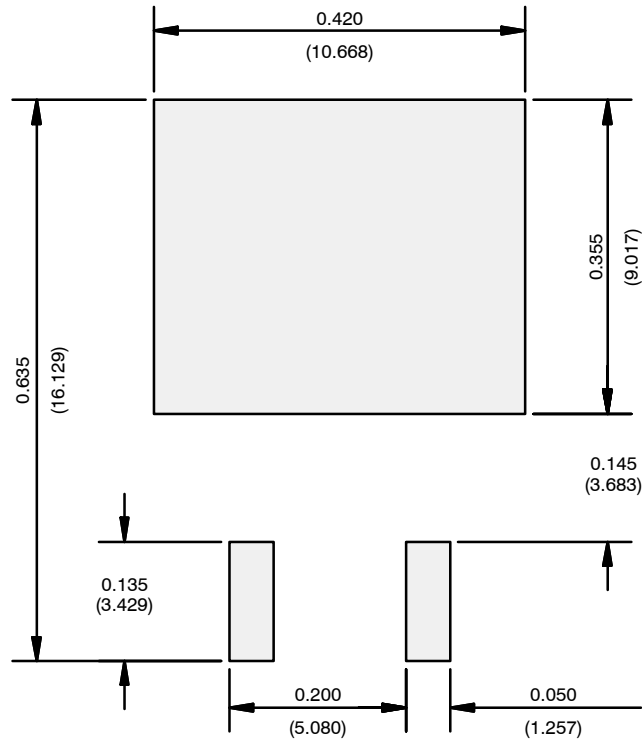
| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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