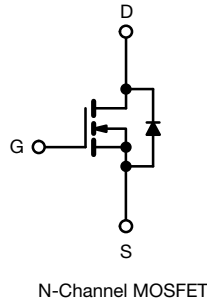
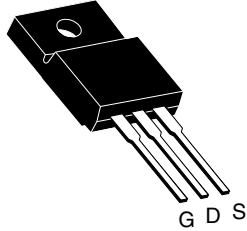


E Series Power MOSFET

TO-220 FULLPAK


FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

PRODUCT SUMMARY

| | | |
|---|-----------------|------|
| V_{DS} (V) at T_J max. | 700 | |
| $R_{DS(on)}$ max. (Ω) at 25 °C | $V_{GS} = 10$ V | 0.38 |
| Q_g max. (nC) | 70 | |
| Q_{gs} (nC) | 9 | |
| Q_{gd} (nC) | 16 | |
| Configuration | Single | |

ORDERING INFORMATION

| | |
|---------------------------------|----------------|
| Package | TO-220 FULLPAK |
| Lead (Pb)-free and Halogen-free | SiHF12N65E-GE3 |

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)


| PARAMETER | SYMBOL | LIMIT | UNIT |
|---|------------------|----------------|------|
| Drain-Source Voltage | V_{DS} | 650 | V |
| Gate-Source Voltage | V_{GS} | ± 30 | |
| Continuous Drain Current ($T_J = 150$ °C) ^e | V_{GS} at 10 V | $T_C = 25$ °C | 12 |
| | | $T_C = 100$ °C | 8 |
| Pulsed Drain Current ^a | I_{DM} | 28 | A |
| Linear Derating Factor | | 0.26 | |
| Single Pulse Avalanche Energy ^b | E_{AS} | 226 | mJ |
| Maximum Power Dissipation | P_D | 33 | W |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | °C |
| Drain-Source Voltage Slope | dV/dt | $T_J = 125$ °C | 37 |
| Reverse Diode dV/dt ^d | | 28 | |
| Soldering Recommendations (Peak temperature) ^c | For 10 s | 300 | °C |
| Mounting Torque | M3 screw | 0.6 | Nm |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.
- Limited by maximum junction temperature.



| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|-------------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R _{thJA} | - | 65 | °C/W |
| Maximum Junction-to-Case (Drain) | R _{thJC} | - | 3.8 | |

| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | | |
|---|----------------------------------|---|---|------|------|-------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | | 650 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | | - | 0.78 | - | V/°C |
| Gate-Source Threshold Voltage (N) | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 2 | - | 4 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 20 V | | - | - | ± 100 | nA |
| | | V _{GS} = ± 30 V | | - | - | ± 1 | μA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 650 V, V _{GS} = 0 V | | - | - | 1 | μA |
| | | V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C | | - | - | 10 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 6 A | - | 0.33 | 0.38 | Ω |
| Forward Transconductance | g _{fs} | V _{DS} = 30 V, I _D = 6 A | | - | 3.5 | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz | | - | 1224 | - | pF |
| Output Capacitance | C _{oss} | | | - | 65 | - | |
| Reverse Transfer Capacitance | C _{rss} | | | - | 4 | - | |
| Effective Output Capacitance, Energy Related ^a | C _{o(er)} | | | - | 50 | - | |
| Effective Output Capacitance, Time Related ^b | C _{o(tr)} | V _{DS} = 0 V to 520 V, V _{GS} = 0 V | | - | 160 | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V | I _D = 6 A, V _{DS} = 520 V | - | 35 | 70 | nC |
| Gate-Source Charge | Q _{gs} | | | - | 9 | - | |
| Gate-Drain Charge | Q _{gd} | | | - | 16 | - | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 520 V, I _D = 6 A, V _{GS} = 10 V, R _g = 9.1 Ω | | - | 16 | 32 | ns |
| Rise Time | t _r | | | - | 19 | 38 | |
| Turn-Off Delay Time | t _{d(off)} | | | - | 35 | 70 | |
| Fall Time | t _f | | | - | 18 | 36 | |
| Gate Input Resistance | R _g | f = 1 MHz, open drain | | - | 0.81 | - | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 12 | A |
| Pulsed Diode Forward Current | I _{SM} | | | - | - | 28 | |
| Diode Forward Voltage | V _{SD} | T _J = 25 °C, I _S = 6 A, V _{GS} = 0 V | | - | 1.0 | 1.2 | V |
| Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = I _S = 6 A, di/dt = 100 A/μs, V _R = 25 V | | - | 309 | 618 | ns |
| Reverse Recovery Charge | Q _{rr} | | | - | 3.8 | 7.6 | μC |
| Reverse Recovery Current | I _{RRM} | | | - | 21 | - | A |

Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.
- b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

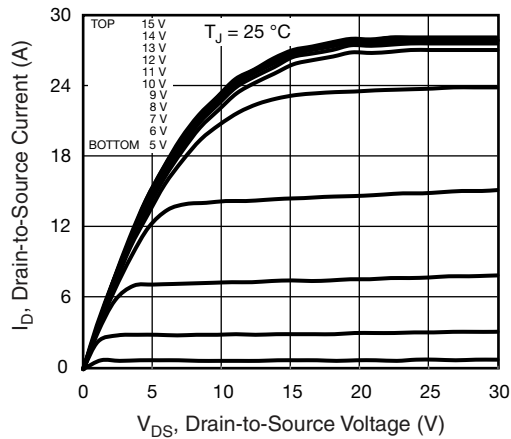


Fig. 1 - Typical Output Characteristics

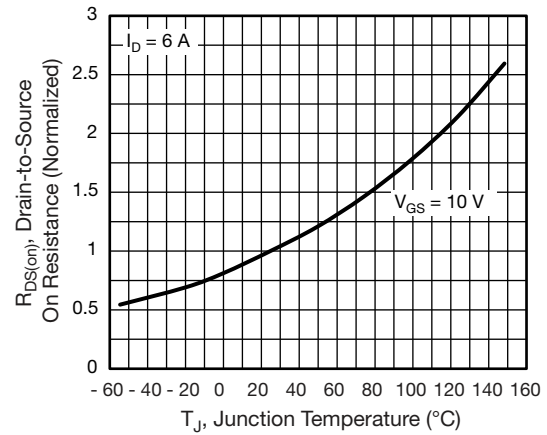


Fig. 4 - Normalized On-Resistance vs. Temperature

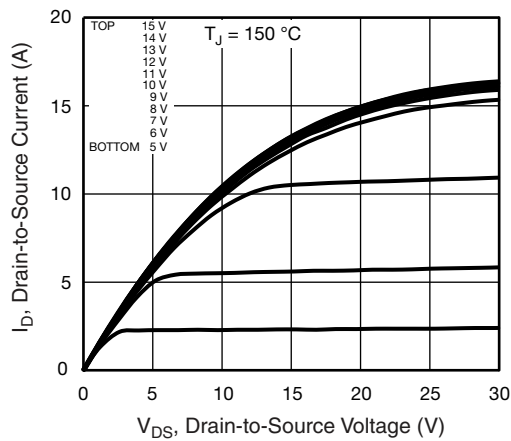


Fig. 2 - Typical Output Characteristics

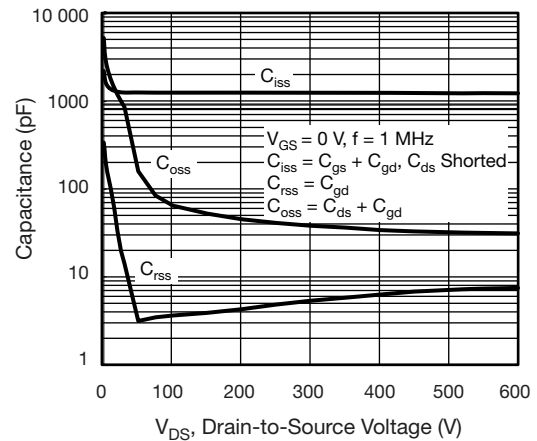


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

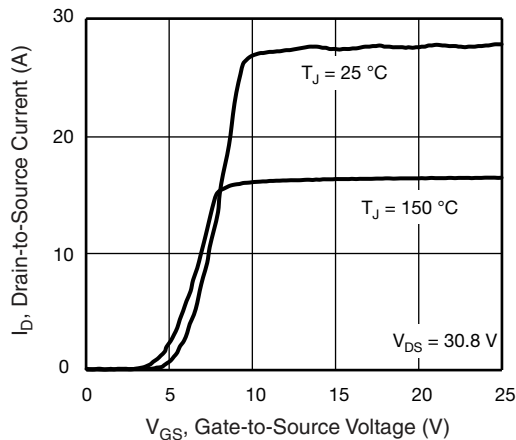


Fig. 3 - Typical Transfer Characteristics

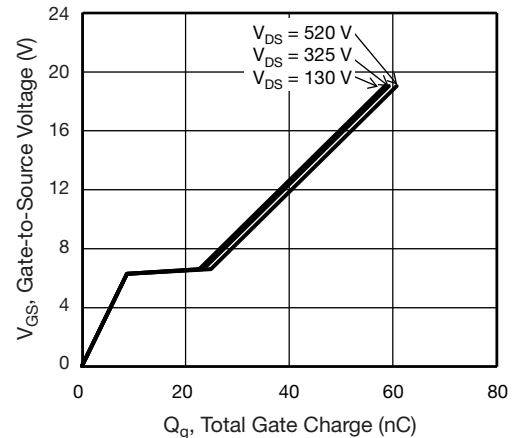


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

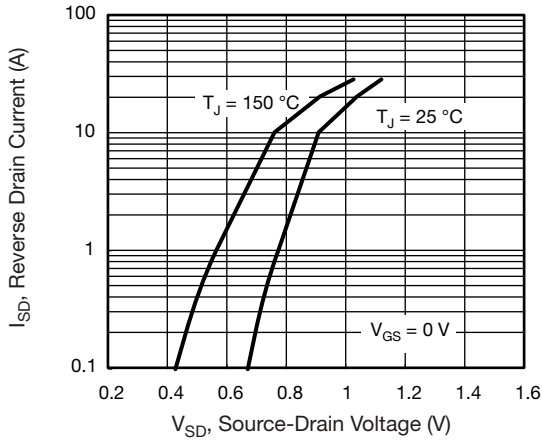


Fig. 7 - Typical Source-Drain Diode Forward Voltage

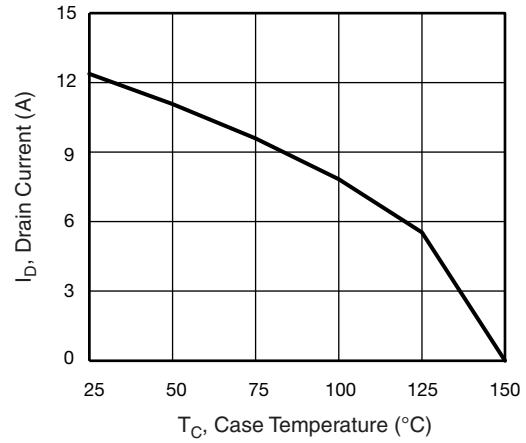


Fig. 9 - Maximum Drain Current vs. Case Temperature

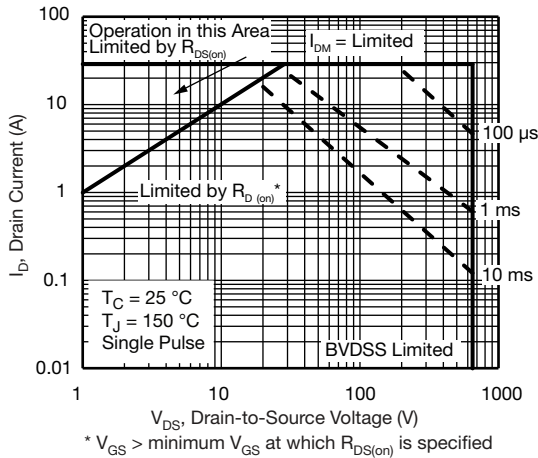


Fig. 8 - Maximum Safe Operating Area

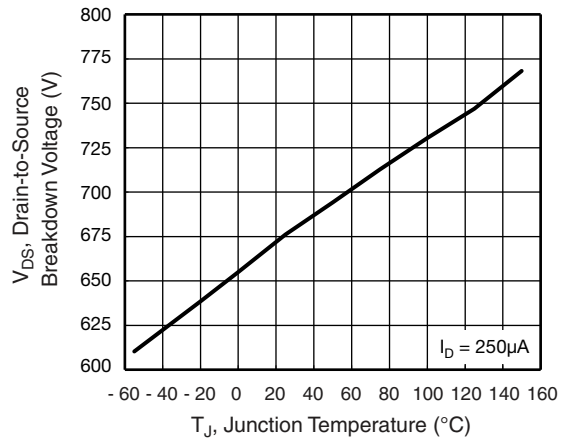


Fig. 10 - Temperature vs. Drain-to-Source Voltage

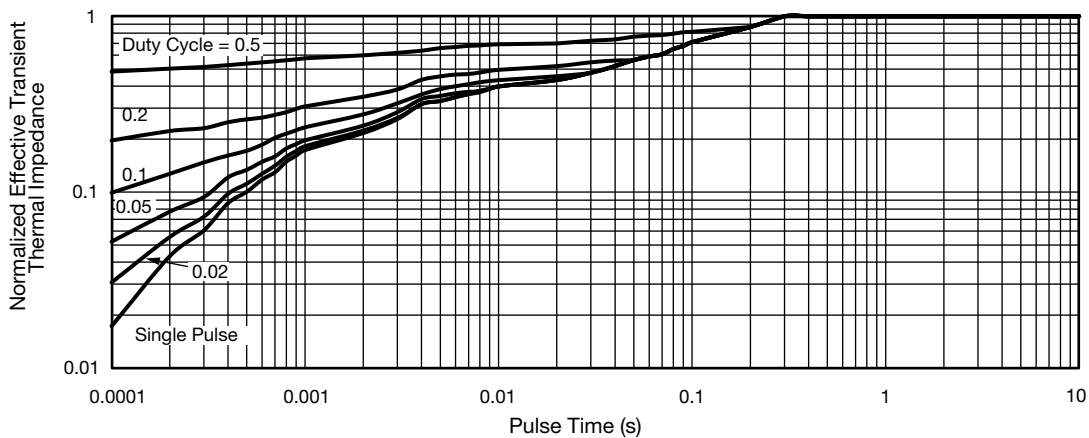


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

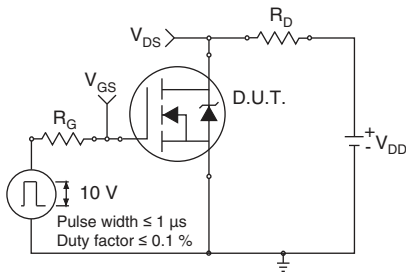


Fig. 12 - Switching Time Test Circuit



Fig. 16 - Basic Gate Charge Waveform

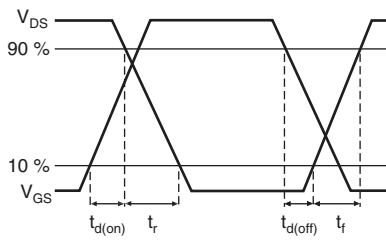


Fig. 13 - Switching Time Waveforms



Fig. 17 - Gate Charge Test Circuit



Fig. 14 - Unclamped Inductive Test Circuit

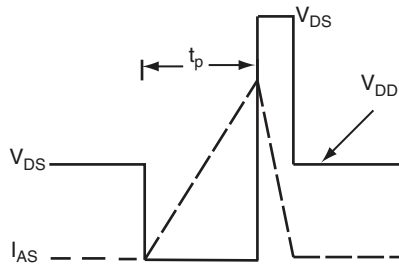
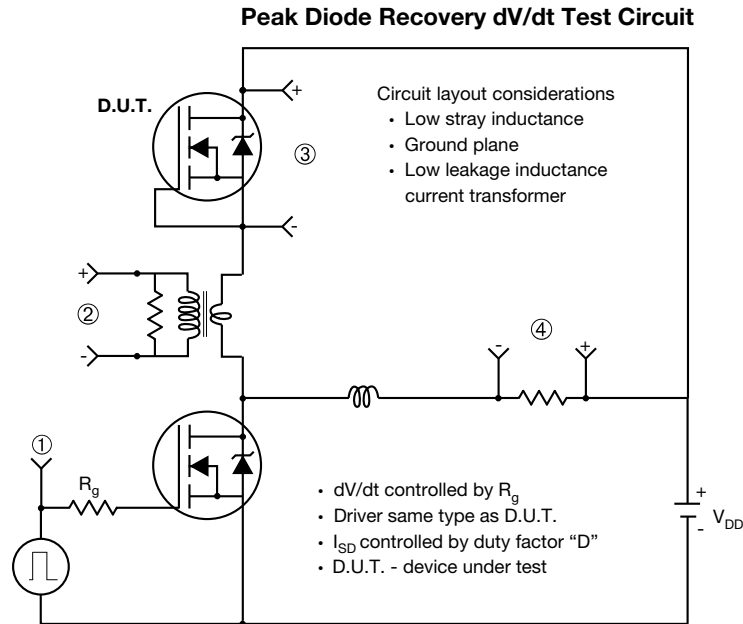


Fig. 15 - Unclamped Inductive Waveforms



Note

a. $V_{GS} = 5 V$ for logic level devices

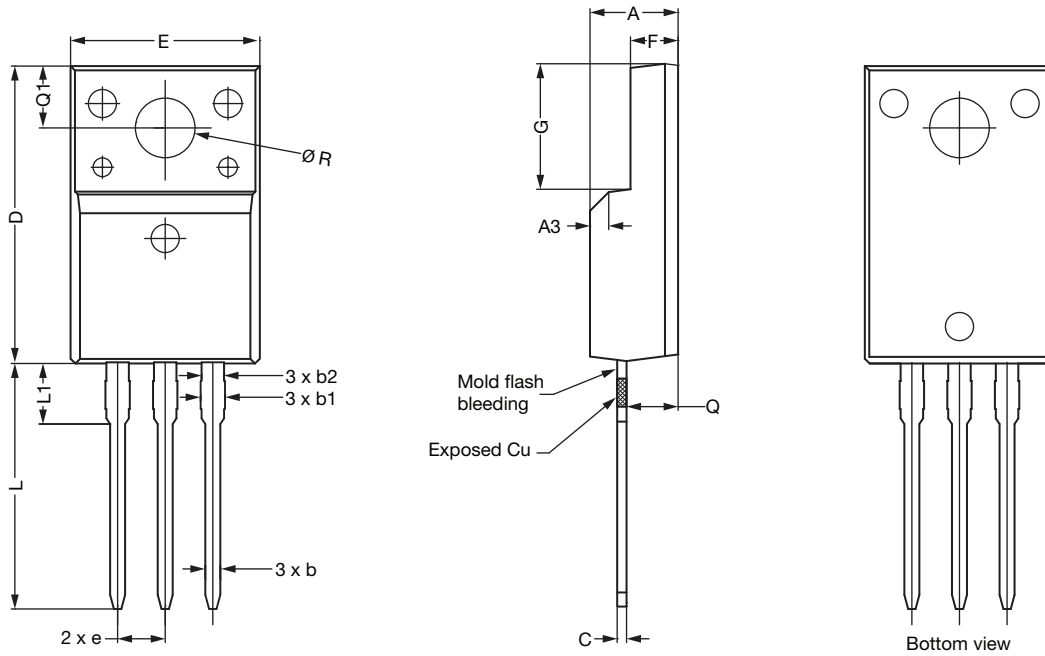
Fig. 18 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



| DIM. | MILLIMETERS | | |
|-----------------|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 4.60 | 4.70 | 4.80 |
| b | 0.70 | 0.80 | 0.91 |
| b1 | 1.20 | 1.30 | 1.47 |
| b2 | 1.10 | 1.20 | 1.30 |
| C | 0.45 | 0.50 | 0.63 |
| D | 15.80 | 15.87 | 15.97 |
| e | 2.54 BSC | | |
| E | 10.00 | 10.10 | 10.30 |
| F | 2.44 | 2.54 | 2.64 |
| G | 6.50 | 6.70 | 6.90 |
| L | 12.90 | 13.10 | 13.30 |
| L1 | 3.13 | 3.23 | 3.33 |
| Q | 2.65 | 2.75 | 2.85 |
| Q1 | 3.20 | 3.30 | 3.40 |
| $\varnothing R$ | 3.08 | 3.18 | 3.28 |

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking



OPTION 2: FACILITY CODE = Y



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|--------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.570 | 4.830 | 0.180 | 0.190 |
| A1 | 2.570 | 2.830 | 0.101 | 0.111 |
| A2 | 2.510 | 2.850 | 0.099 | 0.112 |
| b | 0.622 | 0.890 | 0.024 | 0.035 |
| b2 | 1.229 | 1.400 | 0.048 | 0.055 |
| b3 | 1.229 | 1.400 | 0.048 | 0.055 |
| c | 0.440 | 0.629 | 0.017 | 0.025 |
| D | 8.650 | 9.800 | 0.341 | 0.386 |
| d1 | 15.88 | 16.120 | 0.622 | 0.635 |
| d3 | 12.300 | 12.920 | 0.484 | 0.509 |
| E | 10.360 | 10.630 | 0.408 | 0.419 |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.200 | 13.730 | 0.520 | 0.541 |
| L1 | 3.100 | 3.500 | 0.122 | 0.138 |
| n | 6.050 | 6.150 | 0.238 | 0.242 |
| Ø P | 3.050 | 3.450 | 0.120 | 0.136 |
| u | 2.400 | 2.500 | 0.094 | 0.098 |
| V | 0.400 | 0.500 | 0.016 | 0.020 |

ECN: E19-0180-Rev. D, 08-Apr-2019
DWG: 5972

Notes

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2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking



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