# 1.7 Ω, Low On Resistance, +12 V, +5 V, +3 V, ± 5 V, SPST Switches

## DESCRIPTION

The DG9421E and DG9422E are monolithic single-pole-single-throw (SPST) analog switches. The DG9421E has a normally closed function. The DG9422E has a normally open function.

Processed with high density BiCMOS technology, the parts achieve low resistance, fast switching speed, low power dissipation, high -3dB bandwidth, and low voltage logic control threshold.

The DG9421E and DG9422E operate on single and dual supplies. Single supply voltage ranges from +3 V to +16 V while dual supply operation is recommended with ± 3 V to ± 8 V. Each switch conducts equally well in both direction when on, and blocks input voltages up to the supply levels when off.

The low and flat on resistance over the full input signal voltage range brings excellent linearity, reduces insertion loss and signal distortion, makes them ideal for data acquisition and programmable gain control applications. These switch characters also make them ideal fit for audio signal switch and reed relay replacement.

Operation temperature is specified from -40 °C to +85 °C. The DG9421E and DG9422E are available in 6 lead TSSOP packages.

## BENEFITS

- Wide operation voltage range
- Low signal errors and distortion
- Fast switching time
- Simple interfacing

## FEATURES

Pb-free Available

RoHS* Available

HALOGEN FREE

- 3 V to 16 V single supply or ± 3 thru ± 8 V dual supply operation
- Low on resistance: 1.7 Ω typical at 12 V
- 2.4 V logic compatible for control
- Bi-directional rail to rail signal switching
- Fast switching speed
- High bandwidth: 161 MHz
- Control logic input can be over V+
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

**Note**

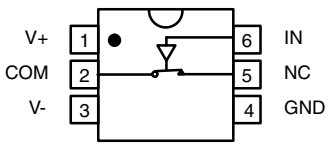
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Audio and video signal routing
- Relay replacement
- Battery powered systems
- Computer peripherals
- Audio and video signal routing

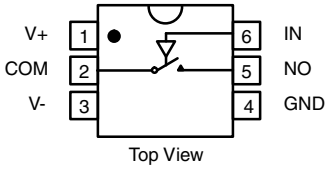
## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

TSOP-6




Top View
Device Marking:
DG9421EDV = 4Mxxx

TSOP-6




Top View
Device Marking:
DG9422EDV = 4Nxxx

**TRUTH TABLE**

| LOGIC | DG9421E | DG9422E |
|---|---|---|
| 0 | On | Off |
| 1 | Off | On |

**Notes**

- Logic “0” ≤ 0.8 V
- Logic “1” ≥ 2.4 V
- Switches shown for logic “0” input

**ORDERING INFORMATION**

| TEMP. RANGE | PACKAGE | PART NUMBER |
|---|---|---|
| -40 °C to +85 °C | 6-pin TSOP | DG9421EDV-T1-GE3 |
| | | DG9422EDV-T1-GE3 |

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | LIMIT | UNIT |
|---|---|---|---|
| V+ reference to V- | | -0.3 to +18 | V |
| IN | | -0.3 to +18 | |
| V+ reference to GND | | -0.3 to +18 | |
| GND reference to V- | | -0.3 to +18 | |
| COM, NC, NO [a] | | (V-) - 0.3 V to (V+) + 0.3 V or 50 mA, whichever occurs first | - |
| Continuous current (any terminal) | | 50 | mA |
| Peak current, NO, NC or COM (pulsed at 1 ms, 10 % duty cycle) | | 100 | |
| Storage temperature | | -65 to +150 | °C |
| Power dissipation (packages) [b] | 6-pin TSOP [c] | 570 | mW |
| ESD / HBM | JS-001 | 2000 | V |
| ESD / CDM | JS-002 | 2000 | |
| Latch up | per JEDEC78 | 300 | mA |

**Notes**

a. Signals on NO, NC, COM exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 7 mW/°C above 25 °C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## SPECIFICATIONS [a] (Single supply 12 V)

| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V- = 0 V, $V_{IN}$ = 2.4 V, 0.8 V [f] | TEMP. [b] | LIMITS -40 °C to +85°C MIN. [d] | TYP. [c] | MAX. [d] | UNIT |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog signal range [a] | $V_{ANALOG}$ | | Full | 0 | - | 12 | V |
| Drain-source on-resistance | $R_{DS(on)}$ | V+ = 10.8 V, V- = 0 V, $I_{NO/NC}$ = 5 mA, $V_{COM}$ = 2 V / 9 V | Room | - | 1.7 | 2.7 | Ω |
| | | | Full | - | - | 3.2 | |
| Switch off leakage current [g] | $I_{NO/NC(off)}$ | $V_{COM}$ = 1 V / 11 V, $V_{NO/NC}$ = 11 V / 1 V | Room | -1 | ± 0.004 | 1 | nA |
| | | | Full | -10 | ± 1.06 | 10 | |
| | $I_{COM(off)}$ | | Room | -1 | ± 0.004 | 1 | |
| | | | Full | -10 | ± 0.23 | 10 | |
| Channel-on leakage current [g] | $I_{COM(on)}$ | $V_{NO/NC}$ = $V_{COM}$ = 11 V / 1 V | Room | -1 | ± 0.002 | 1 | |
| | | | Full | -10 | ± 0.454 | 10 | |
| **Digital Control** | | | | | | | |
| Input current, $V_{IN}$ low | $I_{IL}$ | $V_{IN}$ under test = 0.8 V | Full | -1 | 0.001 | 1 | µA |
| Input current, $V_{IN}$ high | $I_{IH}$ | $V_{IN}$ under test = 2.4 V | Full | -1 | 0.001 | 1 | |
| **Dynamic Characteristics** | | | | | | | |
| Turn-on time [e] | $t_{ON}$ | $R_L$ = 300 Ω, $C_L$ = 35 pF, $V_S$ = 5 V | Room | - | 28 | 36 | ns |
| | | | Full | - | - | 41 | |
| Turn-off time [e] | $t_{OFF}$ | | Room | - | 12 | 20 | |
| | | | Full | - | - | 22 | |
| Charge injection [e] | Q | $V_g$ = 0 V, $R_g$ = 0 Ω, $C_L$ = 1 nF | Room | - | 19 | - | pC |
| Bandwidth [e] | BW | $R_L$ = 50 Ω, $C_L$ = 5 pF | Room | - | 161 | - | MHz |
| Off-isolation [e] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | - | -58 | - | dB |
| Source off capacitance [e] | $C_{NO/NC(off)}$ | f = 1 MHz | Room | - | 34 | - | pF |
| Drain off capacitance [e] | $C_{COM(off)}$ | | Room | - | 36 | - | |
| Channel on capacitance [e] | $C_{COM(on)}$ | | Room | - | 68 | - | |
| **Power Supplies** | | | | | | | |
| Positive supply current | I+ | $V_{IN}$ = 0 V or 12 V | Room | - | 0.001 | 1 | µA |
| | | | Full | - | - | 5 | |
| Negative supply current | I- | | Room | -1 | -0.001 | - | |
| | | | Full | -5 | - | - | |
| Ground current | $I_{GND}$ | | Room | -1 | -0.001 | - | |
| | | | Full | -5 | - | - | |

| **SPECIFICATIONS** [a] (Dual supply ± 5 V) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 5 V, V- = -5 V, $V_{IN}$ = 2.4 V, 0.8 V [f] | **TEMP.** [b] | **LIMITS** -40 °C to +85 °C | | | **UNIT** |
| | | | | **MIN.** [d] | **TYP.** [c] | **MAX.** [d] | |
| **Analog Switch** | | | | | | | |
| Analog signal range [e] | $V_{ANALOG}$ | | Full | -5 | - | 5 | V |
| Drain-source on-resistance | $R_{DS(on)}$ | V+ = 5 V, V- = 5 V<br>$I_{NO/NC}$ = 5 mA, $V_{COM}$ = ± 3.5 V | Room | - | 1.9 | 2.9 | Ω |
| | | | Full | - | - | 3.4 | |
| Switch off leakage current [g] | $I_{NO/NC(off)}$ | V+ = 5.5 V, V- = 5.5 V<br>$V_{COM}$ = ± 4.5 V, $V_{NO/NC}$ = ∓ 4.5 V | Room | -1 | ± 0.004 | 1 | nA |
| | | | Full | -10 | ± 1.012 | 10 | |
| | $I_{COM(off)}$ | | Room | -1 | ± 0.003 | 1 | |
| | | | Full | -10 | ± 0.188 | 10 | |
| Channel-on leakage current [g] | $I_{COM(on)}$ | V+ = 5.5 V, V- = -5.5 V<br>$V_{NO/NC}$ = $V_{COM}$ = ± 4.5 V | Room | -1 | ± 0.002 | 1 | |
| | | | Full | -10 | ± 0.425 | 10 | |
| **Digital Control** | | | | | | | |
| Input current, $V_{IN}$ low [e] | $I_{IL}$ | $V_{IN}$ under test = 0.8 V | Full | -1 | 0.001 | 1 | µA |
| Input current, $V_{IN}$ high [e] | $I_{IH}$ | $V_{IN}$ under test = 2.4 V | Full | -1 | 0.001 | 1 | |
| **Dynamic Characteristics** | | | | | | | |
| Turn-on time | $t_{ON}$ | $R_L$ = 300 Ω, $C_L$ = 35 pF, $V_S$ = ± 3.5 V | Room | - | 39 | 54 | ns |
| | | | Full | - | - | 62 | |
| Turn-off time | $t_{OFF}$ | | Room | - | 28 | 33 | |
| | | | Full | - | - | 42 | |
| Charge injection [e] | Q | $V_g$ = 0 V, $R_g$ = 0 Ω, $C_L$ = 1 nF | Room | - | 57 | - | pC |
| Bandwidth [e] | BW | $R_L$ = 50 Ω, $C_L$ = 5 pF | Room | - | 179 | - | MHz |
| Off-isolation [e] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | - | -58 | - | dB |
| Source off capacitance [e] | $C_{NO/NC(off)}$ | f = 1 MHz | Room | - | 34 | - | pF |
| Drain off capacitance [e] | $C_{COM(off)}$ | | Room | - | 36 | - | |
| Channel on capacitance [e] | $C_{COM(on)}$ | | Room | - | 68 | - | |
| **Power Supplies** | | | | | | | |
| Positive supply current [e] | I+ | $V_{IN}$ = 0 V or 5 V | Room | - | 0.001 | 1 | µA |
| | | | Full | - | - | 5 | |
| Negative supply current [e] | I- | | Room | -1 | -0.001 | - | |
| | | | Full | -5 | - | - | |
| Ground current [e] | $I_{GND}$ | | Room | -1 | -0.001 | - | |
| | | | Full | -5 | - | - | |

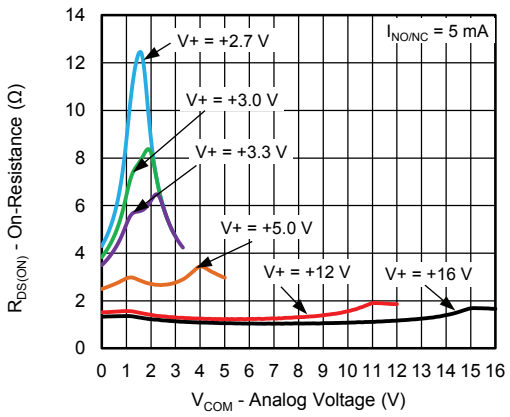
| **SPECIFICATIONS** [a] (Single supply 5 V) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 5 V, V- = 0 V, $V_{IN}$ = 2.4 V, 0.8 V [f] | **TEMP.** [b] | **LIMITS** -40 °C to +85 °C | | | **UNIT** |
| | | | | **MIN.** [d] | **TYP.** [c] | **MAX.** [d] | |
| **Analog Switch** | | | | | | | |
| Analog signal range [e] | $V_{ANALOG}$ | | Full | 0 | - | 5 | V |
| Drain-source on-resistance | $R_{DS(on)}$ | V+ = 4.5 V, $I_{NO/NC}$ = 5 mA, $V_{COM}$ = 1 V, 3.5 V | Room | - | 3.04 | 5.4 | Ω |
| | | | Full | - | - | 7 | |
| **Dynamic Characteristics** | | | | | | | |
| Turn-on time [e] | $t_{ON}$ | $R_L$ = 300 Ω, $C_L$ = 35 pF, $V_S$ = 3.5 V | Room | - | 57 | 82 | ns |
| | | | Hot | - | - | 95 | |
| Turn-off time [e] | $t_{OFF}$ | | Room | - | 24 | 34 | |
| | | | Hot | - | - | 40 | |
| Charge injection [e] | Q | $V_g$ = 0 V, $R_g$ = 0 Ω, $C_L$ = 1 nF | Room | - | 12 | - | pC |
| **Power Supplies** | | | | | | | |
| Positive supply current [e] | I+ | $V_{IN}$ = 0 V or 5 V | Room | - | 0.001 | 1 | µA |
| | | | Hot | - | - | 5 | |
| Negative supply current [e] | I- | | Room | -1 | -0.001 | - | |
| | | | Hot | -5 | - | - | |
| Ground current [e] | $I_{GND}$ | | Room | -1 | -0.001 | - | |
| | | | Hot | -5 | - | - | |

| **SPECIFICATIONS** [a] (Single supply 3 V) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 3 V, V- = 0 V, $V_{IN}$ = 2.4 V, 0.4 V [f] | **TEMP.** [b] | **LIMITS** -40 °C to +85 °C | | | **UNIT** |
| | | | | **MIN.** [d] | **TYP.** [c] | **MAX.** [d] | |
| **Analog Switch** | | | | | | | |
| Analog signal range [e] | $V_{ANALOG}$ | | Full | 0 | - | 3 | V |
| Drain-source on-resistance | $R_{DS(on)}$ | V+ = 2.7 V, V- = 0 V<br>$I_{NO/NC}$ = 5 mA, $V_{COM}$ = 0.5 V, 2.2 V | Room | - | 7.3 | 11.5 | Ω |
| | | | Full | - | - | 18 | |
| Switch off leakage current [g] | $I_{NO/NC(off)}$ | V+ = 3.3 V, V- = 0 V<br>$V_{NO/NC}$ = 1 V, 2 V, $V_{COM}$ = 2 V, 1 V | Room | -1 | ± 0.003 | 1 | nA |
| | | | Full | -10 | ± 0.9 | 10 | |
| | $I_{COM(off)}$ | | Room | -1 | ± 0.0008 | 1 | |
| | | | Full | -10 | ± 0.042 | 10 | |
| Channel-on leakage current [g] | $I_{COM(on)}$ | V+ = 3.3 V, V- = 0 V<br>$V_{COM}$ = $V_{NO/NC}$ = 1 V, 2 V | Room | -1 | ± 0.0014 | 1 | |
| | | | Full | -10 | ± 0.41 | 10 | |
| **Digital Control** | | | | | | | |
| Input current, $V_{IN}$ low [e] | $I_{IL}$ | $V_{IN}$ under test = 0.4 V | Full | -1 | 0.001 | 1 | µA |
| Input current, $V_{IN}$ high [e] | $I_{IH}$ | $V_{IN}$ under test = 2.4 V | Full | -1 | 0.001 | 1 | |
| **Dynamic Characteristics** | | | | | | | |
| Turn-on time | $t_{ON}$ | $R_L$ = 300 Ω, $C_L$ = 35 pF, $V_S$ = 1.5 V | Room | - | 124 | 215 | ns |
| | | | Full | - | - | 222 | |
| Turn-off time | $t_{OFF}$ | | Room | - | 58 | 101 | |
| | | | Full | - | - | 106 | |
| Charge injection [e] | Q | $V_g$ = 0 V, $R_g$ = 0 Ω, $C_L$ = 1 nF | Room | - | 6 | - | pC |
| Off-isolation [e] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | - | -58 | - | dB |
| Source off capacitance [e] | $C_{NO/NC(off)}$ | f = 1 MHz | Room | - | 36 | - | pF |
| Drain off capacitance [e] | $C_{COM(off)}$ | | Room | - | 38 | - | |
| Channel on capacitance [e] | $C_{COM(on)}$ | | Room | - | 70 | - | |

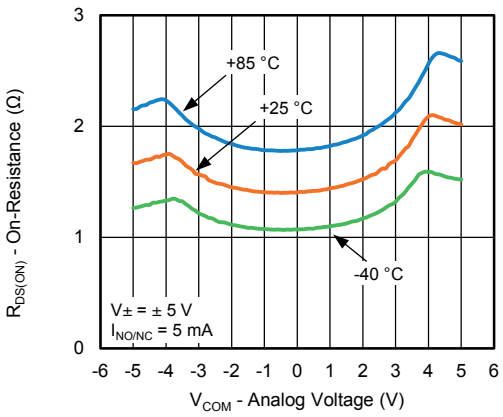
**Notes**

a. Refer to PROCESS OPTION FLOWCHART
b. Room = 25 °C, full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. $V_{IN}$ = input voltage to perform proper function
g. Leakage parameters are guaranteed by worst case test conditions and not subject to test

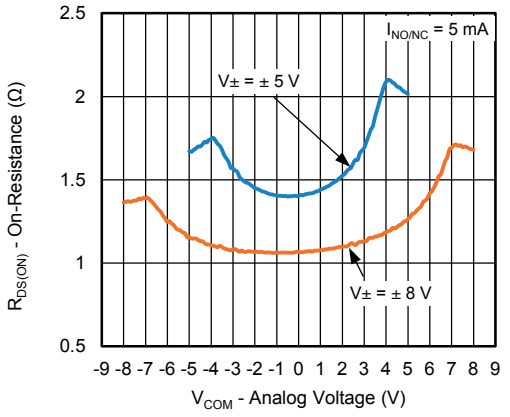
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



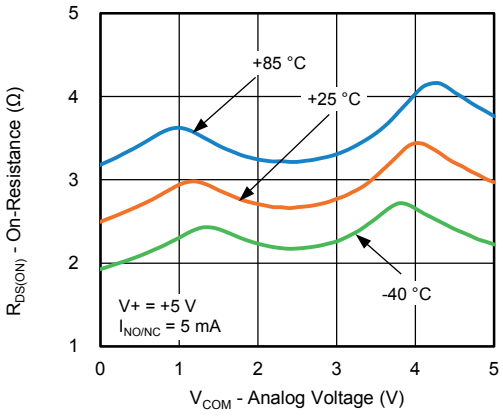

**$R_{ON}$ vs. $V_{COM}$ and Single Supply Voltage**



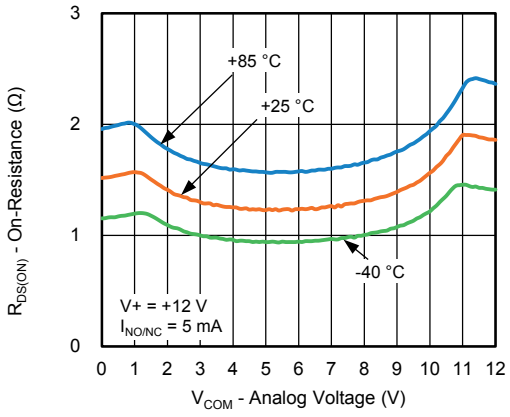

**$R_{DS(on)}$ vs. Analog Voltage and Temperature**



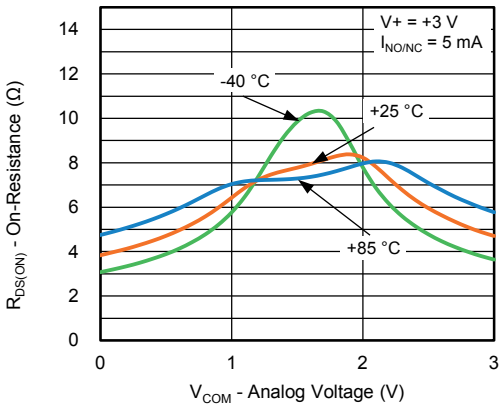

**$R_{ON}$ vs. $V_{COM}$ and Dual Supply Voltage**




**$R_{DS(on)}$ vs. Analog Voltage and Temperature**

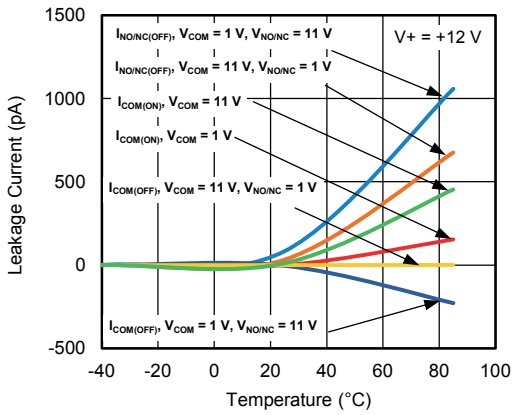



**$R_{DS(on)}$ vs. Analog Voltage and Temperature**

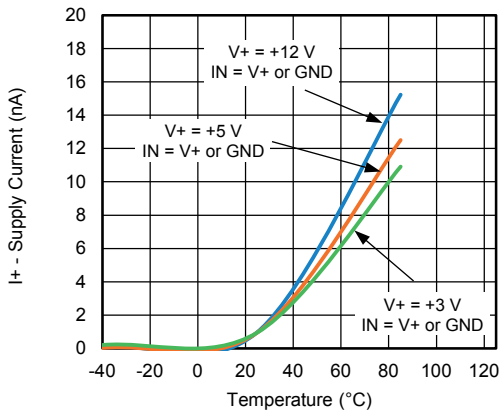



**$R_{DS(on)}$ vs. Analog Voltage and Temperature**

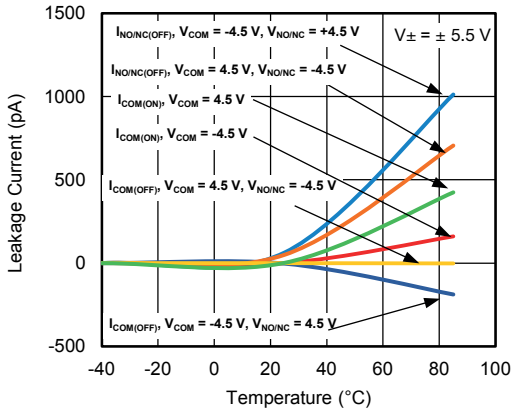
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



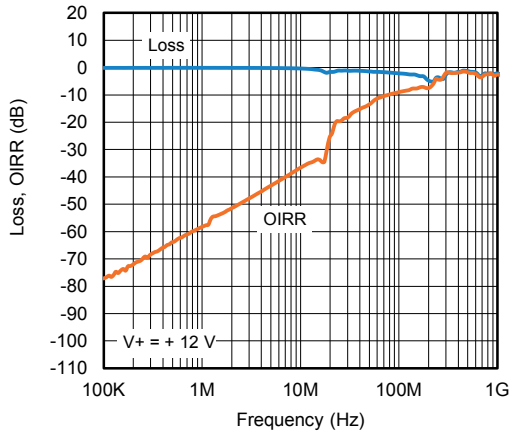

**Leakage Current vs. Temperature**



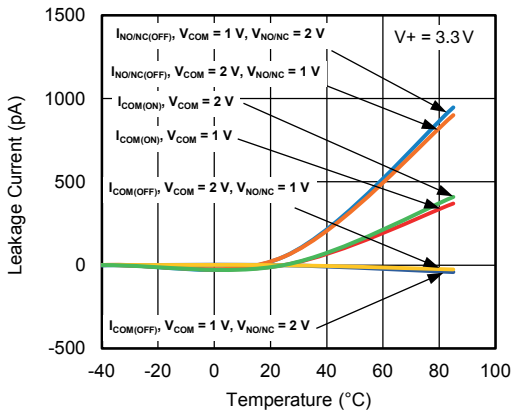

**Supply Current vs. Temperature**



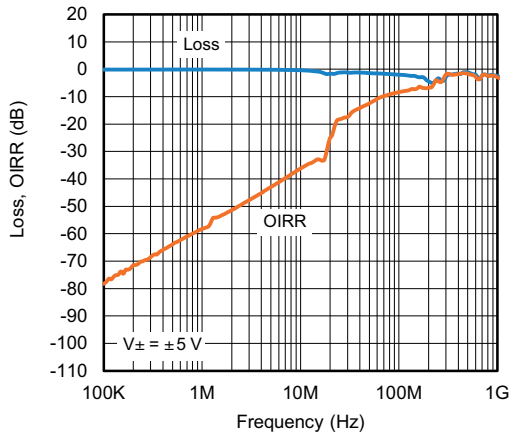

**Leakage Current vs. Temperature**




**Insertion Loss, Off-Isolation vs. Frequency**

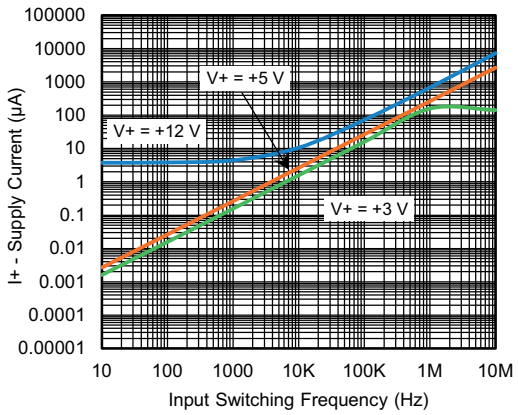



**Leakage Current vs. Temperature**

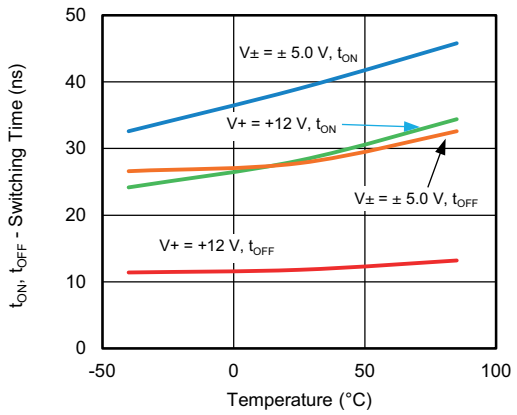



**Insertion Loss, Off-Isolation vs. Frequency**

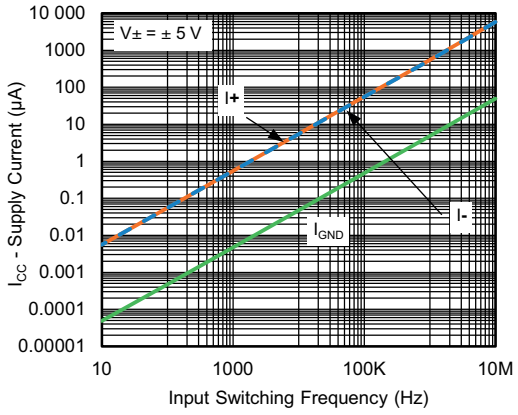
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



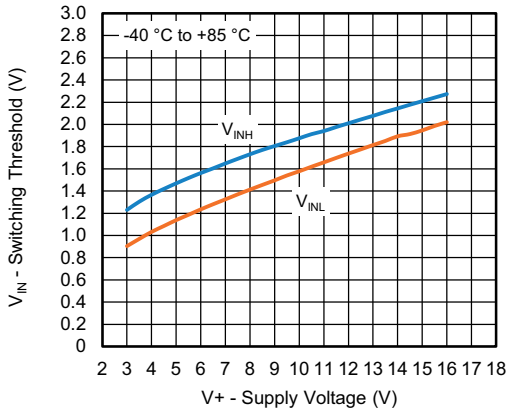

**Supply Current vs. Input Switching Frequency**



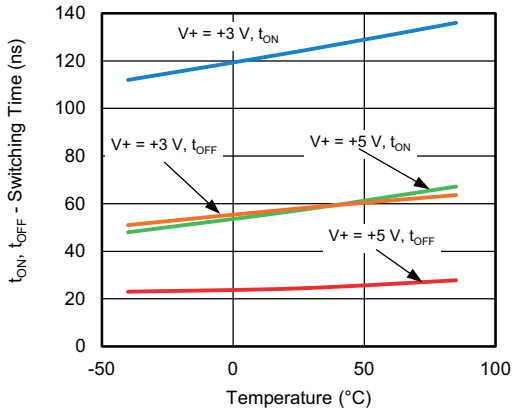

**Switching Time vs. Temperature**



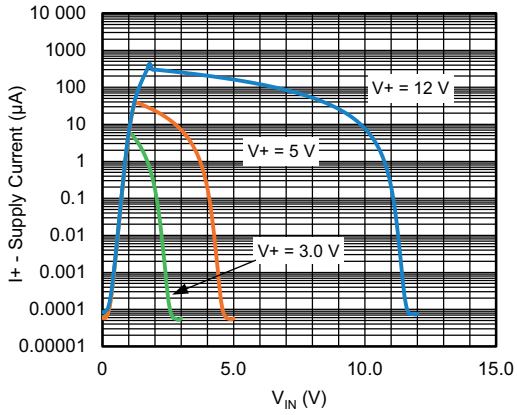

**Supply Current vs. Input Switching Frequency**




**Switching Threshold vs. Supply Voltage**

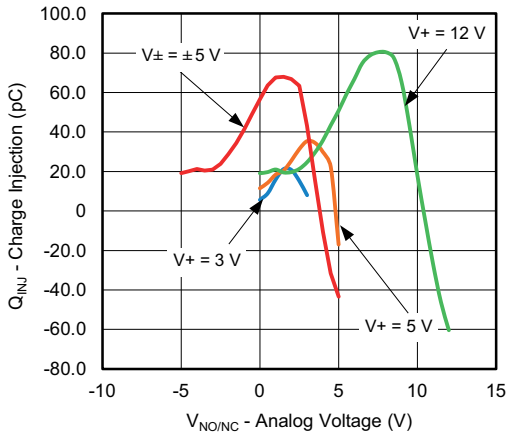



**Switching Time vs. Temperature**



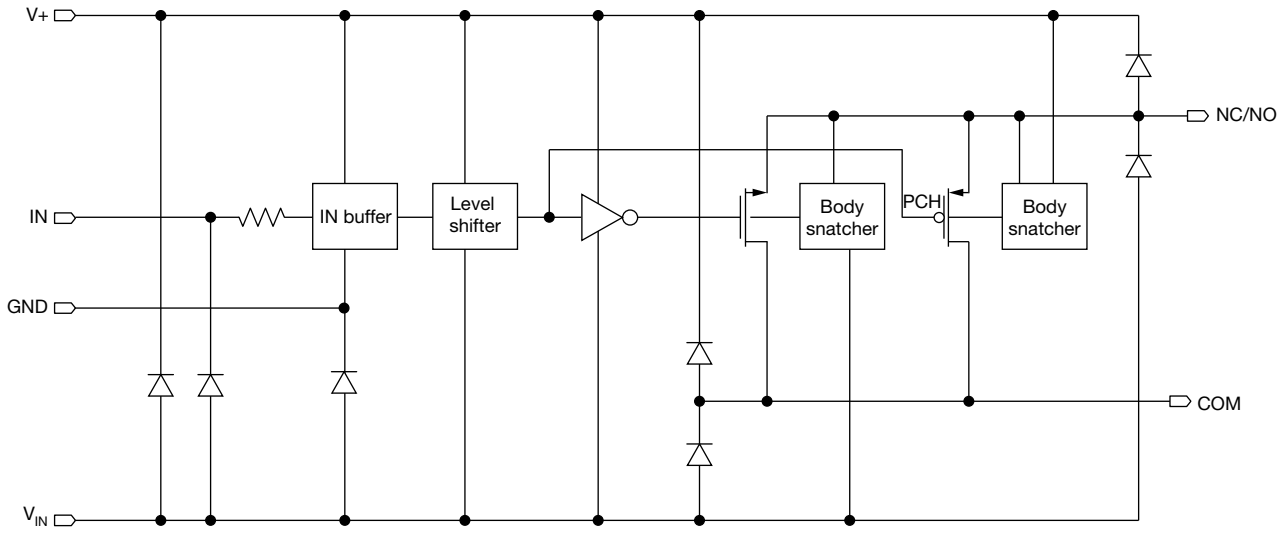

**Supply Current vs. Enable Input Voltage**

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

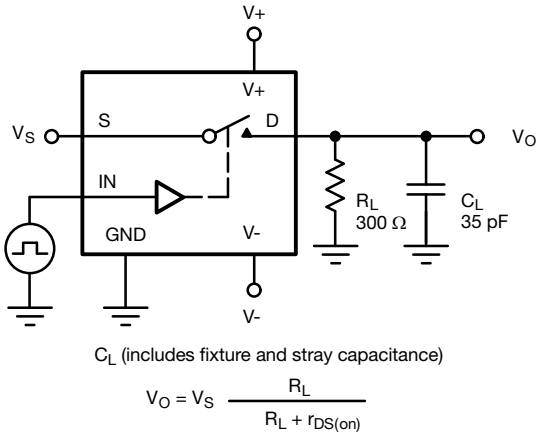



**Charge Injection vs. Analog Voltage**

## SCHEMATIC DIAGRAM (typical channel)

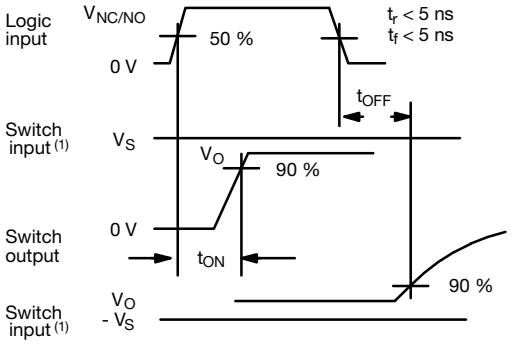


## TEST CIRCUITS




$C_L$ (includes fixture and stray capacitance)

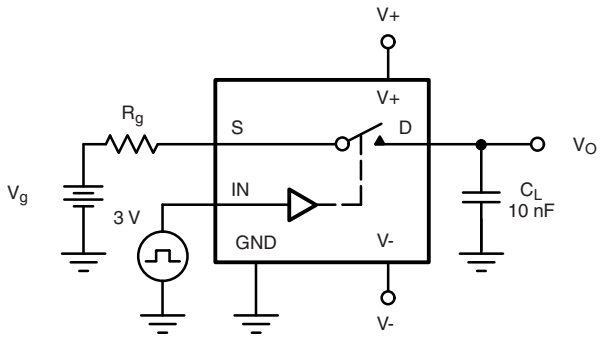
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

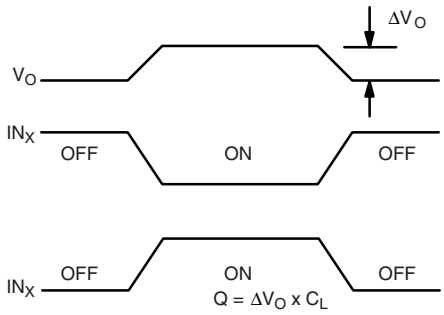



Note

(1) Logic input waveform is inverted for switches that have the opposite logic sense control

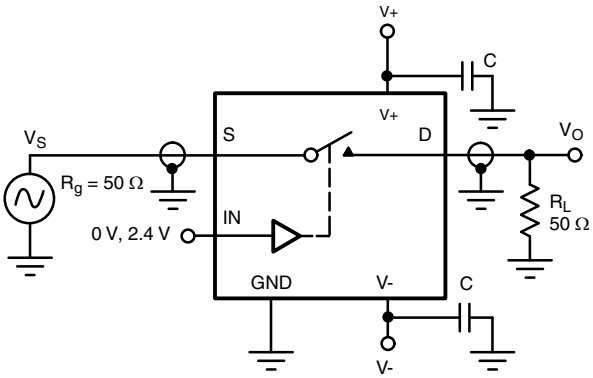
**Fig. 1 - Switching Time**




$IN_X$ dependent on switch configuration Input polarity determined by sense of switch.

**Fig. 2 - Charge Injection**




Off isolation = 20 log $\left|\frac{V_S}{V_O}\right|$

C = RF Bypass

**Fig. 3 - Off Isolation**

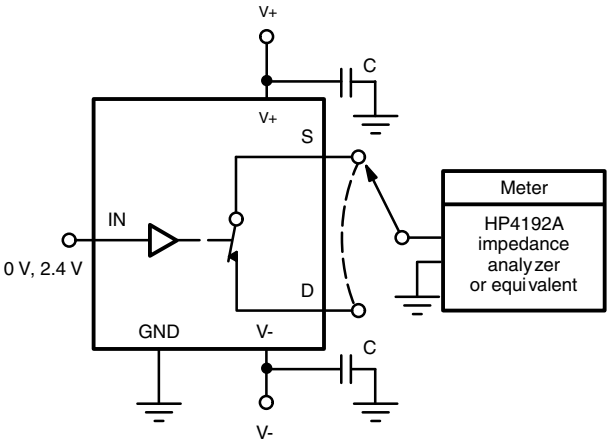
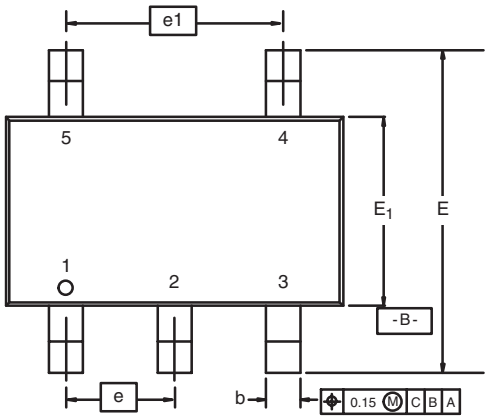


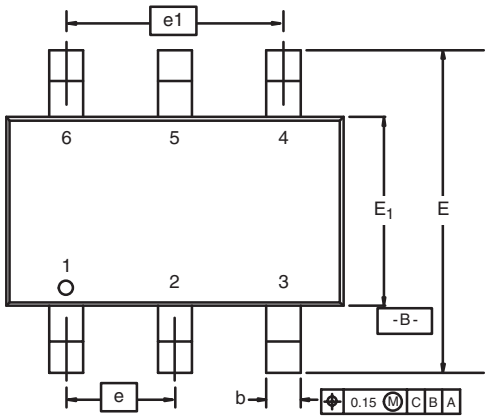

**Fig. 4 - Source/Drain Capacitances**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75411.*

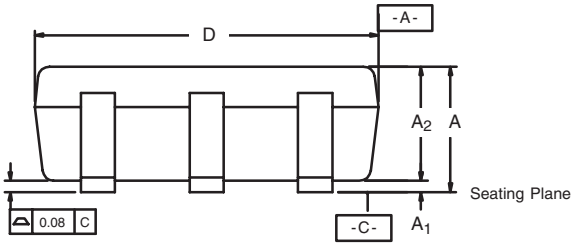
**TSOP: 5/6–LEAD**
**JEDEC Part Number: MO-193C**

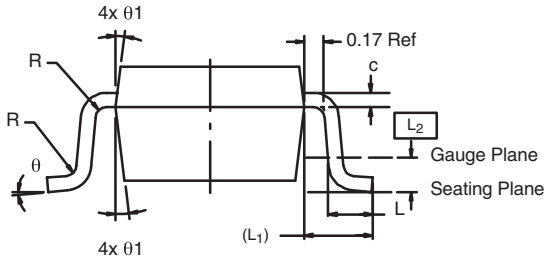



**5-LEAD TSOP**



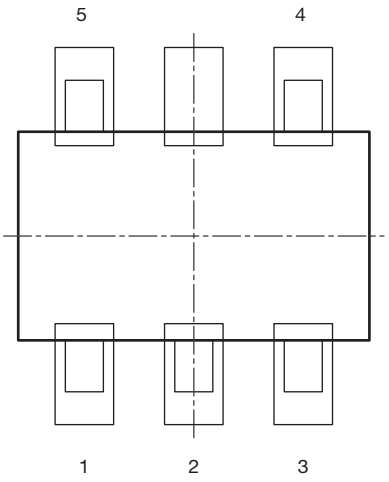

**6-LEAD TSOP**



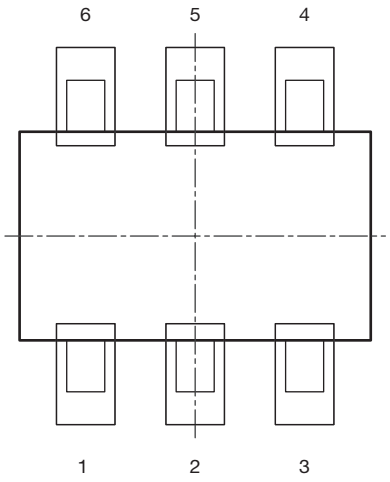




| Dim | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| **A** | 0.91 | - | 1.10 | 0.036 | - | 0.043 |
| **$A_1$** | 0.01 | - | 0.10 | 0.0004 | - | 0.004 |
| **$A_2$** | 0.90 | - | 1.00 | 0.035 | 0.038 | 0.039 |
| **b** | 0.30 | 0.32 | 0.45 | 0.012 | 0.013 | 0.018 |
| **c** | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| **D** | 2.95 | 3.05 | 3.10 | 0.116 | 0.120 | 0.122 |
| **E** | 2.70 | 2.85 | 2.98 | 0.106 | 0.112 | 0.117 |
| **$E_1$** | 1.55 | 1.65 | 1.70 | 0.061 | 0.065 | 0.067 |
| **e** | 0.95 BSC | | | 0.0374 BSC | | |
| **$e_1$** | 1.80 | 1.90 | 2.00 | 0.071 | 0.075 | 0.079 |
| **L** | 0.32 | - | 0.50 | 0.012 | - | 0.020 |
| **$L_1$** | 0.60 Ref | | | 0.024 Ref | | |
| **$L_2$** | 0.25 BSC | | | 0.010 BSC | | |
| **R** | 0.10 | - | - | 0.004 | - | - |
| θ | 0° | 4° | 8° | 0° | 4° | 8° |
| $\theta_1$ | 7° Nom | | | 7° Nom | | |
| ECN: C-06593-Rev. I, 18-Dec-06<br>DWG: 5540 | | | | | | |

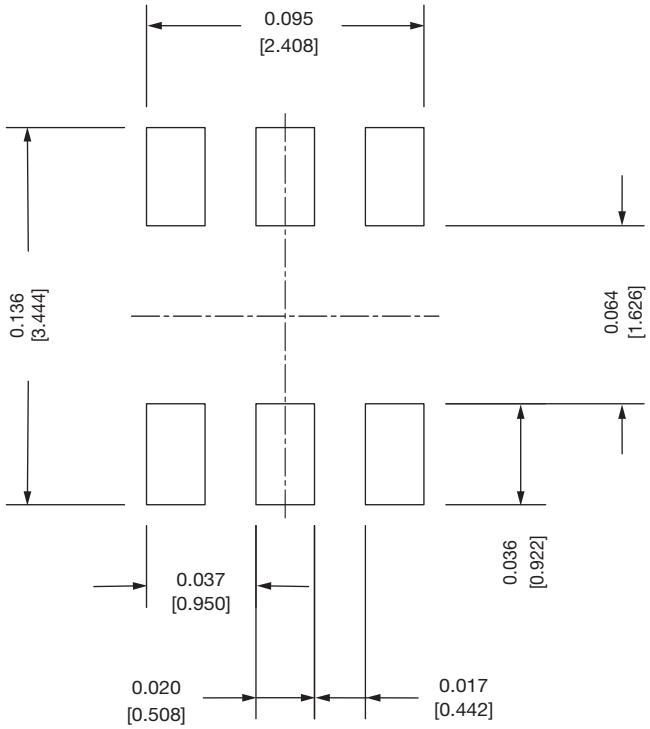
# Recommended Land Pattern For TSOP-5L / TSOP-6L




TSOP 5L




TSOP 6L




**Note**

- All dimensions are in inches (millimeter)

| |
|---|
| ECN: C22-0860-Rev. B, 24-Oct-2022<br>DWG: 3010 |

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