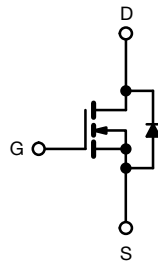
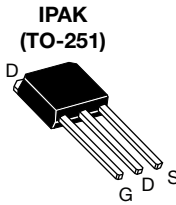


## E Series Power MOSFET



N-Channel MOSFET

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	850	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.82
$Q_g$ max. (nC)	44	
$Q_{gs}$ (nC)	5	
$Q_{gd}$ (nC)	8	
Configuration	Single	

### ORDERING INFORMATION

Package	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHU6N80E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	800	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current <sup>a</sup>	$I_{DM}$	15	
Linear derating factor		0.63	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	95	mJ
Maximum power dissipation	$P_D$	78	W
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Drain-source voltage slope	dv/dt	$T_J = 125$ °C	V/ns
Reverse diode dv/dt <sup>d</sup>			
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s	300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 2.6$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $di/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C



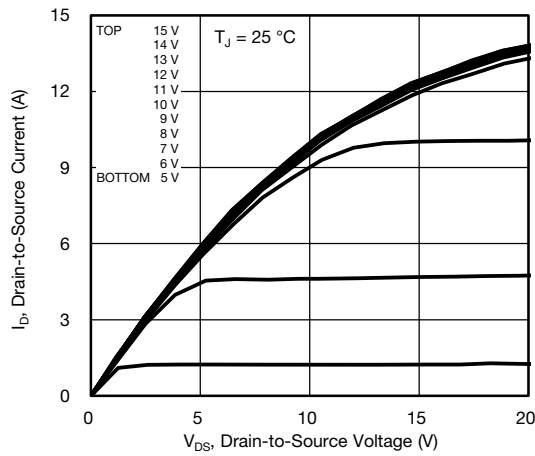
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	1.6	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		800	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	1.1	-	V/°C
Gate-source threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 640 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	10	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3 A	-	0.82	0.94	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 3 A		-	2.5	-	S
<b>Dynamic</b>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	827	-	pF
Output capacitance	C <sub>oss</sub>			-	37	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	5	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>			-	24	-	
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>	V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V		-	109	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3 A, V <sub>DS</sub> = 480 V	-	22	44	nC
Gate-source charge	Q <sub>gs</sub>			-	5	-	
Gate-drain charge	Q <sub>gd</sub>			-	8	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 3 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	13	26	ns
Rise time	t <sub>r</sub>			-	9	18	
Turn-off delay time	t <sub>d(off)</sub>			-	27	54	
Fall time	t <sub>f</sub>			-	18	36	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.5	1.0	2.0	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5.4	A
Pulsed diode forward current	I <sub>SM</sub>			-	-	15	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 3 A, di/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	282	564	ns
Reverse recovery charge	Q <sub>rr</sub>			-	2.0	4.0	μC
Reverse recovery current	I <sub>RRM</sub>			-	11	-	A

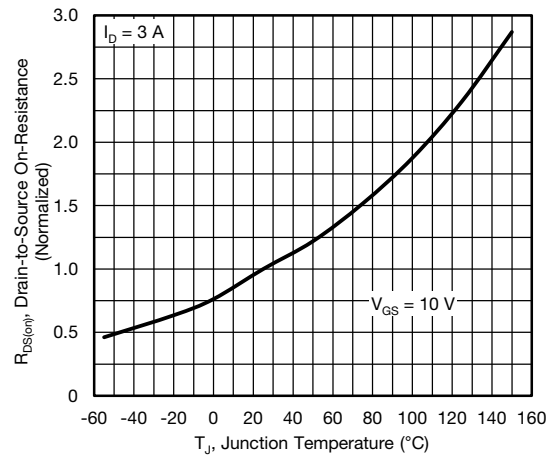
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 V to 480 V V<sub>DSS</sub>
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 V to 480 V V<sub>DSS</sub>

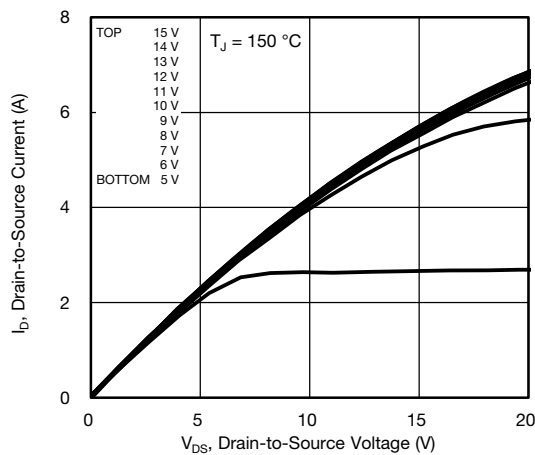
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



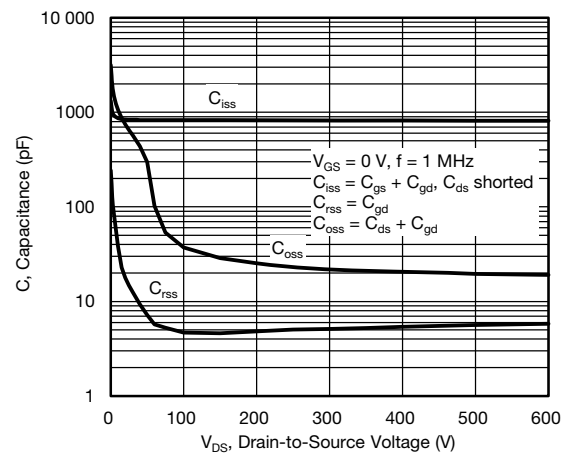
**Fig. 1 - Typical Output Characteristics**



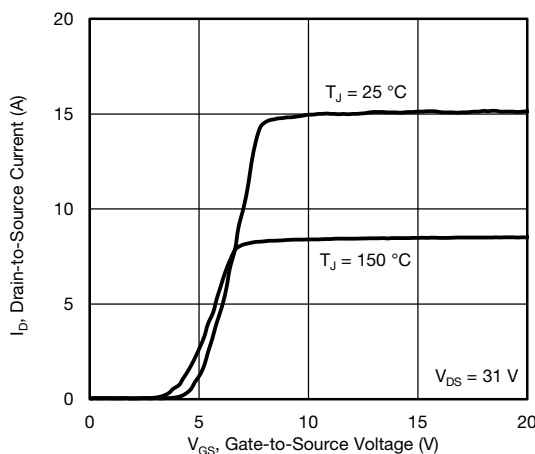
**Fig. 4 - Normalized On-Resistance vs. Temperature**



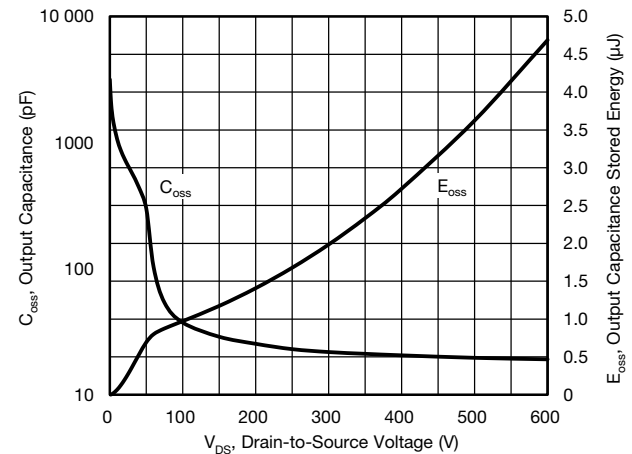
**Fig. 2 - Typical Output Characteristics**



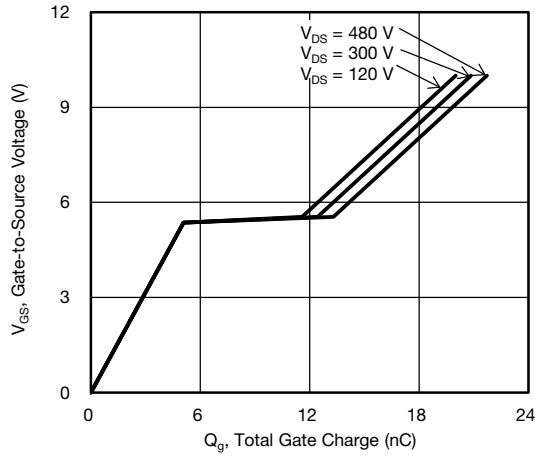
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



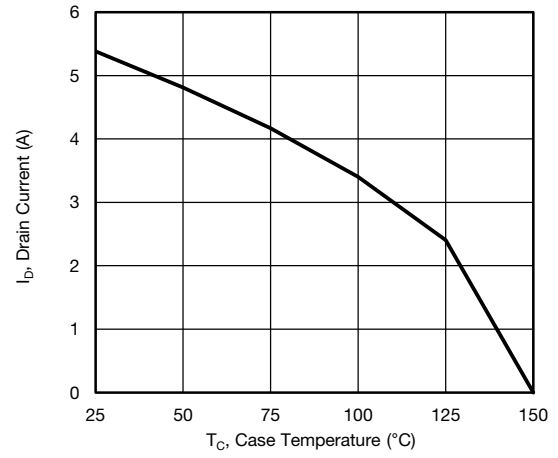
**Fig. 3 - Typical Transfer Characteristics**



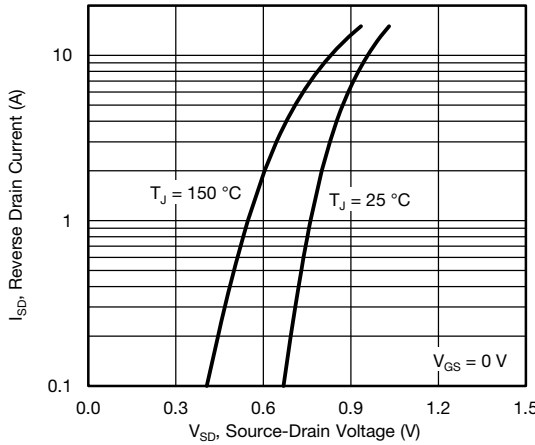
**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**



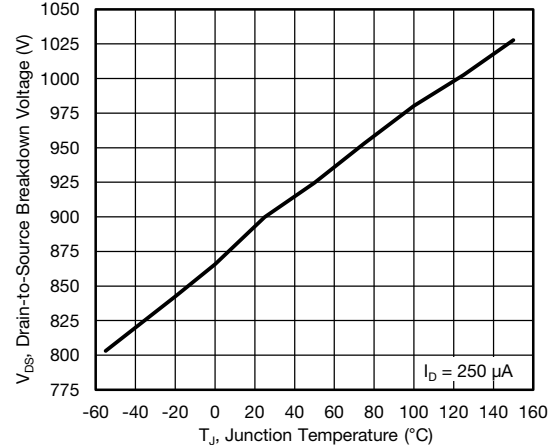
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



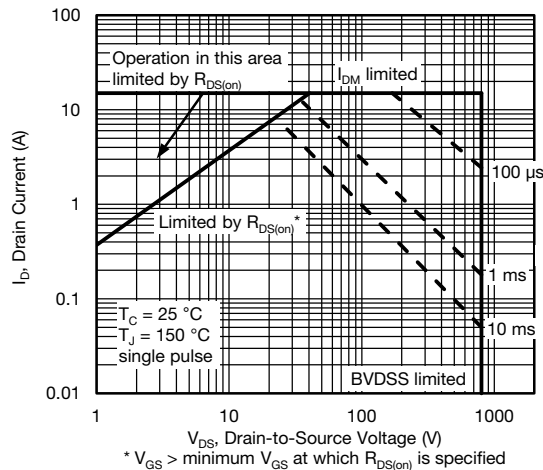
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



**Fig. 11 - Temperature vs. Drain-to-Source Voltage**



**Fig. 9 - Maximum Safe Operating Area**

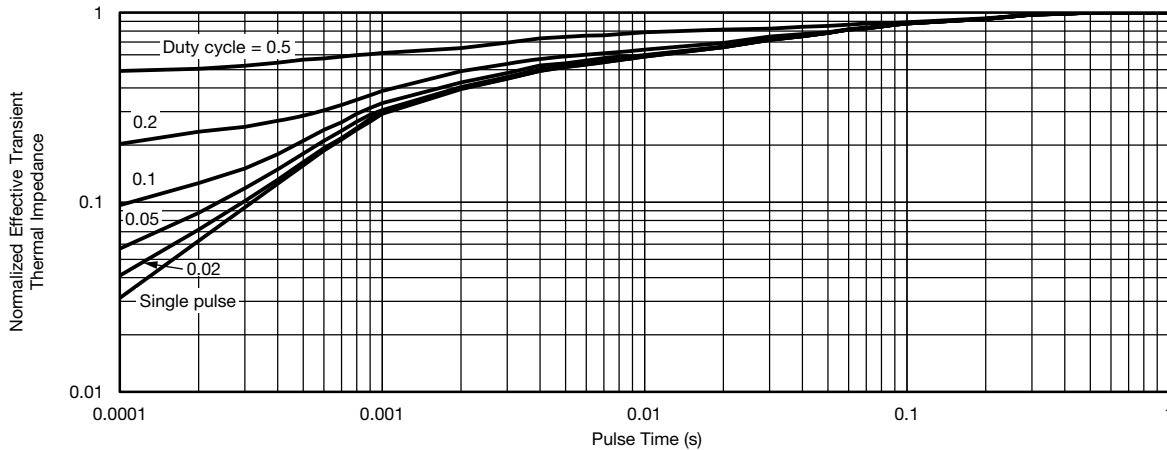


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

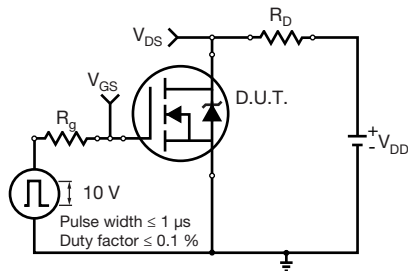


Fig. 13 - Switching Time Test Circuit



Fig. 16 - Unclamped Inductive Waveforms

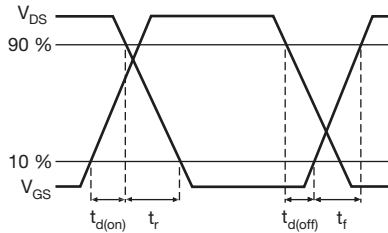


Fig. 14 - Switching Time Waveforms



Fig. 17 - Basic Gate Charge Waveform

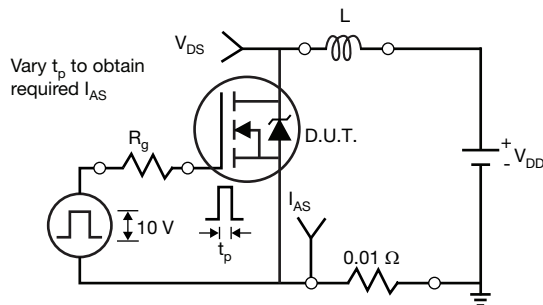
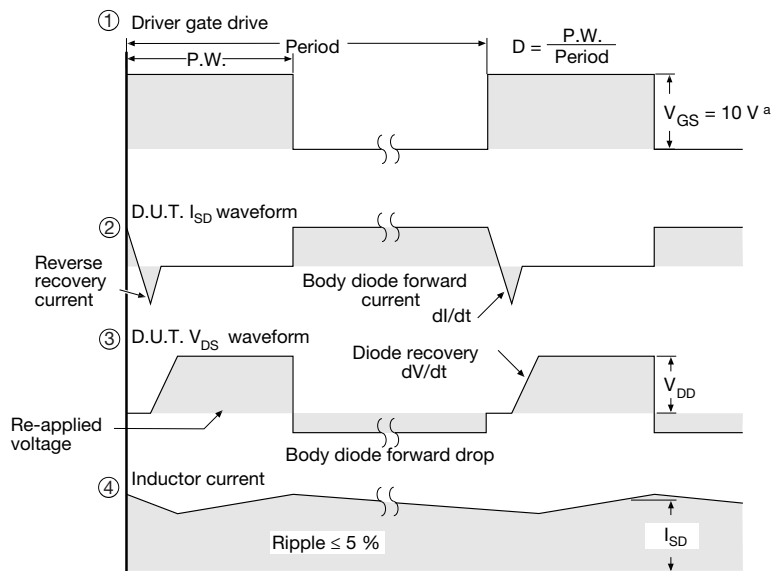
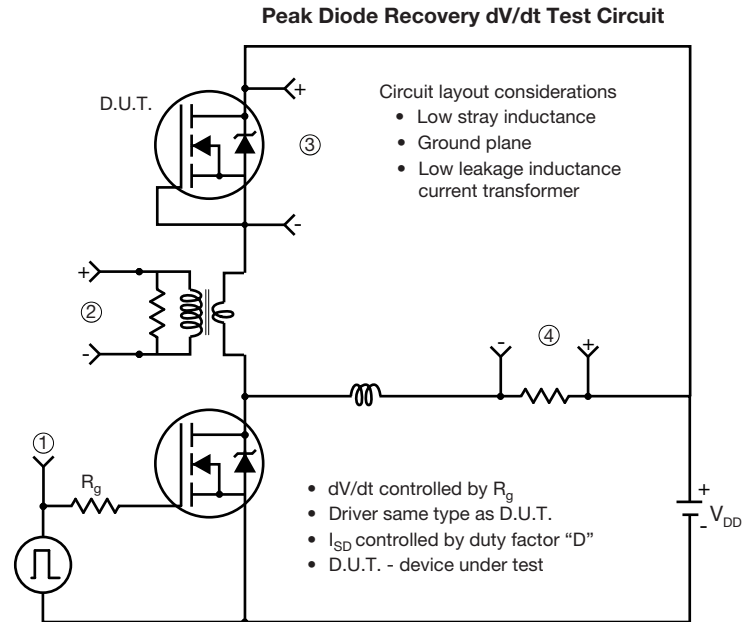


Fig. 15 - Unclamped Inductive Test Circuit



Fig. 18 - Gate Charge Test Circuit



**Note**  
 a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 19 - For N-Channel**

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### Case Outline for TO-251AA (High Voltage)

#### OPTION 1:



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

ECN: E21-0682-Rev. C, 27-Dec-2021  
DWG: 5968

#### Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension are shown in inches and millimeters
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions b4, L2, E1 and D1
- Lead dimension uncontrolled in L3
- Dimension b1, b3 and c1 apply to base metal only
- Outline conforms to JEDEC® outline TO-251AA



**OPTION 2: FACILITY CODE = N**



DIM.	MIN.	NOM.	MAX.
A	2.180	2.285	2.390
A1	0.890	1.015	1.140
b	0.640	0.765	0.890
b1	0.640	0.715	0.790
b2	0.760	0.950	1.140
b3	0.760	0.900	1.040
b4	4.950	5.205	5.460
c	0.460	-	0.610
c1	0.410	-	0.560
c2	0.460	-	0.610
D	5.970	6.095	6.220
D1	4.300	-	-

DIM.	MIN.	NOM.	MAX.
D2	5.380	-	-
E	6.350	6.540	6.730
E1	4.32	-	-
e	2.29 BSC		
L	8.890	9.270	9.650
L1	1.910	2.100	2.290
L2	0.890	1.080	1.270
L3	1.140	1.330	1.520
L4	1.300	1.400	1.500
$\theta_1$	0°	7.5°	15°
$\theta_2$	4°	-	-

ECN: E21-0682-Rev. C, 27-Dec-2021  
DWG: 5968

**Notes**

- Dimensioning and tolerancing per ASME Y14.5M-1994
- All dimension are in millimeters, angles are in degrees
- Heat sink side flash is max. 0.8 mm



## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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