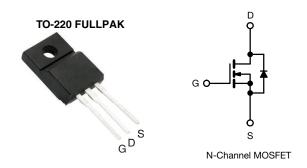


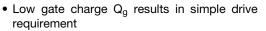


Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	650			
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V 0.93			
Q _g (Max.) (nC)	48			
Q _{gs} (nC)	12			
Q _{gd} (nC)	19			
Configuration	Single			

FEATURES





Improved gate, avalanche and dynamic dV/dt ruggedness

- Fully characterized capacitance and avalanche voltage and current
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- · High speed power switching
- High voltage isolation = 2.5 kV_{RMS} (t = 60 s, f = 60 Hz)

TYPICAL SMPS TOPOLOGIES

- · Single transistor flyback
- Single transistor forward

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIB5N65APbF

ABSOLUTE MAXIMUM RATINGS T _C :	= 25 °C, unl	ess otherwis	e noted		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V _{DS}	650	V
Gate-source voltage			V_{GS}	± 30	7 V
Continuous drain current e	V -+ 10 V	T _C = 25 °C	,	5.1	
Continuous drain current	V _{GS} at 10 V	T _C = 100 °C	I _D	3.2	Α
Pulsed drain current ^a			I _{DM}	21	
Linear derating factor				0.48	W/°C
Single pulse avalanche energy b			E _{AS}	325	mJ
Repetitive avalanche current ^a			I _{AR}	5.2	Α
Repetitive avalanche energy ^a			E _{AR}	6	mJ
Maximum power dissipation $T_C = 25 ^{\circ}C$		P_{D}	60	W	
Peak diode recovery dV/dt c			dV/dt	2.8	V/ns
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For	10 s	-	300	
Mounting torque	M3 :	screw		0.6	Nm

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Starting T_J = 25 °C, L = 24 mH, R_G = 25 Ω , I_{AS} = 5.2 A (see fig. 12)
- c. $I_{SD} \le 5.2$ A, $dI/dt \le 90$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C
- d. 1.6 mm from case
- e. Drain current limited by maximum junction temperature



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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	65	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	2.1	C/VV

PARAMETER	SYMBOL	TES	ST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static		·					
Drain-ssource breakdown voltage	V_{DS}	V _{GS}	= 0 V, I _D = 250 μA	650	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA ^d	1	670	-	mV/°C
Gate-source threshold voltage	$V_{GS(th)}$	V _{DS} =	$= V_{GS}, I_D = 250 \mu A$	2.0	-	4.0	V
Gate-source leakage	I_{GSS}		$V_{GS} = \pm 30 \text{ V}$	ı	-	± 100	nA
Zero gate voltage drain current	less	V _{DS} =	= 650 V, V _{GS} = 0 V	ı	-	25	μΑ
Zero gate voltage drain current	I _{DSS}	V _{DS} = 520 \	$V_{\rm S} = 0 \ V_{\rm T} = 125 \ ^{\circ}{\rm C}$	ı	-	250	μΛ
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.1 A ^b	1	-	0.93	Ω
Forward transconductance	9 _{fs}	V _{DS} = 50 V, I _D = 3.1 A		3.9	-	-	S
Dynamic							
Input capacitance	C_{iss}		$V_{GS} = 0 V$,	ı	1417	-	
Output capacitance	Coss		$V_{DS} = 25 \text{ V},$	ı	177	-	
Reverse transfer capacitance	C_{rss}	T = 1	.0 MHz, see fig. 5	ı	7.0	-	pF
Output capacitance	C _{oss}		V _{DS} = 1.0 V, f = 1.0 MHz	ı	1912	-	Pi
Output capacitance	Ooss	$V_{GS} = 0 V$	V _{DS} = 520 V, f = 1.0 MHz	ı	48	-	
Effective output capacitance	Coss eff.		$V_{DS} = 0 \text{ V to } 520 \text{ V}^{\text{ c}}$	ı	84	-	
Total gate charge	Q_g			-		48	
Gate-source charge	Q _{gs}	V _{GS} = 10 V	$I_D = 5.2 \text{ A}, V_{DS} = 400 \text{ V}$ see fig. 6 and 13 b	-	-	12	nC
Gate-drain charge	Q_{gd}			-	-	19	
Turn-on delay time	t _{d(on)}			-	14	-	
Rise time	t _r		= 325 V, I _D = 5.2 A	-	20	-	no
Turn-off delay time	t _{d(off)}	$R_{G} =$	9.1 Ω , R _D = 62 Ω , see fig. 10 ^b	-	34	-	ns
Fall time	t _f	1		-	18	-	
Drain-Source Body Diode Characteristic	cs	·					
Continuous source-drain diode current	I _S	MOSFET sym		ı	-	5.2	A
Pulsed diode forward current ^a	I _{SM}	integral reverse p - n junction diode		-	-	21	
Body diode voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 5.2 \text{A}, V_{GS} = 0 \text{V}^{ \text{b}}$		-	-	1.5	V
Body diode reverse recovery time	t _{rr}			-	493	739	ns
Body diode reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 5.2 \text{A}, dI/dt = 100 \text{A/}\mu\text{s}^{\text{b}}$		-	2.1	3.2	μC
Forward turn-on time	t _{on}	Intrinsic tu	ırn-on time is negligible (turn	on is dor	ninated b	y L _S and	L _D)

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %
- c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
- d. t = 60 s, f = 60 Hz



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

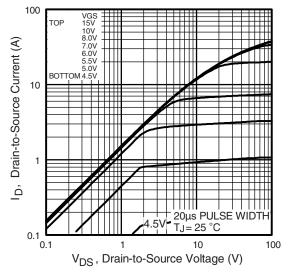


Fig. 1 - Typical Output Characteristics

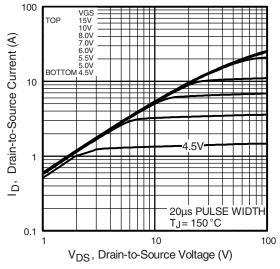


Fig. 2 - Typical Output Characteristics

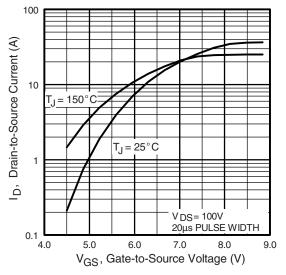


Fig. 3 - Typical Transfer Characteristics

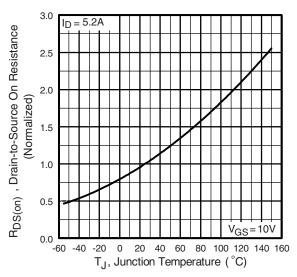


Fig. 4 - Normalized On-Resistance vs. Temperature



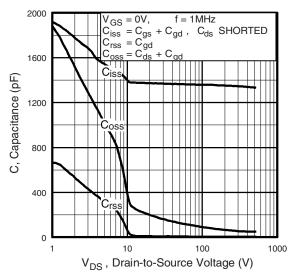


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

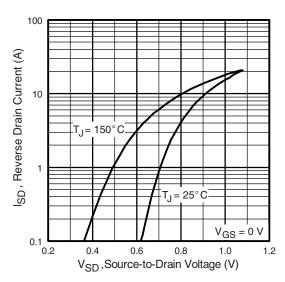


Fig. 7 - Typical Source-Drain Diode Forward Voltage

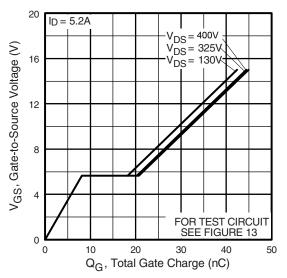


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

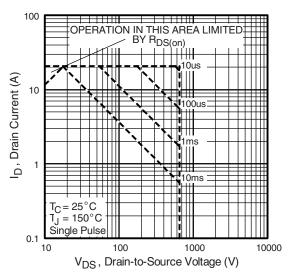


Fig. 8 - Maximum Safe Operating Area



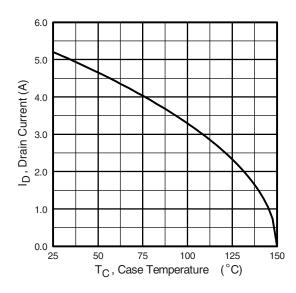


Fig. 9 - Maximum Drain Current vs. Case Temperature

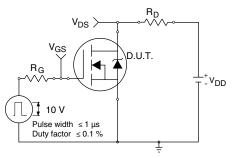


Fig. 10a - Switching Time Test Circuit

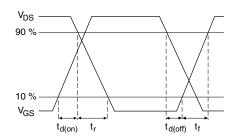


Fig. 10b - Switching Time Waveforms

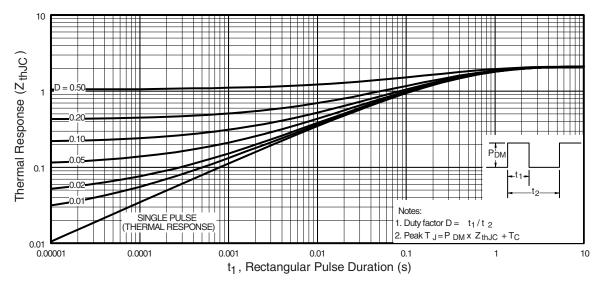


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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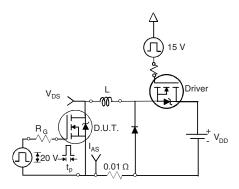


Fig. 12a - Unclamped Inductive Test Circuit

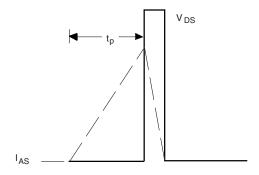


Fig. 12b - Unclamped Inductive Waveforms

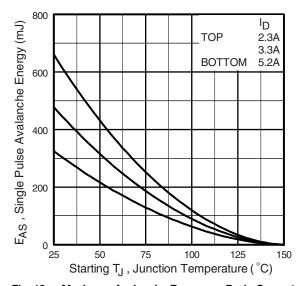


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

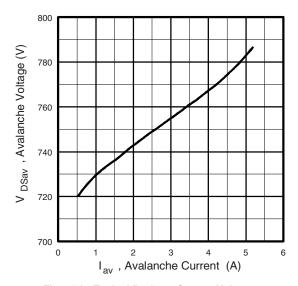


Fig. 12d - Typical Drain-to Source Voltage vs.
Avalanche Current

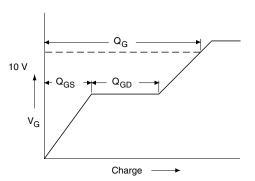


Fig. 13a - Basic Gate Charge Waveform

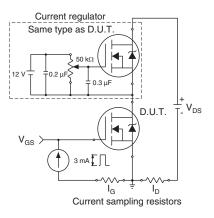
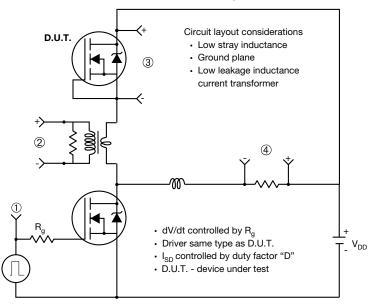


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



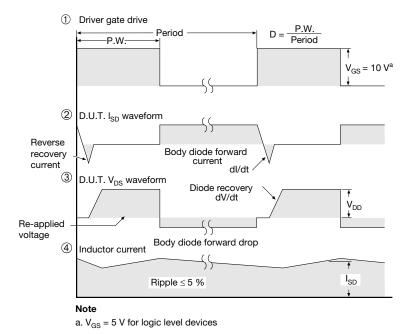


Fig. 14 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



		MILLIMETERS	
DIM.	MIN.	NOM.	MAX.
Α	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
С	0.45	0.50	0.63
D	15.80	15.87	15.97
е		2.54 BSC	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
ØR	3.08	3.18	3.28

- 1. To be used only for process drawing
- 2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
- 3. All critical dimensions should C meet $C_{pk} > 1.33$
- 4. All dimensions include burrs and plating thickness
- 5. No chipping or package damage
- 6. Facility code will be the 1st character located at the 2nd row of the unit marking



OPTION 2: FACILITY CODE = Y



	MILLIM	MILLIMETERS		ES	
DIM.	MIN.	MAX.	MIN.	N. MAX.	
Α	4.570	4.830	0.180	0.190	
A1	2.570	2.830	0.101	0.111	
A2	2.510	2.850	0.099	0.112	
b	0.622	0.890	0.024	0.035	
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	
С	0.440	0.629	0.017	0.025	
D	8.650	9.800	0.341	0.386	
d1	15.88	16.120	0.622	0.635	
d3	12.300	12.920	0.484	0.509	
Е	10.360	10.630	0.408	0.419	
е	2.54	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541	
L1	3.100	3.500	0.122	0.138	
n	6.050	6.150	0.238	0.242	
ØΡ	3.050	3.450	0.120	0.136	
u	2.400	2.500	0.094	0.098	
V	0.400	0.500	0.016	0.020	

ECN: E19-0180-Rev. D, 08-Apr-2019

DWG: 5972

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- 4. All dimensions include burrs and plating thickness
- 5. No chipping or package damage
- 6. Facility code will be the 1st character located at the 2nd row of the unit marking



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