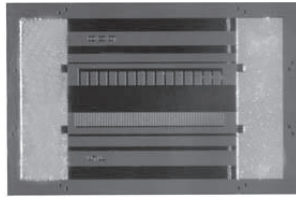


Thin Film Power Resistors



Product may not be to scale

The PWA series resistor chips offer a 500 mW power rating in a small size. These offer one of the best combinations of size and power available.

The PWAs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The PWAs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032, class H or class K.

FEATURES

- Wire bondable
- 500 mW power
- Chip size: 0.030" x 0.045"
- Case: 0503
- Resistance range 0.3 Ω to 1 M Ω
- Oxidized silicon substrate for good power dissipation
- Resistor material: tantalum nitride, self-passivating
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

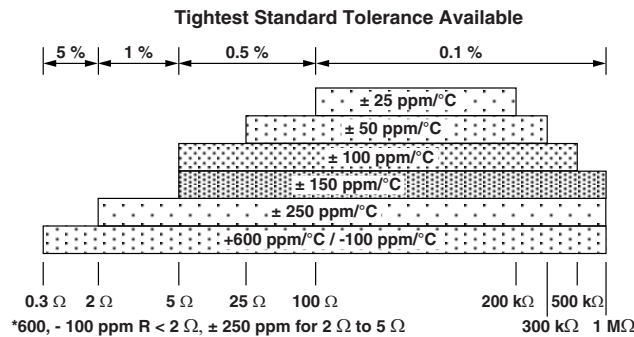


APPLICATIONS

The PWA resistor chips are used mainly in higher power circuits of amplifiers where increased power loads require a more specialized resistor.

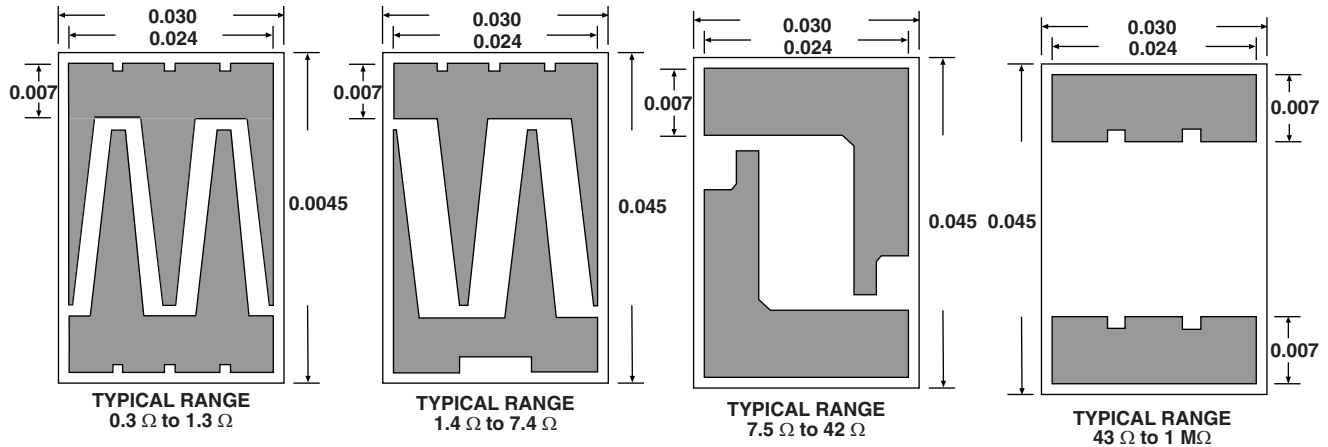
TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES

PARAMETER	VALUE	UNIT
Total Resistance Range	0.3 to 1M	Ω
Standard Tolerances	$\pm 0.1, \pm 0.5, \pm 1, \pm 5$	%
TCR	$\pm 25, \pm 50, \pm 100, \pm 150$	ppm/ $^{\circ}$ C



STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	VALUE	UNIT
Noise, MIL-STD-202, Method 308 100 Ω to 250 k Ω < 100 Ω or > 251 k Ω	-35 typ. -20 typ.	dB
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 max. $\Delta R/R$	%
Stability, 1000 h, +125 $^{\circ}$ C, 250 mW	± 0.5 max. $\Delta R/R$	%
Operating Temperature Range	-55 to +125	$^{\circ}$ C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.1 max. $\Delta R/R$	%
High Temperature Exposure, +150 $^{\circ}$ C, 100 h	± 0.2 max. $\Delta R/R$	%
Dielectric Voltage Breakdown	200	V
Insulation Resistance	10^{12} min.	Ω
Operating Voltage Steady State 5 x Rated Power	100 max. 200 max.	V
DC Power Rating at +70 $^{\circ}$ C (Derated to zero at +175 $^{\circ}$ C) (Conductive epoxy die attach to alumina substrate)	0.5	W
5 x Rated Power Short-Time Overload, +25 $^{\circ}$ C, 5 s	± 0.1 max. $\Delta R/R$	%

DIMENSIONS in inches

SCHEMATIC


MECHANICAL SPECIFICATIONS	
PARAMETER	VALUE
Chip Size	0.030" x 0.045" ± 0.002" (0.762 mm x 1.143 mm ± 0.5 mm)
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.007" x 0.024" (0.1778 mm x 0.6096 mm)
Number of Pads	2
Pad Material	10 kÅ minimum aluminum (Au optional)
Backing	None, lapped semiconductor silicon (Au back optional)

GLOBAL PART NUMBER INFORMATION													
Global Part Number: PWA50000FKANHWS													
Global Part Number Description: PWA 5K 1% 100 ppm Al None H WS													
P	W	A	5	0	0	0	F	K	A	N	H	W	S
MODEL	RESISTANCE	RESISTANCE MULTIPLIER CODE	TOLERANCE CODE (%)	TCR (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE					
PWA 30 x 45 size Power resistor	First 4 digits are significant figures of resistance	D = 0.0001 C = 0.001 B = 0.01 A = 0.1 0 = 1 1 = 10 2 = 100 3 = 1000	B = 0.1 C = 0.25 D = 0.5 F = 1.0 G = 2.0 H = 2.5 J = 5.0 K = 10	E = ± 25 C = ± 50 K = ± 100 V = ± 150 L = ± 200 M = ± 250 Z = +600 / -100	G = Au A = Al	G = Au N = none	H = class H K = class K	WS = waffle pack 100 min, 1 mult.					



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