

## High Stability - High Temperature (230 °C) Thin Film Wraparound Chip Resistors, Sulfur Resistant


**DESIGN SUPPORT TOOLS**
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**INTRODUCTION**

For applications such as down hole applications, the need for parts able to withstand very severe conditions (temperature as high as 215 °C powered or up to 230 °C un-powered) has led Vishay Sfernice to push out the limit of the thin film technology.

Designers might read the application note: Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (P, PRA etc...) (High Temperature Application) [www.vishay.com/doc?53047](http://www.vishay.com/doc?53047) in conjunction with this datasheet to help them to properly design their PCBs and get the best performances of the PHT.

Vishay Sfernice R&D engineers will be willing to support any customer design considerations.

**FEATURES**

- Operating temperature range: -55 °C; +215 °C
- Storage temperature: -55 °C; +230 °C
- Gold terminations (< 1 μm thick)
- 5 sizes available (0402, 0603, 0805, 1206, 2010); other sizes upon request
- Temperature coefficient down to 15 ppm (-55 °C; +215 °C)
- Tolerance down to 0.05 %
- Load life stability: 0.35 % max. after 2000 h at 220 °C (ambient) at Pn
- Shelf life stability: 0.7 % typ. (1 % max.) after 15 000 h at 230 °C
- SMD wraparound
- TCR remains constant after long term storage at 230 °C (15 000 h)
- Sulfur resistant (per ASTM B809-95 humid vapor test)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
**GREEN**  
(5-2008)

**STANDARD ELECTRICAL SPECIFICATIONS**

MODEL	SIZE	RESISTANCE RANGE Ω	RATED POWER <sup>(1)(2)</sup> P <sub>215 °C</sub> W	LIMITING ELEMENT VOLTAGE V	TOLERANCE <sup>(2)</sup> ± %	TEMPERATURE COEFFICIENT <sup>(3)</sup> ± ppm/°C
PHT0402	0402	10 to 130K	0.0189	50	0.05, 0.1, 0.5, 1	10, 15, 25, 30, 50, 55
PHT0603	0603	10 to 320K	0.0375	75	0.05, 0.1, 0.5, 1	10, 15, 25, 30, 50, 55
PHT0805	0805	10 to 720K	0.06	150	0.05, 0.1, 0.5, 1	10, 15, 25, 30, 50, 55
PHT1206	1206	10 to 2.7M	0.1	200	0.05, 0.1, 0.5, 1	10, 15, 25, 30, 50, 55
PHT2010	2010	10 to 7.5M	0.2 <sup>(4)</sup>	300	0.05, 0.1, 0.5, 1	10, 15, 25, 30, 50, 55

**Notes**

- (1) For power handling improvement, please refer to application note 53047: "Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (High Temperature Applications)" [www.vishay.com/doc?53047](http://www.vishay.com/doc?53047) and consult Vishay Sfernice
- (2) See Table 2 on next page
- (3) See Table 1 on next page
- (4) It is possible to dissipate up to 0.3 W, but there will be an additional drift of 0.1 % after load life

**CLIMATIC SPECIFICATIONS**

Operating temperature range	-55 °C; +215 °C
Storage temperature range	-55 °C; +230 °C

**PERFORMANCE VS. HUMID SULFUR VAPOR**

Test conditions	50 °C ± 2 °C, 85 % ± 4 % RH, exposure time 500 h
Test results	Resistance drift < (0.05 % R + 0.05 Ω), no corrosion products observed

**MECHANICAL SPECIFICATIONS**

Substrate	Alumina
Resistive Element	Nichrome (NiCr)
Passivation	Silicon nitride (Si <sub>3</sub> N <sub>4</sub> )
Protection	Epoxy + silicone
Terminations	Gold (< 1 μm) over nickel barrier

**Note**

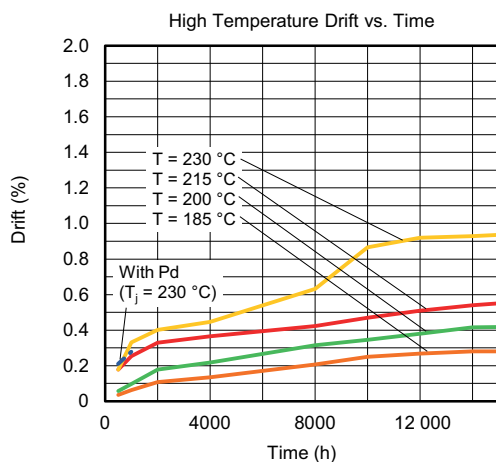
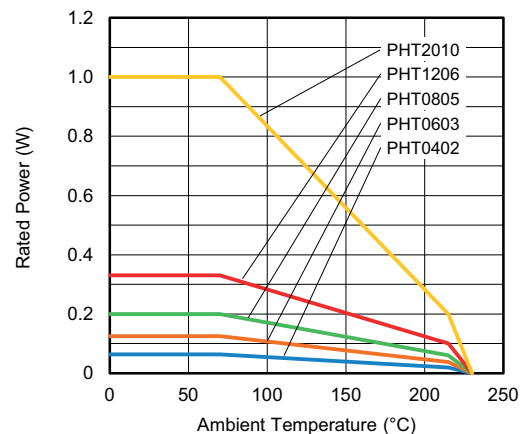
- For other terminations, please consult

**TABLE 1 - TEMPERATURE COEFFICIENT**

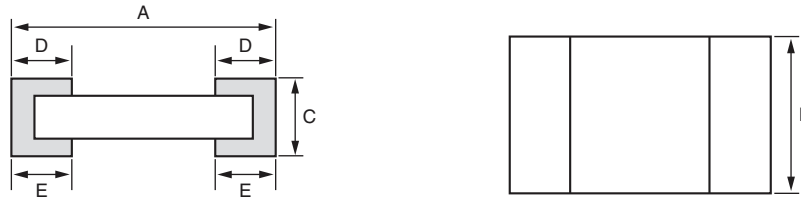
Y	10 ppm/°C	-55 °C; +155 °C
	15 ppm/°C	-55 °C; +215 °C
E	25 ppm/°C	-55 °C; +155 °C
	30 ppm/°C	-55 °C; +215 °C
H	50 ppm/°C	-55 °C; +155 °C
	55 ppm/°C	-55 °C; +215 °C

**TABLE 2 - BEST TOLERANCE AND TCR VS. OHMIC VALUE**

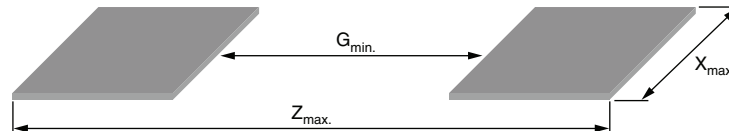
SERIES	RANGE ( $\Omega$ )	TOL. ( $\pm$ %)	TCR CODE
0402	10 to 50	0.1; 0.5; 1	Y; E; H
	> 50 to 90K	0.05; 0.1; 0.5; 1	Y; E; H
	> 90K to 130K	0.05; 0.1; 0.5; 1	E; H
0603	10 to 50	0.1; 0.5; 1	Y; E; H
	> 50 to 210K	0.05; 0.1; 0.5; 1	Y; E; H
	> 210K to 320K	0.05; 0.1; 0.5; 1	E; H
0805	10 to 50	0.1; 0.5; 1	Y; E; H
	> 50 to 480K	0.05; 0.1; 0.5; 1	Y; E; H
	> 480K to 720K	0.05; 0.1; 0.5; 1	E; H
1206	10 to 50	0.1; 0.5; 1	Y; E; H
	> 50 to < 1.8M	0.05; 0.1; 0.5; 1	Y; E; H
	> 1.8M to 2.7M	0.05; 0.1; 0.5; 1	E; H
2010	10 to 50	0.1; 0.5; 1	Y; E; H
	> 50 to 5M	0.05; 0.1; 0.5; 1	Y; E; H
	> 5M to 7.5M	0.05; 0.1; 0.5; 1	E; H

**PHT STABILITY CURVE**

**POWER DERATING CURVE**

**Note**

- Stability will be dependent on resistivity of resistor. Above curves are worst case.

**DIMENSIONS** in millimeters (inches)


CASE SIZE	A	B	C	D/E	
	MAX. TOL. +0.152 (+0.006) MIN. TOL. -0.152 (-0.006)	MAX. TOL. +0.127 (+0.005) MIN. TOL. -0.127 (-0.005)		NOMINAL	TOLERANCE
	NOMINAL	NOMINAL		NOMINAL	TOLERANCE
0402	1.00 (0.039)	0.60 (0.024)	Termination N: 0.5 (0.02) ± 0.127 (0.005)  Termination G: 0.4 (0.016) ± 0.051 (0.002)	0.25 (0.010)	0.1 (0.004)
0603	1.52 (0.060)	0.85 (0.033)		0.38 (0.015)	0.13 (0.005)
0805	1.91 (0.075)	1.27 (0.050)		0.40 (0.016)	
1206	3.06 (0.120)	1.60 (0.063)		0.48 (0.019)	
2010	5.08 (0.200)	2.54 (0.100)			

**SUGGESTED LAND PATTERN (TO IPC-7351A)**


CHIP SIZE	DIMENSIONS (in millimeter)		
	Z <sub>max.</sub>	G <sub>min.</sub>	X <sub>max.</sub>
0402	1.55	0.15	0.73
0603	2.37	0.35	0.98
0805	2.76	0.74	1.40
1206	3.91	1.85	1.73
2010	5.93	3.71	2.67

**Caution:**

Performances obtained with following mounting conditions:

PCB: polyimide

Solder paste: PbSnAg (93.5/5/1.5)

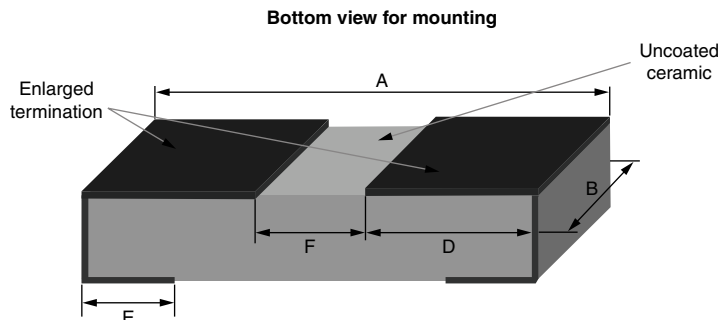
**POPULAR OPTIONS**

It is recommended to consult Vishay Sfernice for availability first.

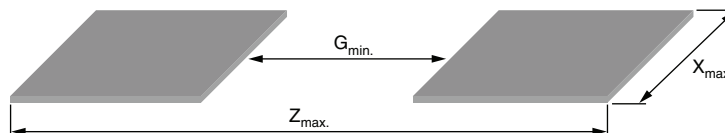
**Option: Enlarged terminations:**

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heatsink (see application note: 53048 "Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film)" [www.vishay.com/doc?53048](http://www.vishay.com/doc?53048)).

Option to order: 0063 (applies to size 1206 / 2010).

**DIMENSIONS** (Option 0063) in millimeters


CASE SIZE	A	B	E	D	F		
	MAX. TOL. +0.152 MIN. TOL. -0.152	MAX. TOL. +0.127 MIN. TOL. -0.127	MAX. TOL. +0.13 MIN. TOL. -0.13	MAX. TOL. +0.13 MIN. TOL. -0.13	NOMINAL	MIN.	MAX.
	NOMINAL	NOMINAL	NOMINAL	NOMINAL			
1206	3.06	1.60	0.40	1.215	0.63	0.50	0.76
2010	5.08	2.54	0.48	2.25			

**SUGGESTED LAND PATTERN** (Option 0063)


CHIP SIZE	DIMENSIONS (in millimeter)		
	Z <sub>max.</sub>	G <sub>min.</sub>	X <sub>max.</sub>
1206	3.91	0.50	1.73
2010	5.93		2.67



PACKAGING

ESD packaging available: waffle-pack and plastic tape and reel (low conductivity). Paper tape available upon request (for sizes 0402, 0603, 0805 and 1206).

Table with columns: SIZE, MOQ, NUMBER OF PIECES PER PACKAGE (WAFFLE PACK 2" x 2", TAPE AND REEL MIN., MAX.), TAPE WIDTH. Rows include sizes 0402, 0603, 0805, 1206, 2010.

Note (1) 12 mm on request

PACKAGING RULES

Waffle Pack

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover.

To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code.

Tape and Reel

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided.

When several reels are needed for ordered quantity within MOQ and maximum reel capacity: please consult Vishay Sfernice for specific ordering code.

GLOBAL PART NUMBER INFORMATION table showing breakdown of PHT1206Y1001BGT063 into fields like GLOBAL MODEL, SIZE, TCR, VALUE, TOLERANCE, TERMINATION, PACKAGING, and OPTION.

Note (1) For usage at temperatures up to 200 °C maximum N (tin/silver termination are available upon request)

CODIFICATION OF PACKAGING table mapping codes (W, WA, T, TA, TB, TC, TD, TE, TF, PT, PA, PB, PC, PD, PE, PF) to packaging types and quantities.



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