1、General Description

GN1640 is a LED (Light Emitting Diode Display) drive control circuit integrating MCU digital interface, digital latch, LED drive circuit, etc. The product has excellent performance and reliable quality, and is mainly applied in display drive for electronic scales and other small home appliances.

Features

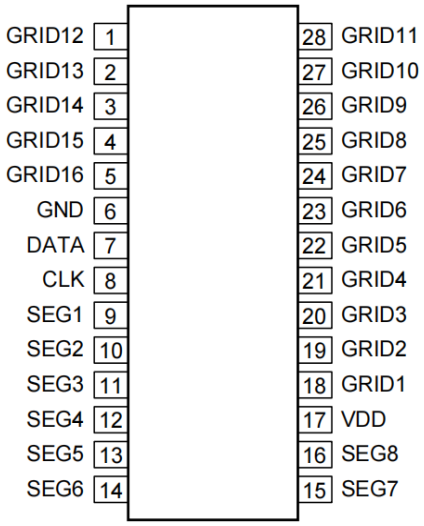
- Power CMOS technique
- Brightness adjusting circuit：duty cycle adjustable among 8 levels
- Display mode: 8 segment×16 grid
- Dual-line serial interface :SCLK, DIN
- Built-in RC oscillation
- Built-in power-on reset circuit
- Built-in auto blanking circuit

Packaging from

GN1640	SOP28	25PCS/tube	2000PCS/box	20000PCS/box(Size of plastic body：17.9mm×7.55mm Pin Spacing：1.27mm)
GN1640T	SSOP28	50PCS/tube	10000PCS/box	50000PCS/box(Size of plastic body：9.9mm×3.9mm Pin Spacing：0.635mm)

2、Block Diagram And Pin Description

2.1、Pin Configurations



SOP28/SSOP28

2.2、Pin Description

Pin No. SOP28/SSOP28	Pin Name	I/O	Description
1	GRID12	O	Grid output. N tube open drain output

2	GRID13	O	Grid output. N tube open drain output
3	GRID14	O	Grid output. N tube open drain output
4	GRID15	O	Grid output. N tube open drain output
5	GRID16	O	Grid output. N tube open drain output
6	GND	-	Logic grounding. Connect to system grounding
7	DATA	I	Serial data input. Input data changed at low level of SCLK
8	CLK	I	Clock input. Input data at rising edge
9	SEG1	O	Segment output. P tube open drain output
10	SEG2	O	Segment output. P tube open drain output
11	SEG3	O	Segment output. P tube open drain output
12	SEG4	O	Segment output. P tube open drain output
13	SEG5	O	Segment output. P tube open drain output
14	SEG6	O	Segment output. P tube open drain output
15	SEG7	O	Segment output. P tube open drain output
16	SEG8	O	Segment output. P tube open drain output
17	VDD	-	Logic power supply
18	GRID1	O	Grid output. N tube open drain output
19	GRID2	O	Grid output. N tube open drain output
20	GRID3	O	Grid output. N tube open drain output
21	GRID4	O	Grid output. N tube open drain output
22	GRID5	O	Grid output. N tube open drain output
23	GRID6	O	Grid output. N tube open drain output
24	GRID7	O	Grid output. N tube open drain output
25	GRID8	O	Grid output. N tube open drain output
26	GRID9	O	Grid output. N tube open drain output
27	GRID10	O	Grid output. N tube open drain output
28	GRID11	O	Grid output. N tube open drain output

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Tamb=25℃,All voltage referenced to VSS,unless otherwise specified)

Characteristic	Symbol	Condition	Value	Unit
Power Supply Voltage	VDD	-	-0.5～7.0	V
Input Voltage	V_{IN}	-	-0.5～VDD+0.5	V
LED SEG drive output current	I_{O1}	-	-50	mA
LED GRID drive output current	I_{O2}	-	+150	mA
Operating Temperature	T_{amb}	-	-40～+85	℃
Storage Temperature	T_{stg}	-	-65～150	℃
Soldering Temperature	T_L	10s	260	℃

3.2、Recommended Operating Range

Parameter	Symbol	Min	Typ	Max	Unit
Logic Supply Voltage	VDD	3	5	5.5	V
High-level Input Voltage	V_{IH}	0.7VDD	-	VDD	V
Low-level Input Voltage	V_{IL}	0	-	0.2VDD	V

3.3、Electrical Characteristics

3.3.1、AC Characteristics

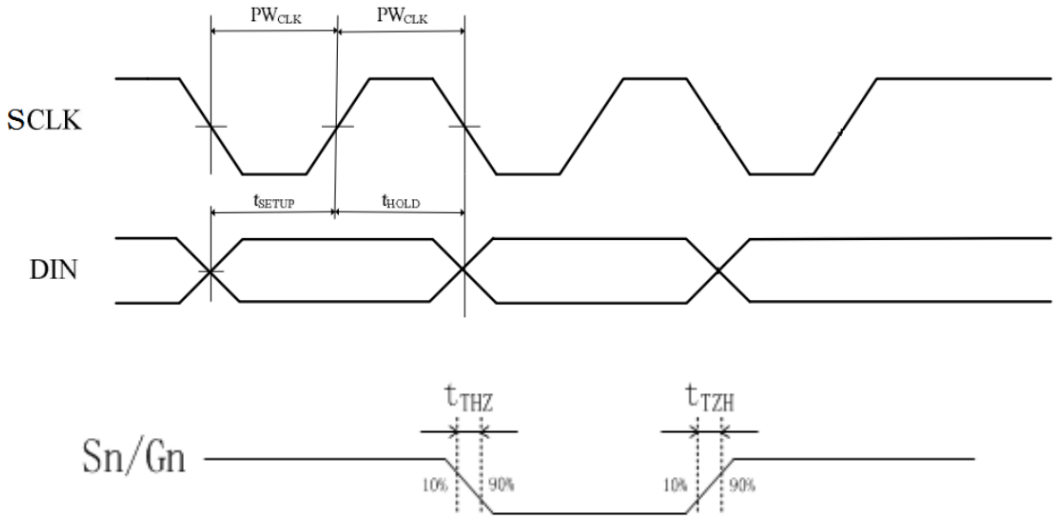
(VDD=4.5V～5.5V,VSS=0V,unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Oscillation	f_{osc}	-		-	400	-	kHz
Rise time	T_{TZH1}	C_L=300pF	SEG1～SEG8	-	-	2	us
	T_{TZH2}		GRID1～GRID16	-	-	0.5	us
Fall time	T_{THZ}	C_L=300Pf, SEGn, GRIDn		-	-	120	us
Maximum clock	f_{MAX}	50%duty cycle		1	-	-	MHz

3.3.2、AC Characteristics

(VDD=4.5V～5.5V,VSS=0V,unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock pulse width	PWCLK	-	400	-	-	ns
Data setup time	tSETUP	-	100	-	-	ns
Data hold time	tHOLD	-	100	-	-	ns



3.3.3、DC Characteristics

(VDD=5V,VSS=0V,unless otherwise specified.)

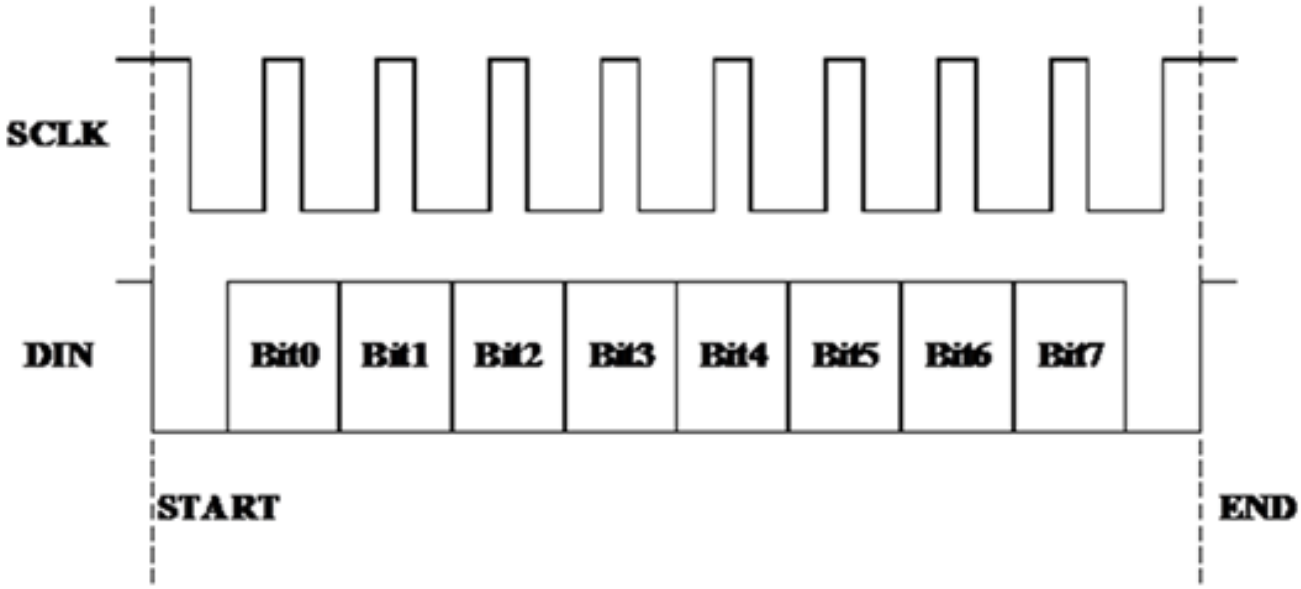
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level output current	I_{OH1}	SEG1～SEG8, V_{OH}=VDD-2V	-	-60	-	mA
	I_{OH2}	SEG1～SEG8, V_{OH}=VDD-3V	-	-70	-	mA
Low level output	I_{OL}	GRID1～GRID16, V_{OL}=0.3V	80	100	-	mA
Segment High-level Output Current Tolerance	I_{TOLSG}	SEG1～SEG8, V_{OH}=VDD-3V	-	-	5	%
High level input	V_{IH}	DIN, SCLK	0.7VDD	-	-	V
Low level input	V_{IL}	DIN, SCLK	-	-	0.2VDD	V
Hysteresis voltage	V_H	DIN, SCLK	-	0.35	-	V
Input leakage	I_I	V_{IN}=VDD or VSS	-	-	±1	uA
Supply current	I_{DD}	No load, V_{IN}=VDD	-	150	-	uA

4、Interface Description

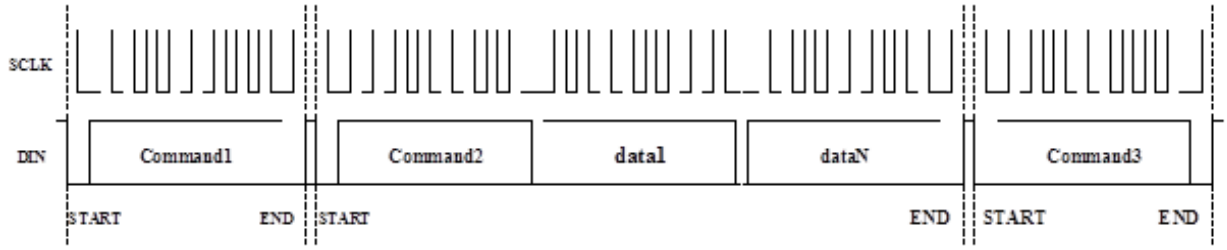
Data in microprocessor communicate with GN1640 through the bus interface. During data input, if SCLK is at high level, the signal on DIN shall remain unchanged; it can only be changed if the clock signal on SCLK is at low level. Low level of data inputs are always transmitted before high level.

The starting condition of data input is: when SCLK is high, the DIN becomes low from high; the ending condition is: when SCLK is high, the DIN becomes high from low.

Transmission process of command data is shown in the following figure:



4.1、Write SRAM data address self-add mode



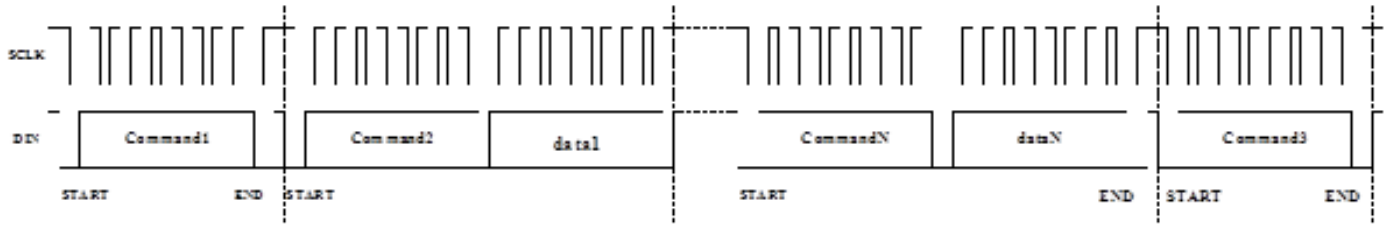
Command1:Data set command

Command2:Address setting command

data1～dataN:Display data

Command3:Display control command

4.2、Write SRAM data fixed address mode



Command1:Data set command
Command2:Address setting command
data1:Display data
Commandn:Address setting command
datan:Display data
Command3:Display control command

5、Command Description

Commands are used to set display modeand status of LED driver.
When “start”command becomes valid, the first byte input by DIN is taken as the firstcommand. Through decoding, the highest B7 and B6 bits are adopted to distinguish differentcommands.

Bit7	Bit6	Command
0	1	Data set command
1	0	Display control command
1	1	Address setting command

If “end”becomes valid during transmission of command or data, the serial communication will be initialized and the commands or data under transmission will become invalid (those completed transmission will remain valid).

5.1、Data Set Command

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
0	1	Fill in 0 for items not applicable		0	0	Fill in 0 for items not applicable		Address auto +1
0	1			0	1			Fixed address
0	1			0	-			Normal mode
0	1			1	-			Testing mode(internal use)

5.2、Address Setting Command

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	显示地址	GRIDn

1	1	Fill in 0 for items not applicable	0	0	0	0	00H	GRID1
1	1		0	0	0	1	01H	GRID2
1	1		0	0	1	0	02H	GRID3
1	1		0	0	1	1	03H	GRID4
1	1		0	1	0	0	04H	GRID5
1	1		0	1	0	1	05H	GRID6
1	1		0	1	1	0	06H	GRID7
1	1		0	1	1	1	07H	GRID8
1	1		1	0	0	0	08H	GRID9
1	1		1	0	0	1	09H	GRID10
1	1		1	0	1	0	0AH	GRID11
1	1		1	0	1	1	0BH	GRID12
1	1		1	1	0	0	0CH	GRID13
1	1		1	1	0	1	0DH	GRID14
1	1		1	1	1	0	0EH	GRID15
1	1		1	1	1	1	0FH	GRID16

When power-on, the default address isset as 00H.

The relationships between display data, chip pins and display addresses are shown in thefollowing table:

SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Display memory address 00H								GRID1
Display memory address 01H								GRID2
Display memory address 02H								GRID3
Display memory address 03H								GRID4
Display memory address 04H								GRID5
Display memory address 05H								GRID6
Display memory address 06H								GRID7
Display memory address 07H								GRID8
Display memory address 08H								GRID9
Display memory address 09H								GRID10
Display memory address 0AH								GRID11
Display memory address 0BH								GRID12
Display memory address 0CH								GRID13
Display memory address 0DH								GRID14
Display memory address 0EH								GRID15
Display memory address 0FH								GRID16

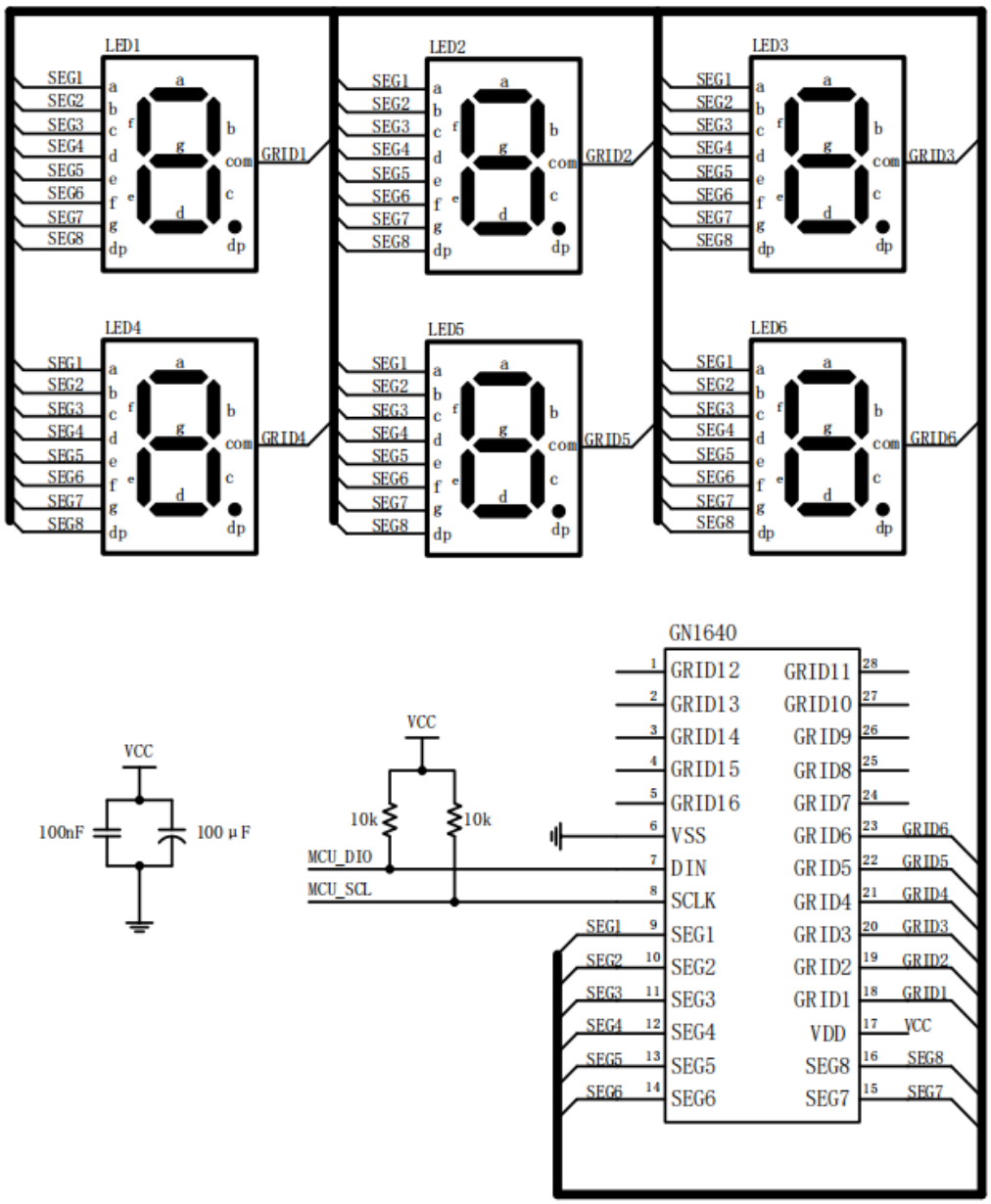
5.3、Display Control Command

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Description
1	0			1	0	0	0		Set pulse width to 1/16
1	0			1	0	0	1		Set pulse width to 2/16

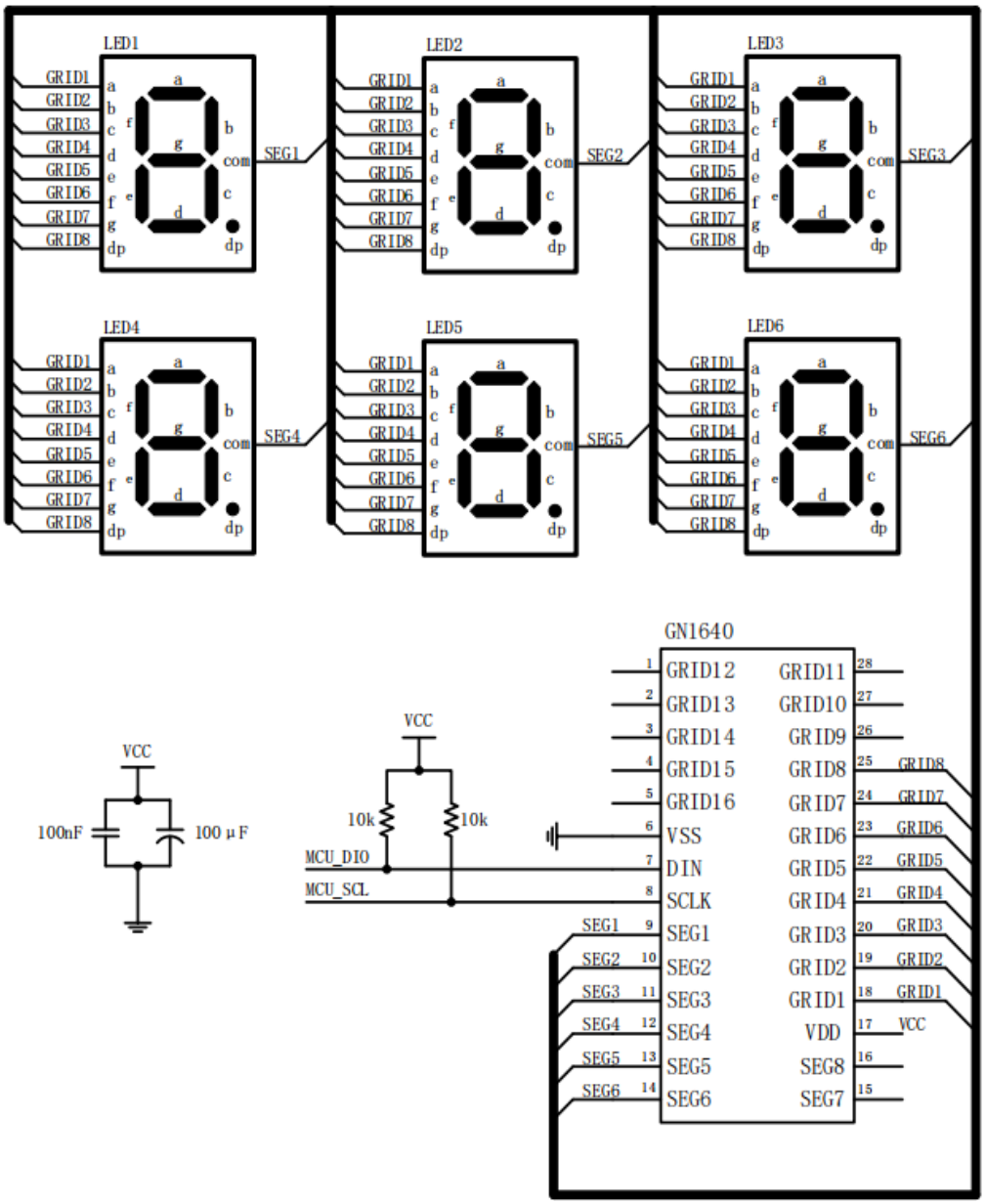
1	0	Fill in 0 foritems not applicable	1	0	1	0	Extinction quantity setting (brightness setting)	Set pulse width to 4/16
1	0		1	0	1	1		Set pulse width to 10/16
1	0		1	1	0	0		Set pulse width to 11/16
1	0		1	1	0	1		Set pulse width to 12/16
1	0		1	1	1	0		Set pulse width to 13/16
1	0		1	1	1	1		Set pulse width to 14/16
1	0		0	X	X	X	Display switch control	Display OFF
1	0		1	X	X	X		Display ON

6、Typical ApplicationCircuitAnd Application Note

6.1、TypicalApplication Circuit of Common Cathode Digital Tube



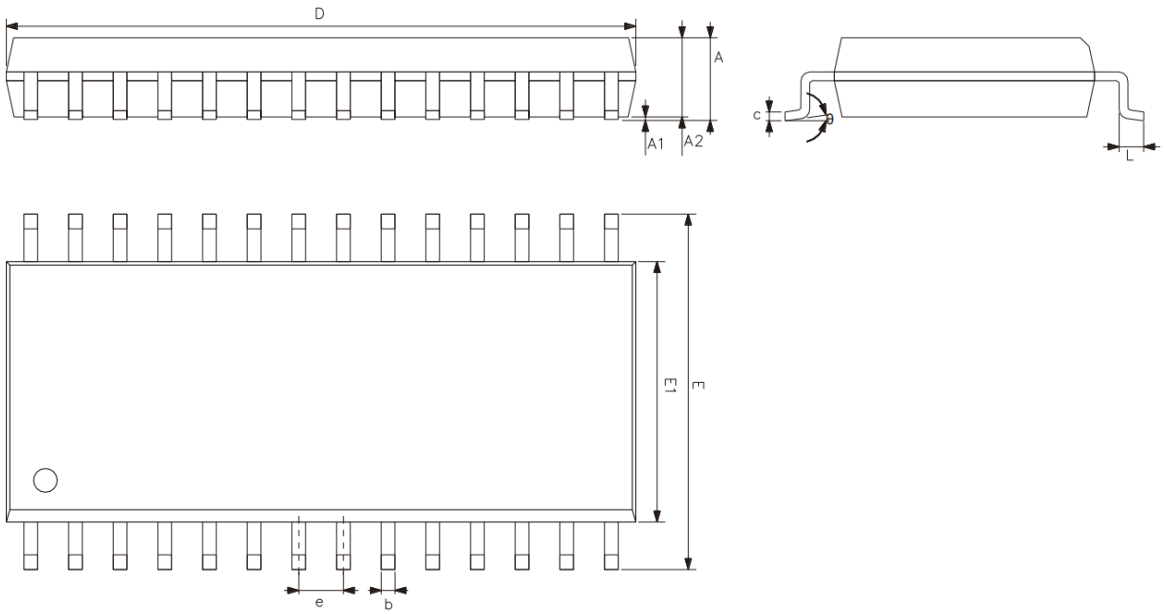
6.2、TypicalApplication Circuit of CommonAnode Digital Tube



Note: The capacitor is necessary between VDD and VSS, which recommended 100uF and 104.And PCB layout as close as possible to the chip pin.

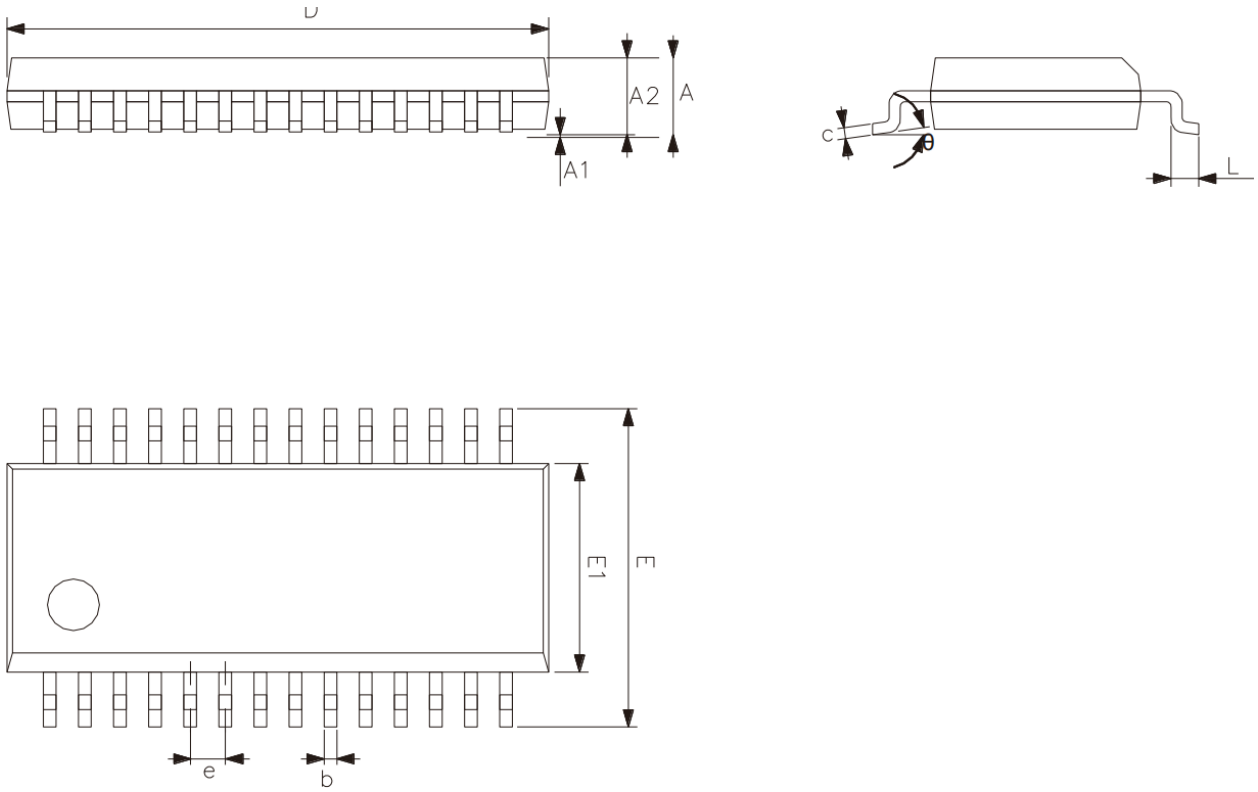
7、Package Dimensions and Outline Drawings

7.1、SOP-28 Outline Drawings and Package Dimensions



Symbol	Dimensions(mm)	
	Min.	Max.
A	2.15	2.75
A1	0.03	0.30
A2	2.05	2.44
b	0.35	0.51
c	0.20	0.36
D	17.70	18.30
E	10.00	10.65
E1	7.30	7.70
e	1.27	
L	0.40	1.27
θ	0°	8°

7.2、SSOP-28(0.635mm) Outline Drawings and Package Dimensions



Symbol	Dimensions(mm)	
	Min.	Max.
A	-	1.75
A1	0.02	0.25
A2	1.30	1.60
b	0.23	0.31
c	0.19	0.25
D	9.75	10.00
E	5.80	6.45
E1	3.75	4.00
e	0.635	
L	0.35	0.80
θ	0°	8°

8、StatementsAnd Notes

8.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
Explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

8.2、Notes

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