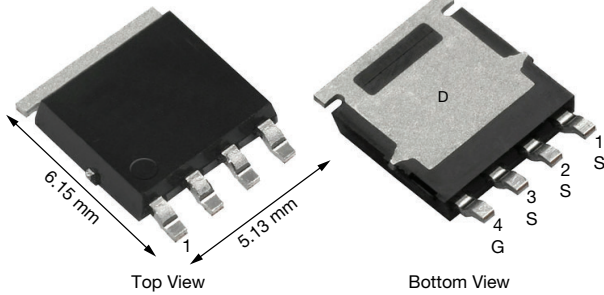


N-Channel 45 V (D-S) MOSFET

PowerPAK® SO-8L Single



FEATURES

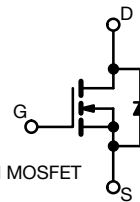
- TrenchFET® Gen IV power MOSFET
- Very low Q_g and Q_{oss} reduce power loss and improve efficiency
- Flexible leads provide resilience to mechanical stress
- 100 % R_g and UIS tested
- Q_{gd}/Q_{gs} ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- DC/AC inverters



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	45
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00283
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00410
Q_g typ. (nC)	21.4
I_D (A) ^a	110
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SiJ150DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	45	V	
Gate-source voltage	V_{GS}	+20, -16		
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	110	A
		$T_C = 70$ °C	88	
		$T_A = 25$ °C	30.9 ^{b, c}	
		$T_A = 70$ °C	24.6 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	300	A	
Continuous source-drain diode current	I_S	$T_C = 25$ °C		
		$T_A = 25$ °C	3 ^{b, c}	
Single pulse avalanche current	I_{AS}	30	mJ	
Single pulse avalanche energy	E_{AS}	45		
Maximum power dissipation	P_D	$T_C = 25$ °C	65.7	W
		$T_C = 70$ °C	42	
		$T_A = 25$ °C	5.2 ^{b, c}	
		$T_A = 70$ °C	3.3 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^{b, f}	R_{thJA}	20	25	°C/W	
Maximum junction-to-case (drain)	R_{thJC}	1.5	1.9		

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 62.5 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	45	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 1 mA	-	28	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-5.4	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.1	-	2.3	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 45 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 45 V, V _{GS} = 0 V, T _J = 75 °C	-	-	20	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	-	0.00225	0.00283	Ω
		V _{GS} = 4.5 V, I _D = 15 A	-	0.00310	0.00410	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 15 A	-	72	-	S
Dynamic ^b						
Input capacitance	C _{ISS}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	4000	-	pF
Output capacitance	C _{OSS}		-	630	-	
Reverse transfer capacitance	C _{RSS}		-	56	-	
C _{RSS} /C _{ISS} ratio			-	0.014	0.028	
Total gate charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 15 A	-	46.7	70	nC
		V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 15 A	-	21.4	32	
Gate-source charge	Q _{gs}		-	11.1	-	
Gate-drain charge	Q _{gd}		-	3.6	-	
Output charge	Q _{OSS}	V _{DS} = 20 V, V _{GS} = 0 V	-	28	-	
Gate resistance	R _g	f = 1 MHz	0.5	1.15	2	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	15	30	ns
Rise time	t _r		-	6	12	
Turn-off delay time	t _{d(off)}		-	30	60	
Fall time	t _f		-	6	12	
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	30	60	
Rise time	t _r		-	67	134	
Turn-off delay time	t _{d(off)}		-	28	56	
Fall time	t _f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	59.7	A
Pulse diode forward current (t _p = 100 μs)	I _{SM}		-	-	300	
Body diode voltage	V _{SD}	I _S = 5 A	-	0.72	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 15 A, di/dt = 100 A/μs, T _J = 25 °C	-	32	64	ns
Body diode reverse recovery charge	Q _{rr}		-	24	48	nC
Reverse recovery fall time	t _a		-	17	-	ns
Reverse recovery rise time	t _b		-	15	-	

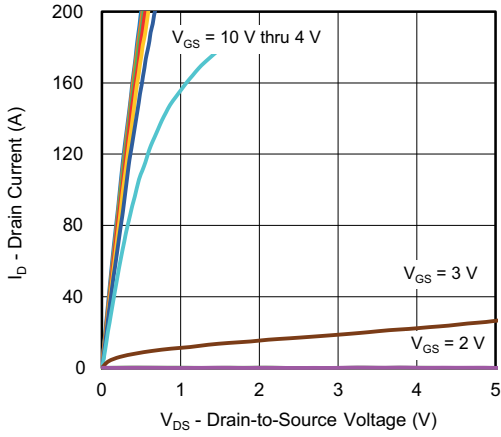
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing

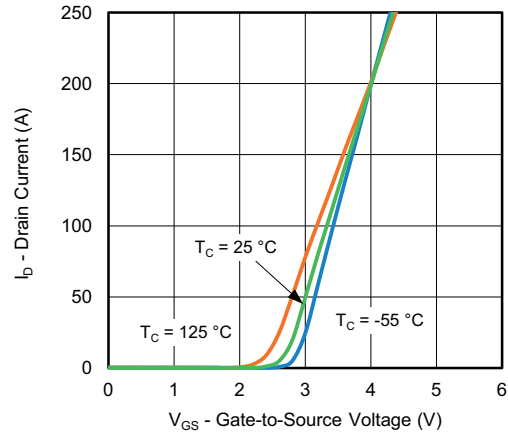
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



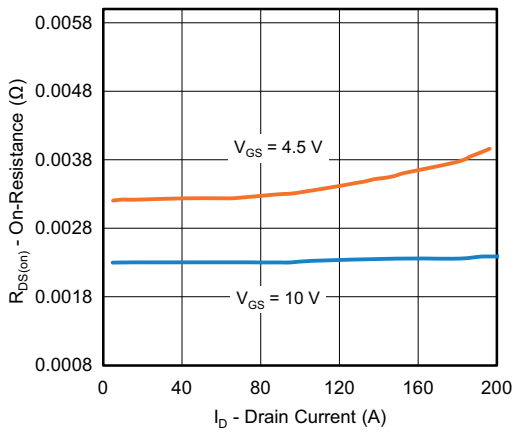
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



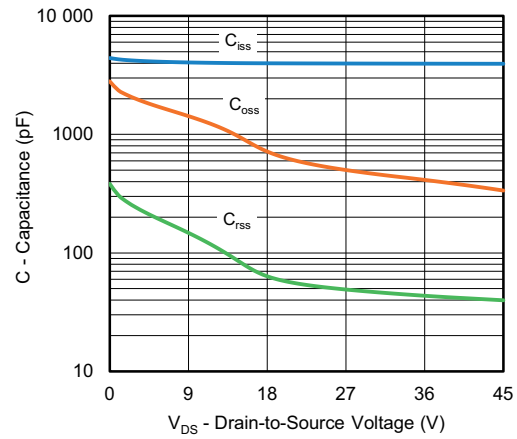
Output Characteristics



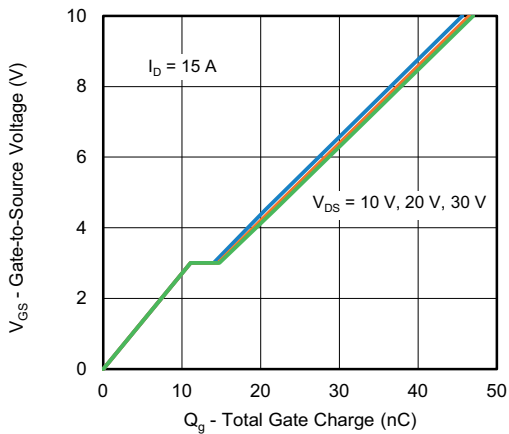
Transfer Characteristics



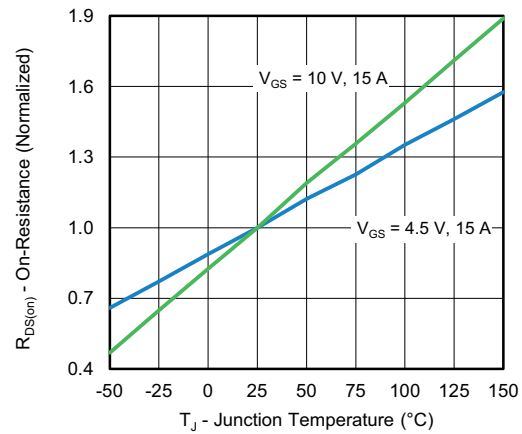
On-Resistance vs. Drain Current



Capacitance



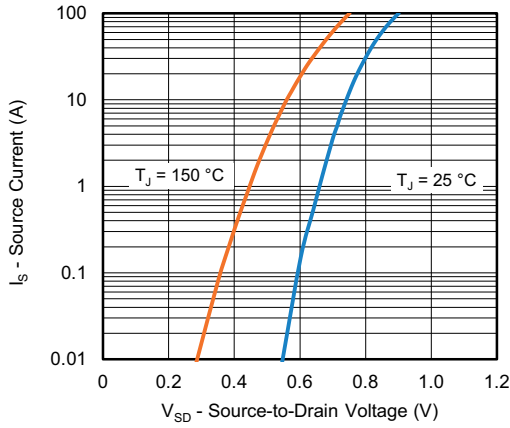
Gate Charge



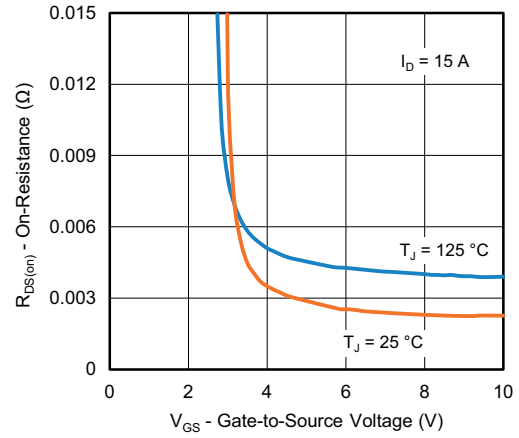
On-Resistance vs. Junction Temperature



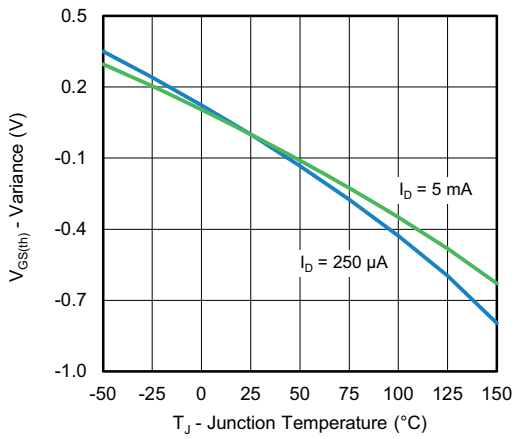
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



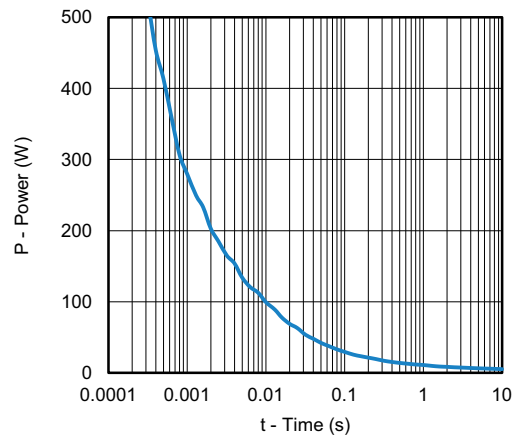
Source-Drain Diode Forward Voltage



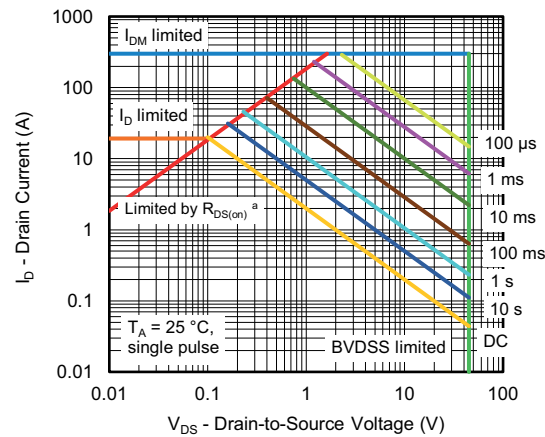
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



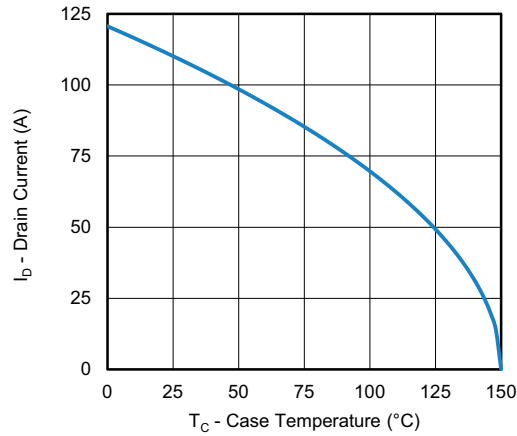
Single Pulse Power, Junction-to-Ambient



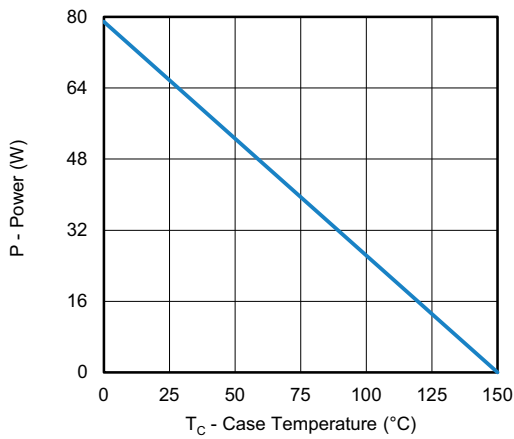
Safe Operating Area



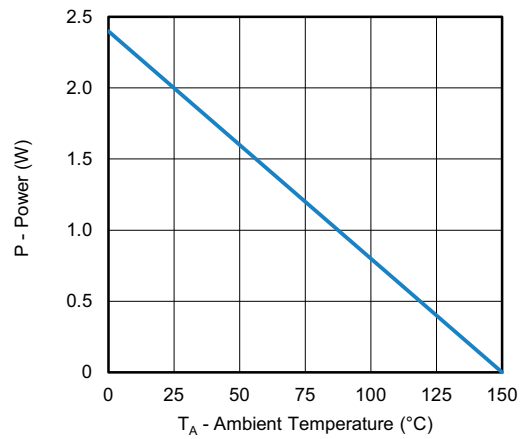
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



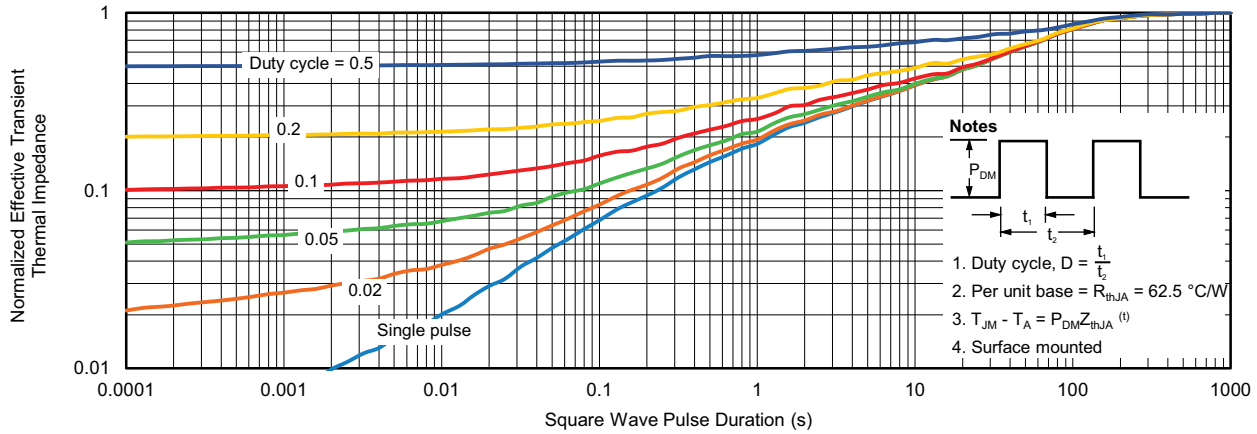
Power, Junction-to-Ambient

Note

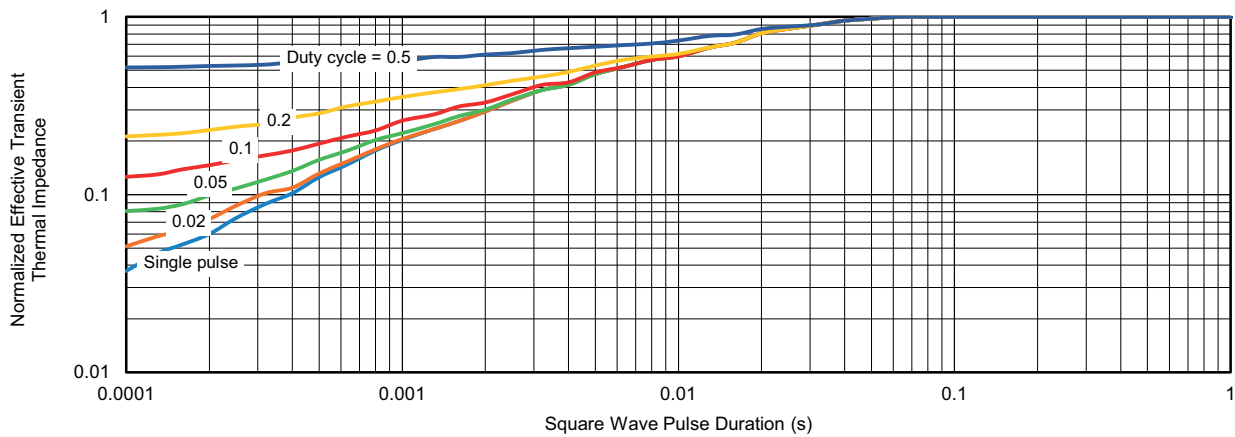
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77134.

Case Outline for PowerPAK® 1212-SWLH and PowerPAK® 1212-8SH



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		
ECN: S20-0930-Rev. C, 07-Dec-2020						
DWG: 6062						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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