

## VMMBZ16C1HD1 to VMMBZ33C1HD1

Vishay Semiconductors

AUTOMOTIVE GRADE

RoHS

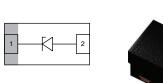
COMPLIANT

HALOGEN FREE

GREEN

(5-2008)

# Single-Line Unidirectional ESD-Protection Diode in DFN1006-2A





G

**MARKING** (example only)



Bar = pin 1 marking X = date code YY = type code (see table below)

### **LINKS TO ADDITIONAL RESOURCES**



VMMBZ16C1HD1





#### **FEATURES**

- Compact DFN1006-2A package
- Low package height < 0.5 mm
- 1-line unidirectional ESD-protection
- AEC-Q101 qualified available
- Working range 14 V; 28 V
- ESD immunity acc. IEC 61000-4-2 ±15 kV to ±30 kV contact discharge ±15 kV to ±30 kV air discharge
- Lead plating: Sn (e3)

-08

- Soldering can be checked by standard vision inspection
- AOI = Automated Optical Inspection
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912">www.vishay.com/doc?99912</a>

### **Soldering Recommendations for DFN Packages:**

please see Application Note: <a href="https://www.vishay.com/doc?86198">www.vishay.com/doc?86198</a>

VMMBZ16C1HD1HG3-08

ORDERING INFORMATION						
PART NUMBER (EXAMPLE)		ENVIRONMENTAL AND QUALITY CODE				
	AEC-Q101 QUALIFIED	RoHS COMPLIANT + LEAD (Pb)-FREE TERMINATIONS	TIN PLATED	10K PER 7" REEL (8 mm TAPE)	ORDERING CODE (EXAMPLE)	
		GREEN		MOQ = 10K/BOX		
VMMBZ16C1HD1	-	G	3	-08	VMMBZ16C1HD1-G3-08	

PACKAGE DATA									
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS			
VMMBZ16C1HD1	DFN1006-2A	2X	0.83 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C			
VMMBZ33C1HD1	DFN1006-2A	2L	0.83 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C			



## VMMBZ16C1HD1 to VMMBZ33C1HD1

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ABSOLUTE MAXIMUM RATINGS VMMBZ16C1HD1 (T <sub>amb</sub> = 25 °C, unless otherwise specified)						
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT		
Peak pulse current	Acc. IEC 61000-4-5, 8/20 μs/single shot	I <sub>PPM</sub>	4	Α		
Peak pulse power	Acc. IEC 61000-4-5, 8/20 μs/single shot <sup>(1)</sup>	P <sub>PP</sub>	108	W		
Peak pulse current	tp = 10/1000 μs <sup>(1)</sup>	I <sub>PPM</sub>	0.7	Α		
Peak pulse power	tp = 10/1000 μs <sup>(1)</sup>	P <sub>PP</sub>	16	W		
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses (1)		30	kV		
	Air discharge acc. IEC 61000-4-2; 10 pulses (1)	$V_{ESD}$	30	kV		
Operating temperature	Junction temperature	TJ	-55 to +150	°C		
Storage temperature		T <sub>stg</sub>	-55 to +150	°C		

#### Note

<sup>(1)</sup> Guaranteed by design; tested during device characterization

ABSOLUTE MAXIMUM RATINGS VMMBZ33C1HD1 (T <sub>amb</sub> = 25 °C, unless otherwise specified)						
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT		
Peak pulse current	Acc. IEC 61000-4-5, 8/20 µs/single shot	I <sub>PPM</sub>	1.7	Α		
Peak pulse power	Acc. IEC 61000-4-5, 8/20 μs/single shot <sup>(1)</sup>	P <sub>PP</sub>	100	W		
Peak pulse current	tp = 10/1000 μs <sup>(1)</sup>	I <sub>PPM</sub>	0.3	Α		
Peak pulse power	tp = 10/1000 μs <sup>(1)</sup>	$P_{PP}$	15	W		
ECD income to	Contact discharge acc. IEC 61000-4-2; 10 pulses (1)	M	15	kV		
ESD immunity	Air discharge acc. IEC 61000-4-2; 10 pulses (1)	$V_{ESD}$	15	kV		
Operating temperature	Junction temperature	TJ	-55 to +150	°C		
Storage temperature		T <sub>stg</sub>	-55 to +150	°C		

#### Note

 $<sup>^{(1)}</sup>$  Guaranteed by design; tested during device characterization

<b>ELECTRICAL CHARACTERISTICS</b> VMMBZ16C1HD1 (T <sub>amb</sub> = 25 °C, unless otherwise specified)							
PARAMETER	TEST CONDITIONS / REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Protection paths	Number of lines which can be protected	N <sub>channel</sub>	-	-	1	lines	
Reverse stand off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	14	V	
Reverse voltage	At I <sub>R</sub> = 10 nA	$V_R$	14	-	-	V	
Reverse current	At V <sub>R</sub> = 14 V	I <sub>R</sub>	-	< 1	10	nA	
	At V <sub>R</sub> = 14 V; T <sub>J</sub> = 150 °C <sup>(1)</sup>		-	0.06	10	μΑ	
Reverse breakdown voltage	At I <sub>R</sub> = 1 mA	V <sub>BR</sub>	15.2	16	16.8	V	
	At $I_R = 1$ mA; $T_J = -40$ °C to $+150$ °C $^{(1)}$		14.3	-	19.0	V	
Reverse clamping voltage	At $I_{PP} = I_{PPM} = 4 \text{ A}$ , $t_p = 8/20 \mu\text{s}$	V <sub>C</sub>	19	23	27	V	
	$t_p = 100 \text{ ns (TLP)}; I_{TLP} = 16 \text{ A}^{(1)}$	V <sub>C_TLP</sub>	-	24	-	V	
Dynamic resistance	$t_p = 100 \text{ ns (TLP)}^{(1)}$	r <sub>dyn</sub>	-	0.48	-	Ω	
Capacitance	At V <sub>R</sub> = 0 V; f = 1 MHz	C <sub>D</sub>	24.6	29	33.4	pF	

### Note

<sup>(1)</sup> Guaranteed by design; tested during device characterization



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<b>ELECTRICAL CHARACTERISTICS</b> VMMBZ33C1HD1 (T <sub>amb</sub> = 25 °C, unless otherwise specified)							
PARAMETER	TEST CONDITIONS / REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Protection paths	Number of lines which can be protected	N <sub>channel</sub>	-	-	1	lines	
Reverse stand off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	28	V	
Reverse voltage	At I <sub>R</sub> = 10 nA	$V_R$	28	-	-	V	
D	At V <sub>R</sub> = 28 V	I <sub>R</sub>	-	< 1	10	nA	
Reverse current	At V <sub>R</sub> = 28 V; TJ = 150 °C <sup>(1)</sup>		=	0.1	10	μΑ	
Reverse breakdown voltage	At I <sub>R</sub> = 1 mA	$V_{BR}$	31.3	33	34.7	V	
	At $I_R = 1$ mA; $T_J = -40$ °C to +150 °C (1)		29	-	39	V	
Reverse clamping voltage	At $I_{PP} = I_{PPM} = 1.7 \text{ A}, t_p = 8/20 \mu s$	V <sub>C</sub>	40	49	59	V	
	$t_p = 100 \text{ ns (TLP)}; I_{TLP} = 16 \text{ A}^{(1)}$	$V_{C\_TLP}$	-	85	-	V	
Dynamic resistance	t <sub>p</sub> = 100 ns (TLP) <sup>(1)</sup>	r <sub>dyn</sub>	-	0.34	-	Ω	
Capacitance	At V <sub>R</sub> = 0 V; f = 1 MHz	C <sub>D</sub>	13.6	16.1	18.6	pF	

#### Note

100

80

60

40

20

0

## **TYPICAL CHARACTERISTICS** ( $T_{amb} = 25$ °C, unless otherwise specified)

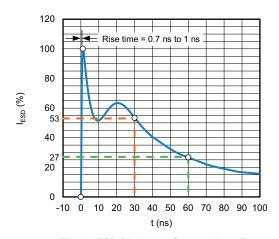


Fig. 1 - ESD Discharge Current Wave Form According to IEC 61000-4-2 (330  $\Omega$  / 150 pF)

us to 100 %

20 us to 50 %

10



t (μs)
Fig. 2 - 8/20 μs Peak Pulse Current Wave Form
According to IEC 61000-4-5

20

30

40

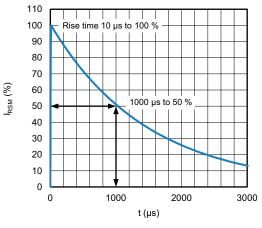


Fig. 3 - 10/1000 µs Peak Pulse Current Wave Form

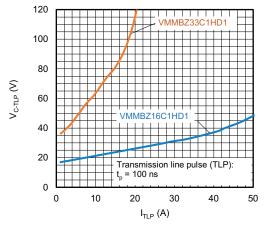


Fig. 4 - Typical Clamping Voltage vs. Peak Pulse Current

<sup>(1)</sup> Guaranteed by design; tested during device characterization

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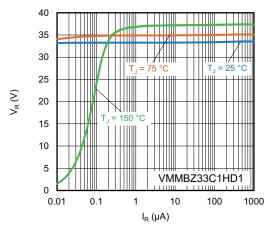


Fig. 5 - Typical Reverse Voltage vs. Reverse Current

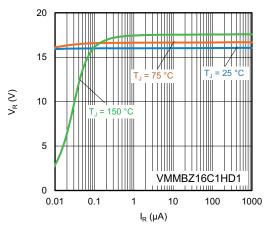


Fig. 6 - Typical Reverse Voltage vs. Reverse Current

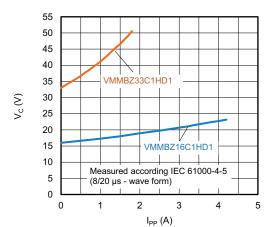


Fig. 7 - Typical Peak Clamping Voltage vs. Peak Pulse Current

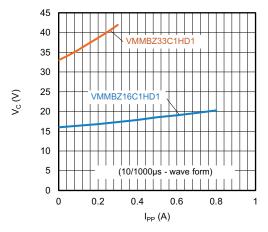


Fig. 8 - Typical Peak Clamping Voltage vs. Peak Pulse Current

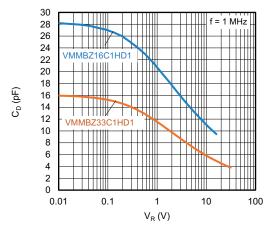


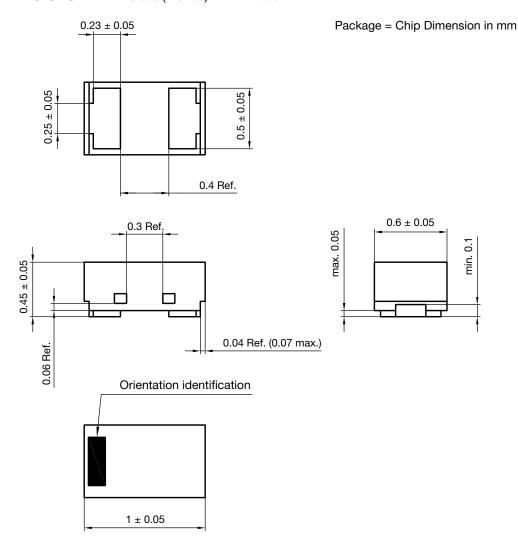
Fig. 9 - Typical Capacitance vs. Reverse Voltage

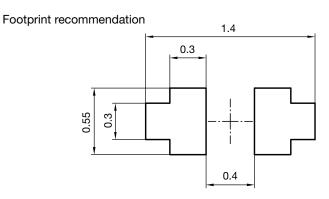




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### PACKAGE DIMENSIONS in millimeters (Inches): DFN1006-2A



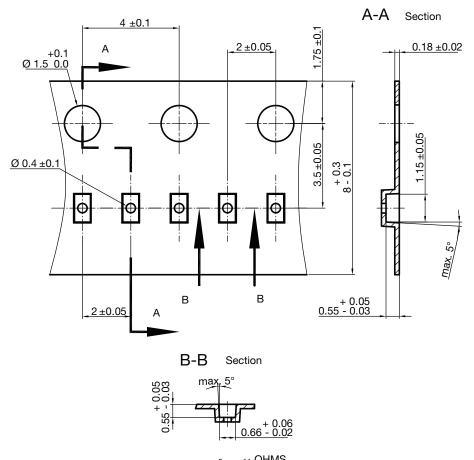


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### **CARRIER TAPE DFN1006-2A**



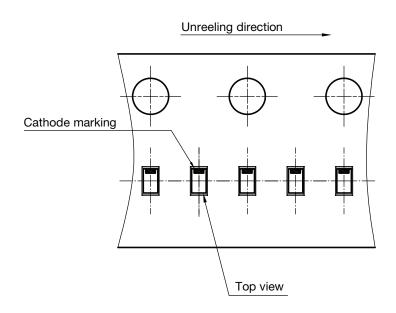
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S8-V-3906.04-064 (4)

created 28.10.2019

surface resistance:  $10^5$  -  $10^{11} \frac{OHMS}{SQ}$ Cummulative tolerances of 10 sprocket holes is  $\pm 0.2$  mm

### **ORIENTATION IN CARRIER TAPE DFN1006-2A**



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