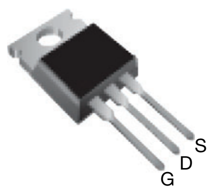
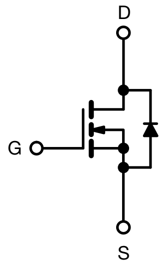
# Power MOSFET

TO-220AB




N-Channel MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 800 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 6.5 |
| $Q_g$ max. (nC) | 38 | |
| $Q_{gs}$ (nC) | 5.0 | |
| $Q_{gd}$ (nC) | 21 | |
| Configuration | Single | |

## FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Available

**RoHS***

Available

**Note**

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

| ORDERING INFORMATION | |
|---|---|
| Package | TO-220AB |
| Lead (Pb)-free | IRFBE20PbF |
| Lead (Pb)-free and halogen-free | IRFBE20PbF-BE3 |

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-source voltage | | | $V_{DS}$ | 800 | V |
| Gate-source voltage | | | $V_{GS}$ | ± 20 | |
| Continuous drain current | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 1.8 | A |
| | | $T_C$ = 100 °C | | 1.2 | |
| Pulsed drain current [a] | | | $I_{DM}$ | 7.2 | |
| Linear derating factor | | | | 0.43 | W/°C |
| Single pulse avalanche energy [b] | | | $E_{AS}$ | 180 | mJ |
| Repetitive avalanche current [a] | | | $I_{AR}$ | 1.8 | A |
| Repetitive avalanche energy [a] | | | $E_{AR}$ | 5.4 | mJ |
| Maximum power dissipation | $T_C$ = 25 °C | | $P_D$ | 54 | W |
| Peak diode recovery dV/dt [c] | | | dV/dt | 2.0 | V/ns |
| Operating junction and storage temperature range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering recommendations (peak temperature) [d] | For 10 s | | | 300 | |
| Mounting torque | 6-32 or M3 screw | | | 10 | lbf · in |
| | | | | 1.1 | N · m |

**Notes**

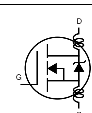
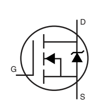
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 104 mH, $R_g$ = 25 Ω, $I_{AS}$ = 1.8 A (see fig. 12)

c. $I_{SD} \leq 1.8$ A, dI/dt ≤ 80 A/μs, $V_{DD} \leq 600$, $T_J \leq 150$ °C

d. 1.6 mm from case

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum junction-to-ambient | $R_{thJA}$ | - | 62 | °C/W |
| Case-to-sink, flat, greased surface | $R_{thCS}$ | 0.50 | - | |
| Maximum junction-to-case (drain) | $R_{thJC}$ | - | 2.3 | |

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-source breakdown voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 800 | - | - | V |
| $V_{DS}$ temperature coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 0.98 | - | V/°C |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 2.0 | - | 4.0 | V |
| Gate-source leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 100 | nA |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ = 800 V, $V_{GS}$ = 0 V | - | - | 100 | μA |
| | | $V_{DS}$ = 640 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 500 | |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V; $I_D$ = 1.1 A [b] | - | - | 6.5 | Ω |
| Forward transconductance | $g_{fs}$ | $V_{DS}$ = 100 V, $I_D$ = 1.1 A [b] | 0.80 | - | - | S |
| **Dynamic** | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | - | 530 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 150 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 90 | - | |
| Total gate charge | $Q_g$ | $V_{GS}$ = 10 V; $I_D$ = 1.8 A, $V_{DS}$ = 400 V, see fig. 6 and 13 [b] | - | - | 38 | nC |
| Gate-source charge | $Q_{gs}$ | | - | - | 5.0 | |
| Gate-drain charge | $Q_{gd}$ | | - | - | 21 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$ = 400 V, $I_D$ = 1.8 A, $R_g$ = 18 Ω, $R_D$ = 230 Ω, see fig. 10 [b] | - | 8.2 | - | ns |
| Rise time | $t_r$ | | - | 17 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 58 | - | |
| Fall time | $t_f$ | | - | 27 | - | |
| Gate input resistance | $R_g$ | f = 1 MHz, open drain | 0.6 | - | 4.2 | Ω |
| Internal drain inductance | $L_D$ | Between lead, 6 mm (0.25") from package and center of die contact  | - | 4.5 | - | nH |
| Internal source inductance | $L_S$ | | - | 7.5 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous source-drain diode current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 1.8 | A |
| Pulsed diode forward current [a] | $I_{SM}$ | | - | - | 7.2 | |
| Body diode voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 1.8 A, $V_{GS}$ = 0 V [b] | - | - | 1.4 | V |
| Body diode reverse recovery time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = 1.8 A, dI/dt = 100 A/μs [b] | - | 380 | 570 | ns |
| Body diode reverse recovery charge | $Q_{rr}$ | | - | 0.94 | 1.4 | μC |
| Forward turn-on time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

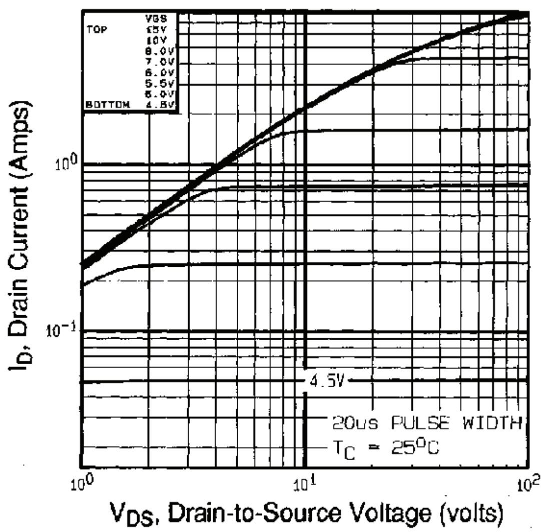



**Fig. 1 - Typical Output Characteristics, $T_C$ = 25 °C**

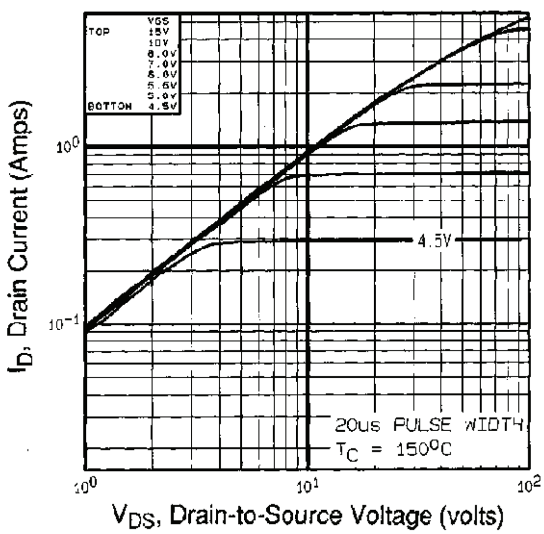



**Fig. 2 - Typical Output Characteristics, $T_C$ = 150 °C**

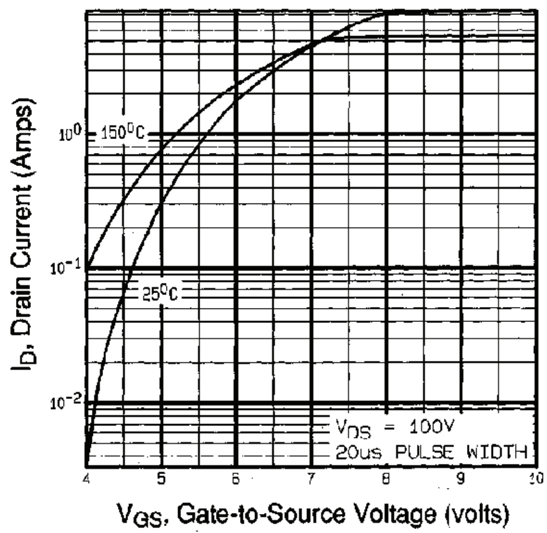



**Fig. 3 - Typical Transfer Characteristics**

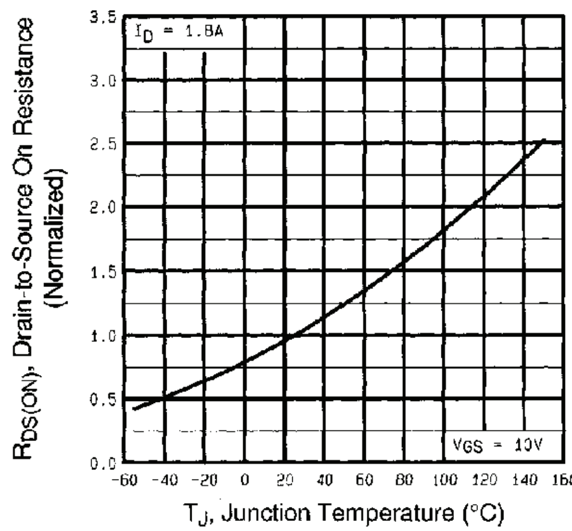



**Fig. 4 - Normalized On-Resistance vs. Temperature**

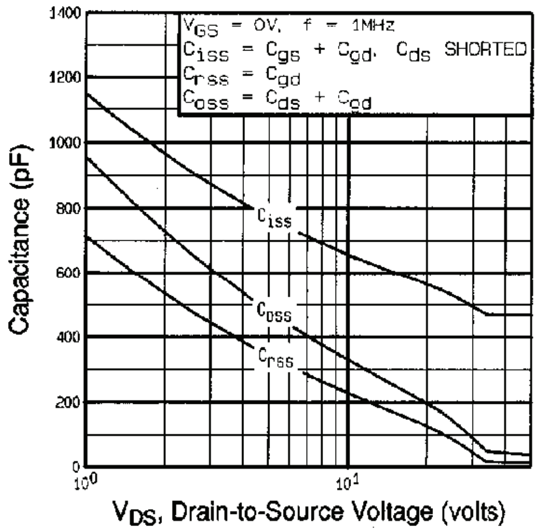



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

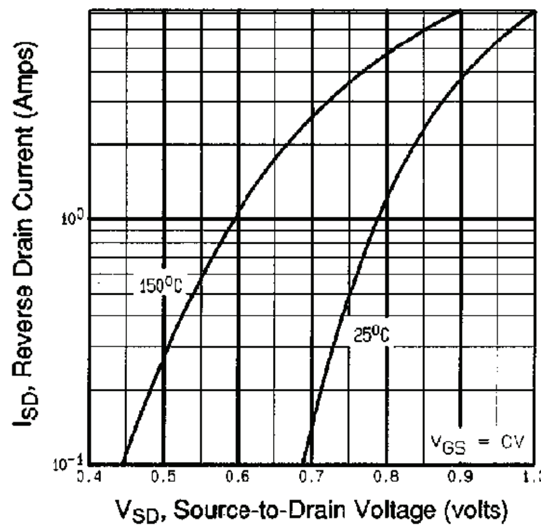



Fig. 7 - Typical Source-Drain Diode Forward Voltage

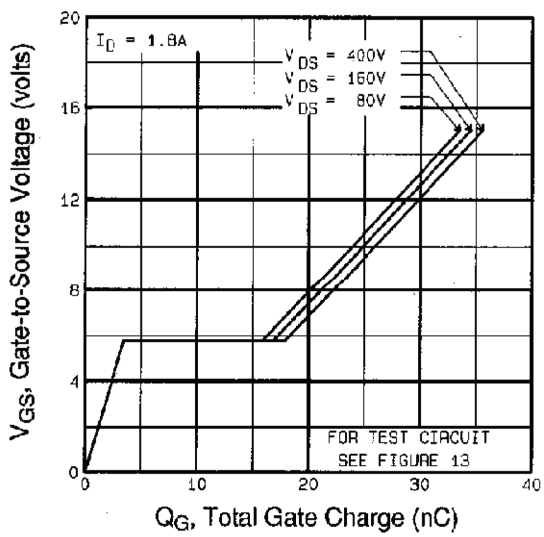



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

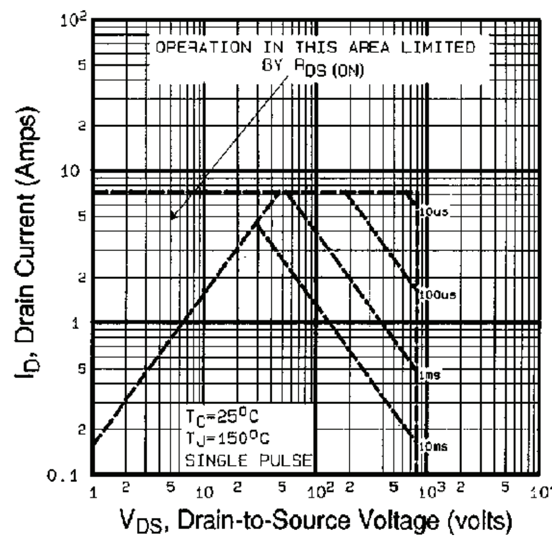



Fig. 8 - Maximum Safe Operating Area

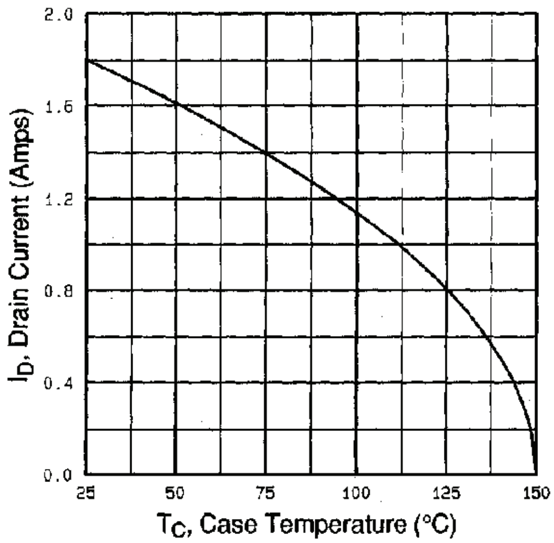



Fig. 9 - Maximum Drain Current vs. Case Temperature

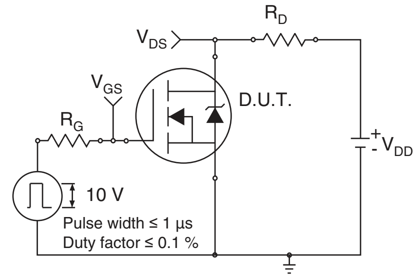



Fig. 10a - Switching Time Test Circuit

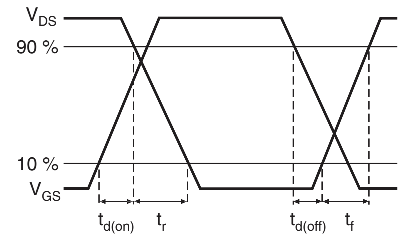



Fig. 10b - Switching Time Waveforms

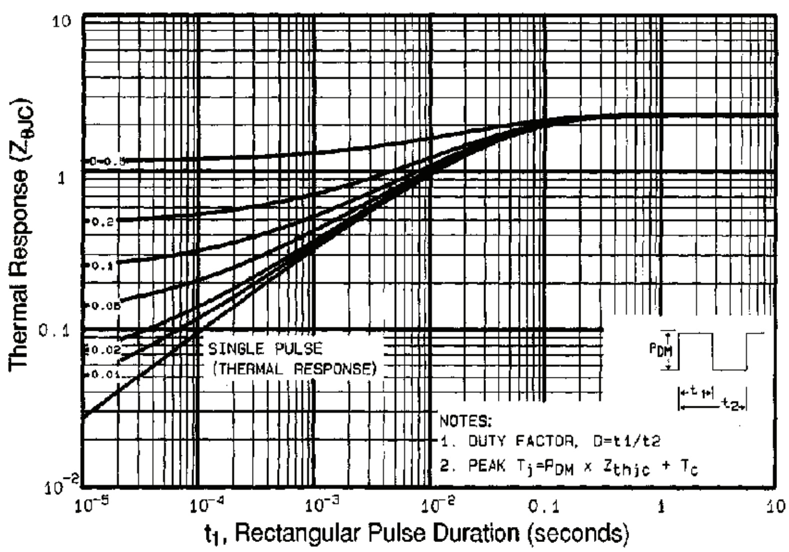



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

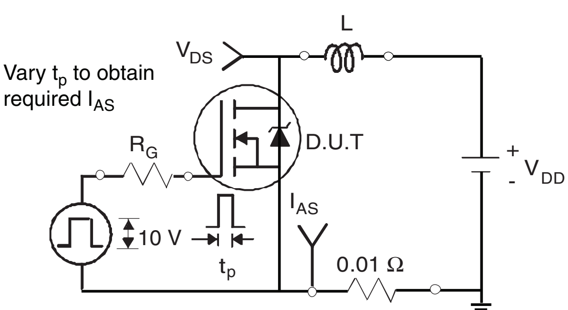



Fig. 12a - Unclamped Inductive Test Circuit

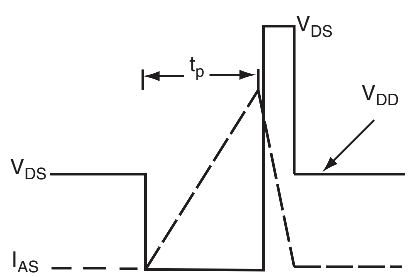



Fig. 12b - Unclamped Inductive Waveforms

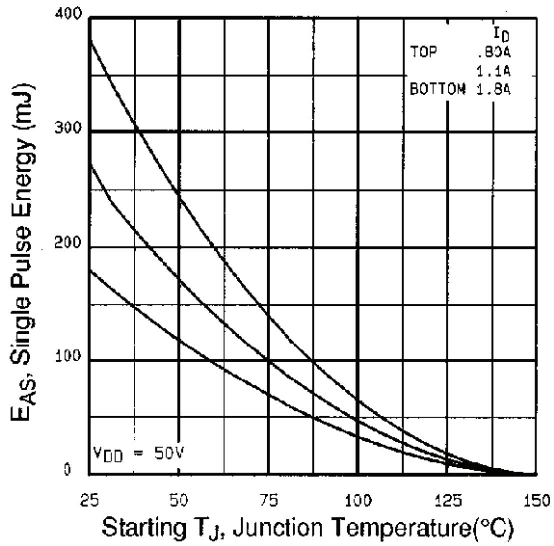



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

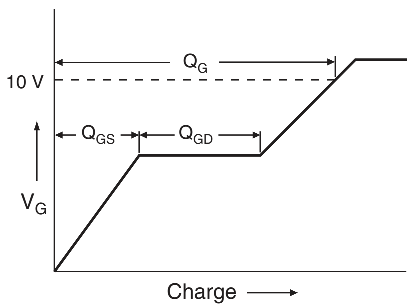



**Fig. 13a - Basic Gate Charge Waveform**

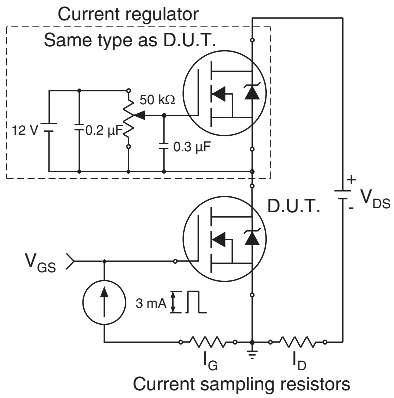
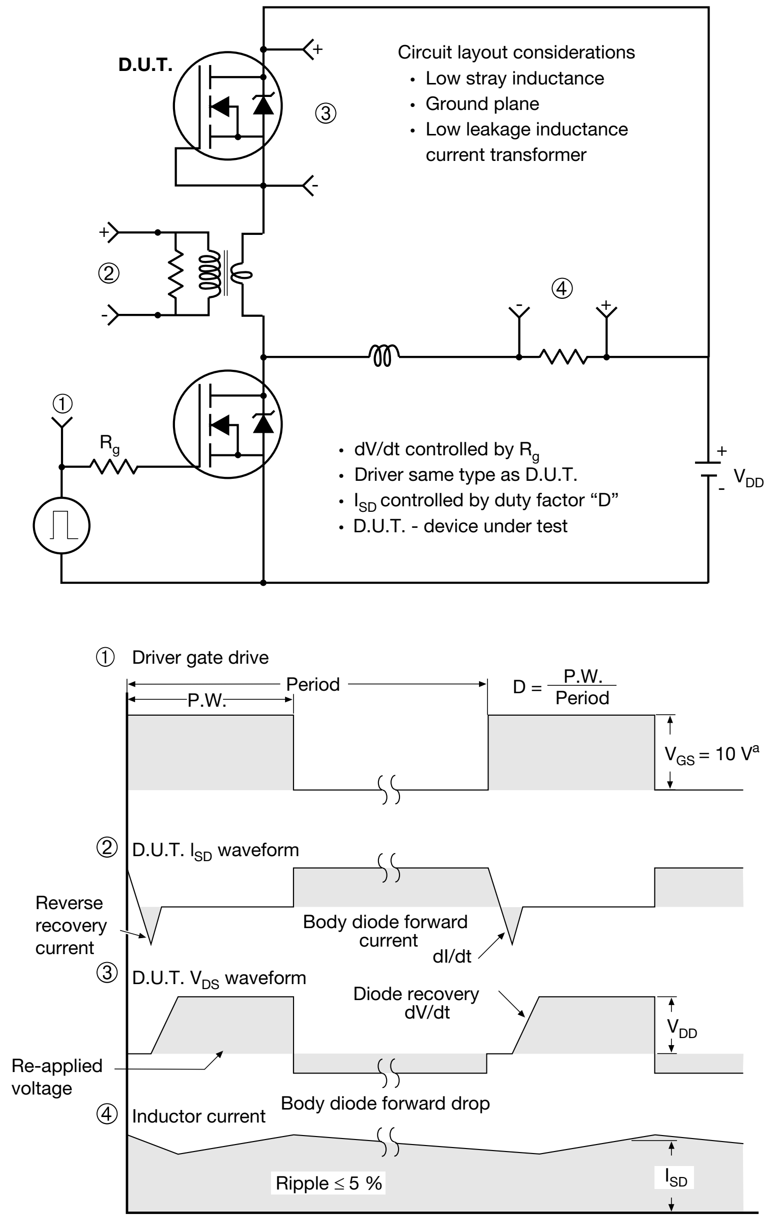



**Fig. 13b - Gate Charge Test Circuit**


For technical questions, contact: hvm@vishay.com

## Peak Diode Recovery dV/dt Test Circuit




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

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