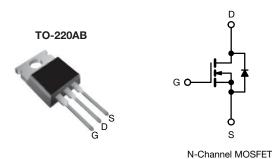


## **Power MOSFET**



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	200			
$R_{DS(on)}(\Omega)$	$V_{GS} = 10 \text{ V}$	0.40		
Q <sub>g</sub> max. (nC)	43			
Q <sub>gs</sub> (nC)	7.0			
Q <sub>gd</sub> (nC)	23			
Configuration	Single			

#### **FEATURES**

- Dynamic dV/dt rating
- Repetitive avalanche rated
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>



#### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

#### **DESCRIPTION**

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION			
Package	TO-220AB		
Lead (Pb)-free	IRF630PbF		
Lead (Pb)-free and halogen-free	IRF630PbF-BE3		

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub>	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			$V_{DS}$	200	V	
Gate-source voltage			$V_{GS}$	± 20		
Continuous drain current	V -+ 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$		9.0		
	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	5.7	Α	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	36		
Linear derating factor				0.59	W/°C	
Single pulse avalanche energy b			E <sub>AS</sub>	250	mJ	
Repetitive avalanche current a			I <sub>AR</sub>	9.0	А	
Repetitive avalanche energy <sup>a</sup>			E <sub>AR</sub>	7.4	mJ	
Maximum power dissipation	T <sub>C</sub> =	25 °C	$P_{D}$	74	W	
Peak diode recovery dV/dt <sup>c</sup>			dV/dt	5.0	V/ns	
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s			300		
Mounting torque	6.00.0*1	0.00 140		10	lbf ⋅ in	
	6-32 or M3 screw			1.1	N⋅m	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b.  $V_{DD}$  = 50 V, starting  $T_J$  = 25 °C, L = 4.6 mH,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 9.0 A (see fig. 12)
- c.  $I_{SD} \le 9.0$  A,  $dI/dt \le 120$  A/ $\mu$ s,  $V_{DD} \le V_{DS}$ ,  $T_J \le 150$  °C
- d. 1.6 mm from case



# Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62		
Case-to-sink, flat, greased surface	R <sub>thCS</sub>	0.50	-	°C/W	
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	1.7		

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	$V_{DS}$	V <sub>GS</sub> :	200	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.24	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		-	4.0	V
Gate-source leakage	I <sub>GSS</sub>		V <sub>GS</sub> = ± 20 V		-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	25 250	μA
Drain-source on-state resistance	R <sub>DS(on)</sub>		I <sub>D</sub> = 5.4 A <sup>b</sup>	-	-	0.40	Ω
Forward transconductance	9 <sub>fs</sub>		= 50 V, I <sub>D</sub> = 5.4 A	3.8	_	-	S
Dynamic	0.0	1 50			l		
Input capacitance	C <sub>iss</sub>		-	800	-	pF	
Output capacitance	C <sub>oss</sub>	1	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$		240		-
Reverse transfer capacitance	C <sub>rss</sub>	f = 1.0 MHz, see fig. 5		-	76		-
Total gate charge	Qg		$V_{GS} = 10 \text{ V}$ $I_D = 5.9 \text{ A}, V_{DS} = 160 \text{ V},$ see fig. 6 and 13 b	-	-	43	nC
Gate-source charge	$Q_{gs}$	V <sub>GS</sub> = 10 V		-	-	7.0	
Gate-drain charge	Q <sub>gd</sub>	1		-	-	23	
Turn-on delay time	t <sub>d(on)</sub>		•	-	9.4	-	
Rise time	t <sub>r</sub>	$V_{DD}$ = 100 V, $I_{D}$ = 5.9 A, $R_{g}$ = 12 $\Omega$ , $R_{D}$ = 16 $\Omega$ , see fig. 10 <sup>b</sup>		-	28	-	ns
Turn-off delay time	t <sub>d(off)</sub>			-	39	-	
Fall time	t <sub>f</sub>			-	20	-	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.6	-	3.3	Ω
Internal drain inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristic	cs			•		•	
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	9.0	^
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	36	- A
Body diode voltage	$V_{SD}$	$T_J = 25  ^{\circ}\text{C}, \ I_S = 9.0  \text{A}, \ V_{GS} = 0  \text{V}^{ \text{b}}$		-	-	2.0	V
Body diode reverse recovery time	t <sub>rr</sub>	$T_J = 25 ^{\circ}\text{C}$ , $I_F = 5.9 \text{A}$ , $dI/dt = 100 \text{A/}\mu\text{s}$		-	170	340	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	1.1	2.2	nC
Forward turn-on time	t <sub>on</sub>	Intrinsic tu	n-on is dominated by L <sub>S</sub> and L <sub>D</sub> )			L <sub>D</sub> )	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq$  300 µs; duty cycle  $\leq$  2 %



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

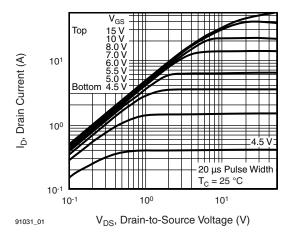


Fig. 1 - Typical Output Characteristics, T<sub>C</sub> = 25 °C

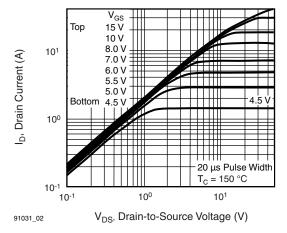


Fig. 2 - Typical Output Characteristics,  $T_C = 150$  °C

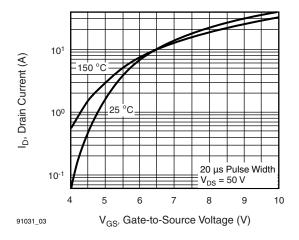


Fig. 3 - Typical Transfer Characteristics

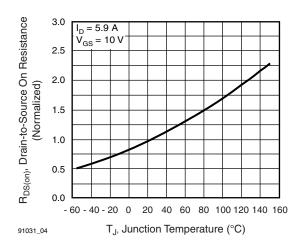


Fig. 4 - Normalized On-Resistance vs. Temperature

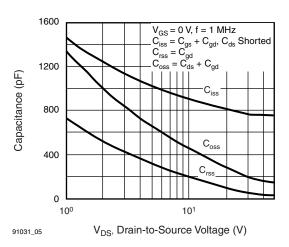


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

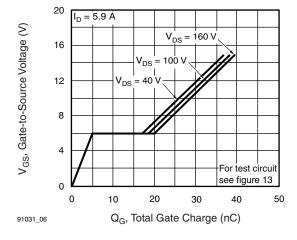


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



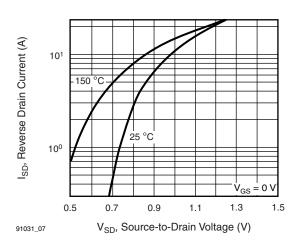


Fig. 7 - Typical Source-Drain Diode Forward Voltage

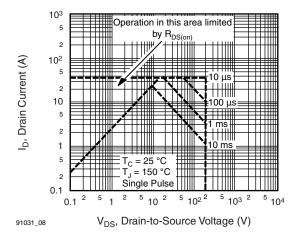


Fig. 8 - Maximum Safe Operating Area

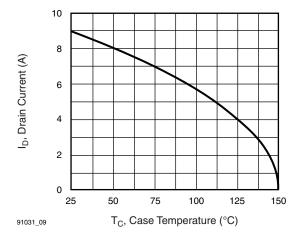


Fig. 9 - Maximum Drain Current vs. Case Temperature

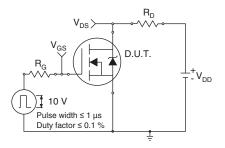


Fig. 10a - Switching Time Test Circuit

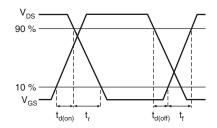


Fig. 10b - Switching Time Waveforms



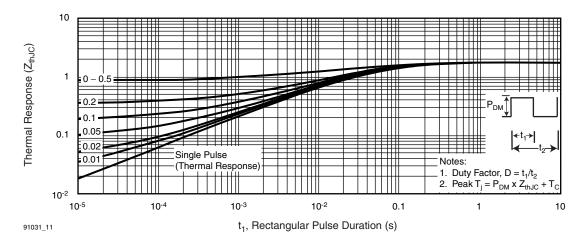


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

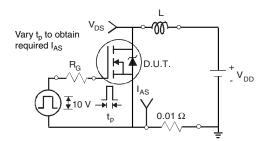


Fig. 12a - Unclamped Inductive Test Circuit

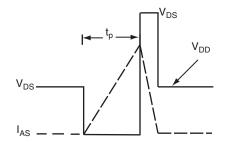


Fig. 12b - Unclamped Inductive Waveforms

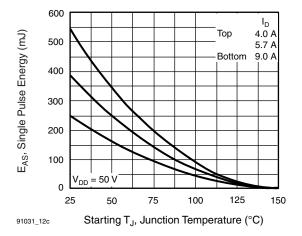


Fig. 12c - Maximum Avalanche Energy vs. Drain Current



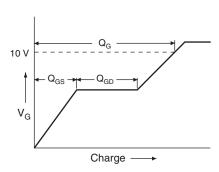


Fig. 13a - Basic Gate Charge Waveform

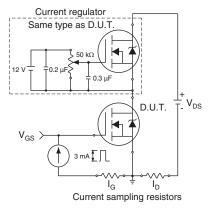
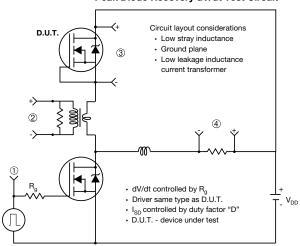


Fig. 13b - Gate Charge Test Circuit

#### Peak Diode Recovery dV/dt Test Circuit



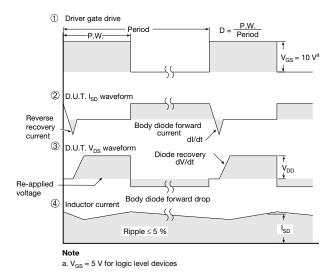


Fig. 14 - For N-Channel

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