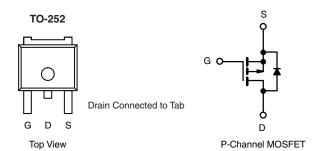


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Vishay Siliconix

# Automotive P-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	- 60			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.055			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.100			
I <sub>D</sub> (A)	- 20			
Configuration	Single			



### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- $\bullet$  100 %  $R_{\rm g}$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC
- AEC-Q101 Qualifiedd



ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD19P06-60L-GE3

ABSOLUTE MAXIMUM RATING	<b>5</b> (10 = 25 °C, unles	s otherwise noted	וג	T
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	- 60	V
Gate-Source Voltage		$V_{GS}$	± 20	V
Continuous Drain Current	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	- 20	
	T <sub>C</sub> = 125 °C		- 11	
Continuous Source Current (Diode Conduction) <sup>a</sup>		Is	- 25	Α
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	- 80	
Single Pulse Avalanche Current	J 0.1 ml J	I <sub>AS</sub>	- 24	
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	28	mJ
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	= 25 °C	46	10/
	T <sub>C</sub> = 125 °C	$P_{D}$	15	W
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient P	CB Mount <sup>c</sup>	$R_{thJA}$	50	°C/W	
Junction-to-Case (Drain)		R <sub>thJC</sub>	3.2	1 C/VV	

### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		- 60	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$		-	- 2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 60 V	-	-	- 1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = - 60 V, T <sub>J</sub> = 125 °C	-	-	- 50	μΑ
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = - 60 V, T <sub>J</sub> = 175 °C	-	-	- 150	1
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = - 10 V	V <sub>DS</sub> ≤ - 5 V	- 20	-	-	Α
		V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 19 A	-	0.046	0.055	Ω
Drain Cauras On State Besistance	В	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 19 A, T <sub>J</sub> = 125 °C	-	-	0.095	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 19 A, T <sub>J</sub> = 175 °C	-	-	0.125	
		V <sub>GS</sub> = - 4.5 V	I <sub>D</sub> = - 10 A	-	0.075	0.100	
Forward Transconductancea	9 <sub>fs</sub>	V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 17 A		-	20	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			-	1192	1490	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	= 0 V V <sub>DS</sub> = - 25 V, f = 1 MHz		160	200	pF
Reverse Transfer Capacitance	C <sub>rss</sub>			-	96	120	
Total Gate Charge <sup>c</sup>	Qg			-	27	41	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	V <sub>GS</sub> = - 10 V	$V_{DS} = -30 \text{ V}, I_{D} = -19 \text{ A}$	-	3.9	-	nC
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	5.9	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		2.3	4.7	7.1	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	7	11	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = - 30 V, $R_L$ = 1.6 $\Omega$ $I_D \cong$ - 19 A, $V_{GEN}$ = - 10 V, $R_g$ = 1 $\Omega$		-	9	14	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	25	38	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	12	18	
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>						
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			=	-	- 80	Α
Forward Voltage	$V_{SD}$	I <sub>F</sub> = - 10 A, V <sub>GS</sub> = 0 V		-	- 0.85	- 1.5	V

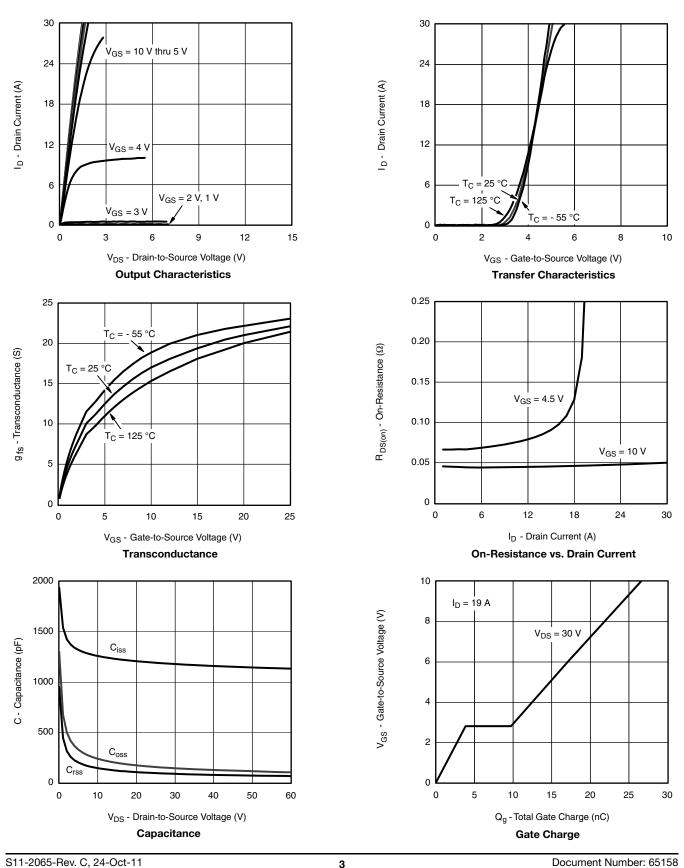
### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

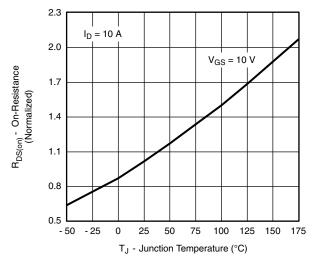


## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

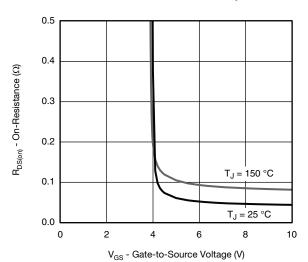




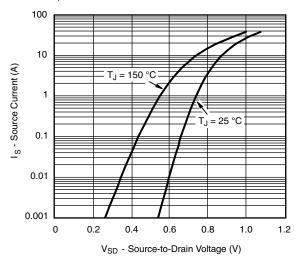
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



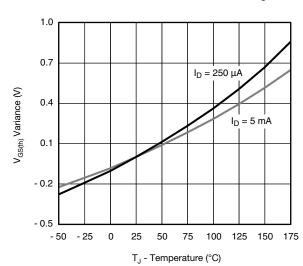
### On-Resistance vs. Junction Temperature



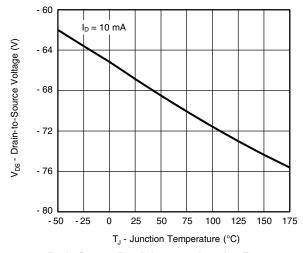
On-Resistance vs. Gate-to-Source Voltage



**Source Drain Diode Forward Voltage** 



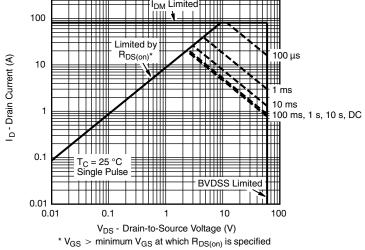
**Threshold Voltage** 



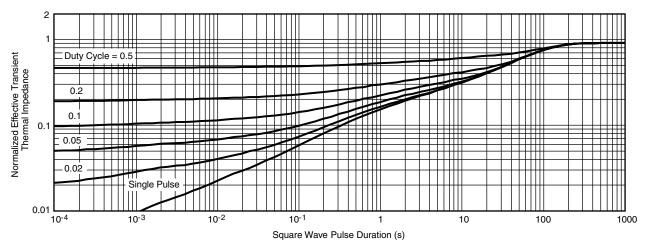
Drain Source Breakdown vs. Junction Temperature



## **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



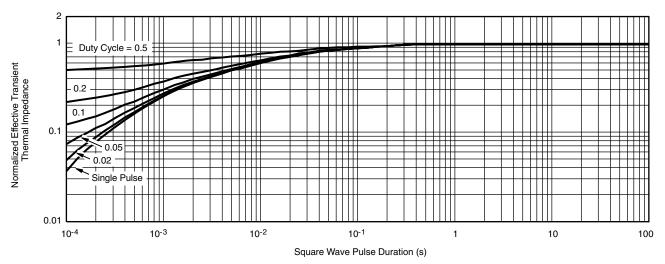
### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

### Note

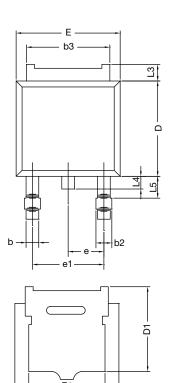
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

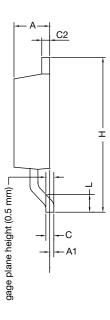
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?65158">www.vishay.com/ppg?65158</a>.



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## **TO-252AA Case Outline**





	MILLIN	METERS	INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
Е	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28	BSC	0.090 BSC		
e1	4.56 BSC		0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T13-0592-Rev. A, 02-Sep-13					

### DWG: 6019

Note

• Dimension L3 is for reference only.



## **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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