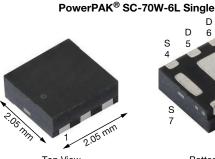
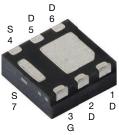
## SQA444CEJW

www.vishay.com

**Vishay Siliconix** 

# Automotive N-Channel 60 V (D-S) 175 °C MOSFET





Bottom View

Top View Marking Code: Q9XXXX

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	60
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$	0.0390
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS}$ = 4.5 V	0.0526
I <sub>D</sub> (A)	9
Configuration	Single

#### **FEATURES**

- TrenchFET<sup>®</sup> power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 %  $R_{\alpha}$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



FREE

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ORDERING INFORMATION	
Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA444CEJW

ABSOLUTE MAXIMUM RATING	<b>S</b> (T <sub>C</sub> = 25 °C, unles	s otherwise noted	)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	60	V
Gate-source voltage		V <sub>GS</sub>	± 20	v
Continuous drain ourrent	T <sub>C</sub> = 25 °C ª	1-	9	
Continuous drain current	T <sub>C</sub> = 125 °C	ID	7.7	
Continuous source current (diode conduction) <sup>a</sup>		I <sub>S</sub>	9	А
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	28	
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	12.5	
Single pulse avalanche energy		E <sub>AS</sub>	7.81	mJ
Movimum power dissinction	T <sub>C</sub> = 25 °C	PD	13.6	W
Maximum power dissipation	T <sub>C</sub> = 125 °C	PD	4.5	vv
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperature) d, e			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>c</sup>	R <sub>thJA</sub>	90	°C/W
Junction-to-case (drain)		R <sub>thJC</sub>	11	0/10

#### Notes

a. Package limited

b. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$ 

c. When mounted on 1" square PCB (FR4 material)

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

S21-1152-Rev. B, 06-Dec-2021

1

d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin.

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SQA444CEJW

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<b>SPECIFICATIONS</b> ( $T_C = 25 \ ^{\circ}C$ , ur		1		[	r	1	
PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static		1		-	T	1	
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> =	= 0 V, I <sub>D</sub> = 250 μA	60	-	-	v
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	- V <sub>GS</sub> , I <sub>D</sub> = 250 μΑ	1.5	2.0	2.5	v
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V	-	-	1	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS}$ = 60 V, $T_J$ = 125 °C	-	-	50	μA
		$V_{GS} = 0 V$	$V_{DS} = 60 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	10	-	-	А
		$V_{GS} = 10 V$	I <sub>D</sub> = 4.5 A	-	0.0318	0.0390	
Drain aquraa an atata rasistanaa a	$\begin{tabular}{ c c c c c c } \hline V_{GS}(th) & V_{DS} = V_{GS}, I_D = 250 \ \mu A & 1.5 & 2.0 \\ \hline I_{GSS} & V_{DS} = 0 \ V, V_{GS} = \pm 20 \ V & - & - & - & - & - & - & - & - & - &$	0.0623					
Dynamic b   Input capacitance   Output capacitance   Reverse transfer capacitance	HDS(on)	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4.5 A, T <sub>J</sub> = 175 °C	-	-	0.0764	Ω
		$V_{GS} = 4.5 V$	I <sub>D</sub> = 3 A	-	0.0429	0.0526	
Forward transconductance b	<b>g</b> <sub>fs</sub>	V <sub>DS</sub> :	= 15 V, I <sub>D</sub> = 4.5 A	-	17	-	S
Dynamic <sup>b</sup>					•	•	
Input capacitance	C <sub>iss</sub>			-	378	530	
Output capacitance	Coss	$V_{GS} = 0 V$	V <sub>DS</sub> = 25 V, f = 1 MHz	-	215	300	pF
Reverse transfer capacitance	C <sub>rss</sub>			-	12	17	
Total gate charge <sup>c</sup>				-	6	9	
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 30 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	-	1.52	-	nC
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	0.55	-	
Gate resistance			f = 1 MHz	0.225	0.450	0.675	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	8	12	
Rise time <sup>c</sup>		Voo	= 30 V. Rι = 6 Ω	-	3	6	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	13	20	ns
Fall time <sup>c</sup>	t <sub>f</sub>			-	3	6	
Source-Drain Diode Ratings and Charact	eristics <sup>b</sup>						
Pulsed current <sup>a</sup>				-	-	28	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> =	4.5 A, V <sub>GS</sub> = 0 V	-	0.84	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>			-	16	32	ns
Body diode reverse recovery charge		1		-	8.4	17	nC
Reverse recovery fall time	ta	$I_F = 2$	A, ai/at = 100 A/µs	-	9	-	
Reverse recovery rise time	t <sub>b</sub>	1		-	7	-	ns
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-1.0	-	А

#### Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing

c. Independent of operating temperature

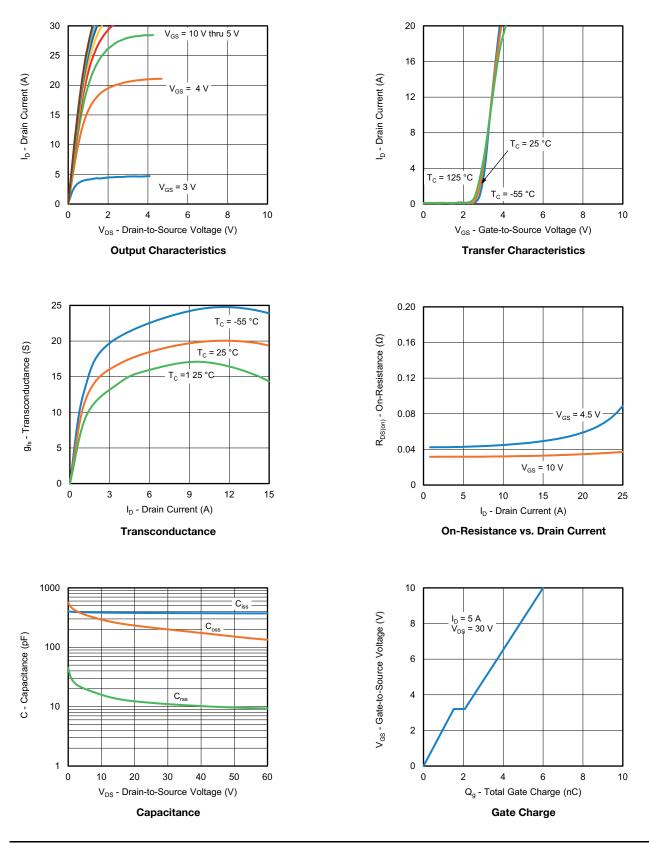
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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## **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



S21-1152-Rev. B, 06-Dec-2021

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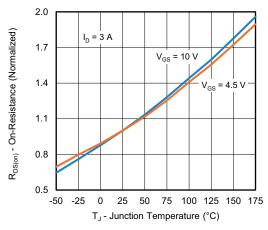
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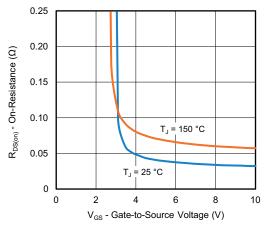


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## **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



**On-Resistance vs. Junction Temperature** 



T<sub>.</sub> = 150 °C

0.6

On-Resistance vs. Gate-to-Source Voltage

T<sub>J</sub> = 25 °C

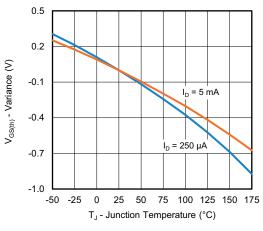
0.9

V<sub>SD</sub> - Source-to-Drain Voltage (V)

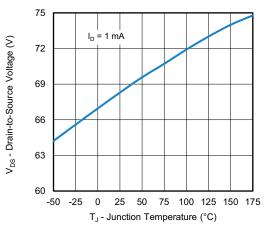
Source Drain Diode Forward Voltage

1.2

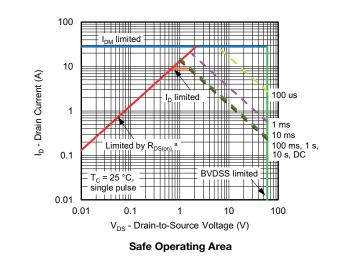
1.5



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



S21-1152-Rev. B, 06-Dec-2021

0.3

100

10

1

0.1

0.01

0

I<sub>s</sub> - Source Current (A)

4

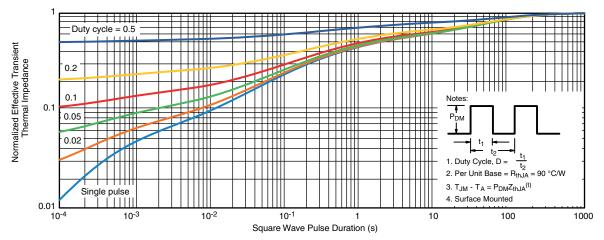
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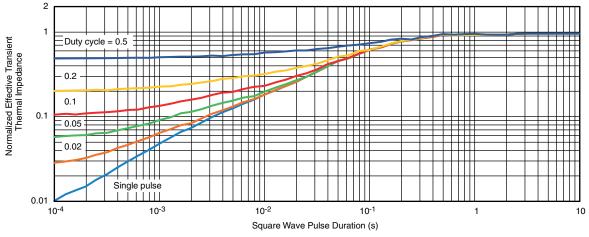


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### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?63136">www.vishay.com/ppg?63136</a>.

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D1

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K1

D2

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K6

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K5

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K4

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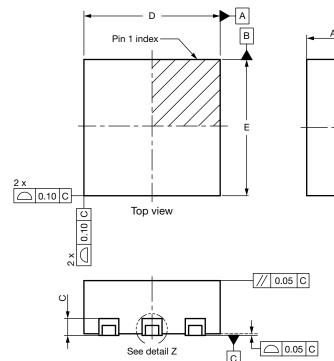
F2

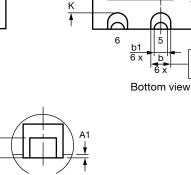
L 4

0.1 M C A B

0.05 🕅 C

# PowerPAK<sup>®</sup> SC70W-6L SIDEWETTABLE





Detail Z (2:1)

K

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E1

DIM		MILLIMETERS		INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	0.70	0.80	0.90	0.027	0.031	0.035	
A1	0.00	0.02	0.05	0.000	0.001	0.002	
A2	0.10	-	-	0.004	-	-	
b	0.25	0.30	0.35	0.010	0.012	0.014	
b1	0.15	0.20	0.23	0.006	0.008	0.009	
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	1.95	2.05	2.15	0.077	0.081	0.085	
D1	0.88	0.98	1.08	0.035	0.039	0.043	
D2	0.20	0.25	0.30	0.008	0.010	0.012	
E	1.95	2.05	2.15	0.077	0.081	0.085	
E1	1.06	1.16	1.26	0.042	0.046	0.050	
E2	0.82	0.87	0.92	0.032	0.034	0.036	
е		0.65 BSC	•		0.026 BSC		
e1		1.30 BSC			0.051 BSC		
К		0.20 typ.			0.008 typ.		
K1		0.47 typ.			0.019 typ.		
K2		0.23 typ.		0.009 typ.			
K3		0.18 typ.		0.007 typ.			
K4		0.35 typ.		0.014 typ.			
K5		0.35 typ.		0.014 typ.			
K6		0.38 typ.		0.015 typ.			
L	0.15	0.25	0.35	0.006	0.010	0.014	
L1	-	0.10	-	-	0.004	-	
I: C19-1644-Rev. A	10-Jan-2020						

A2 Ŧ

#### Notes

Package outline exclusive of mold flash and metal burr

Package outline inclusive of plating .

Revison: 10-Jan-2020



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