



Features

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TSM35N10CP

100V N-Channel Power MOSFET

TO-252 (DPAK)

Advanced Trench Technology

Low Crss typical @ 45pF (Typ.)

Low gate charge typical @ 34nC (Typ.)

Low $R_{\text{DS(ON)}} \, 37 m \Omega$ (Max.)

Ordering Information

Ordering code

TSM35N10CP ROG

Pin Definition:

1. Gate 2. Drain

3. Source

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (mΩ)	I _D (A)
_	100	37 @ V _{GS} =10V	32

Block Diagram

Gate O

N-Channel MOSFET

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Package

TO-252

Note: Halogen-free according to IEC 61249-2-21 definition

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	100	V	
Gate-Source Voltage		V _{GS}	±20	V	
	T _C =25°C		32		
Continuous Drain Contract	T _C =70°C] ,	26	А	
Continuous Drain Current	T _A =25°C	– I _D	5		
	T _A =70°C]	4		
Drain Current-Pulsed Note 1		I _{DM}	70	А	
Avalanche Current, L=0.1mH		I _{AS} , I _{AR}	35	A	
Avalanche Energy, L=0.1mH		E_{AS},E_{AR}	61	mJ	
	T _C =25°C		83.3		
Maximum Davier Disaination	T _C =70°C		53.3	W	
Maximum Power Dissipation	T _A =25°C	- P _D	2		
	T _A =70°C]	1.3		
Storage Temperature Range		T _{STG}	-55 to +150	°C	
Operating Junction Temperature Range		TJ	-55 to +150	°C	

Packing

2.5Kpcs / 13" Reel

* Limited by maximum junction temperature

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	RƏ _{JC}	1.5	°C/W
Thermal Resistance - Junction to Ambient	RƏ _{JA}	62	°C/W



Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Uni
Static	1			•		
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_{D} = 250uA$	BV _{DSS}	100			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 10A$	R _{DS(ON)}		30	37	mΩ
	$V_{GS} = 4.5V, I_D = 10A$	R _{DS(ON)}		32	42	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \text{uA}$	V _{GS(TH)}	1	2	3	V
Zero Gate Voltage Drain Current	$V_{DS} = 100V, V_{GS} = 0V$	I _{DSS}			1	uA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I _{GSS}			±100	nA
Dynamic						
Total Gate Charge		Qg		34		nC
Gate-Source Charge	$V_{DS} = 50V, I_D = 10A,$ $V_{GS} = 10V$	Q _{gs}		6		
Gate-Drain Charge		Q _{gd}		9		
Input Capacitance	$V_{DS} = 30V, V_{GS} = 0V,$ f = 1.0MHz	C _{iss}		1598		pF
Output Capacitance		C _{oss}		132		
Reverse Transfer Capacitance		C _{rss}		45		
Switching						
Turn-On Delay Time		t _{d(on)}		7		
Turn-On Rise Time	$V_{GS} = 10V, V_{DS} = 50V,$ $R_{G} = 3\Omega$	t _r		7		
Turn-Off Delay Time		t _{d(off)}		29		nS
Turn-Off Fall Time		t _f		7		
Drain-Source Diode Characteristic	s and Maximum Rating					
Drain-Source Diode Forward Voltage	V _{GS} =0V, I _S =10A	V _{SD}		0.7		V
Reverse Recovery Time	I _S = 10A, T _J =25 °C	t _{fr}		32		nS
Reverse Recovery Charge	dl/dt = 500A/us	Q _{fr}		200		nC

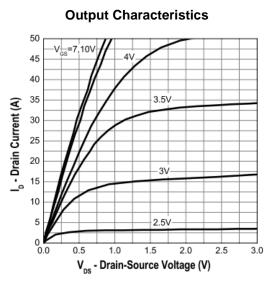
Notes:

1. Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2%.

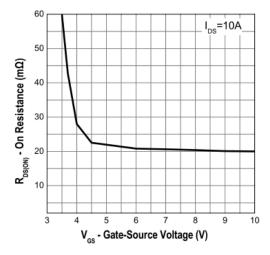
 R_{ΘJA} is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. R_{ΘJC} is guaranteed by design while R_{ΘCA} is determined by the user's board design.



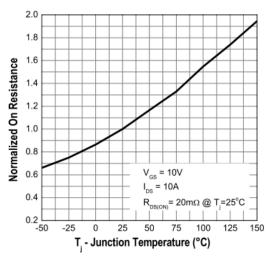
Electrical Characteristics Curve (Tc = 25°C, unless otherwise noted)

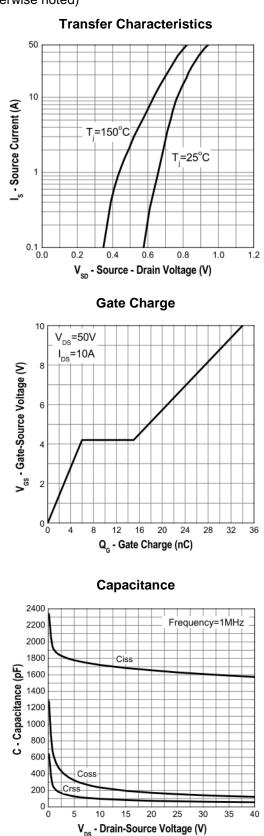


On-Resistance vs. Gate-Source Voltage



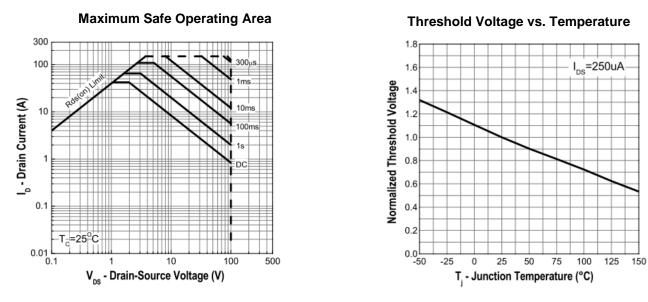
On-Resistance vs. Junction Temperature



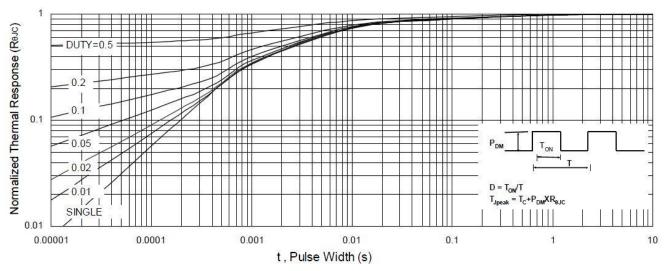




Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

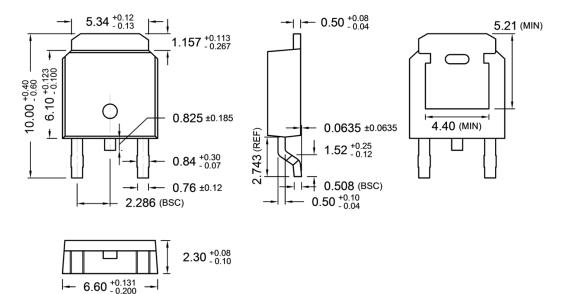


Normalized Thermal Transient Impedance, Junction-to-Ambient



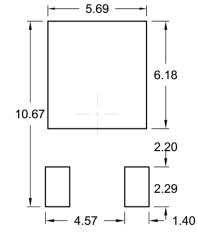


TO-252 Mechanical Drawing

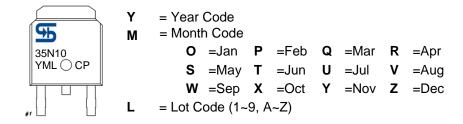


Unit: Millimeters

SUGGESTED PAD LAYOUT (Unit: Millimeters)



Marking Diagram





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