CELLULAR

# SARA-S200

## Size and power optimized RPMA module for the Machine Network™

### Data Sheet


**Abstract**

Technical data sheet describing the SARA-S200 cellular module.

The u-blox SARA-S200 module is an RPMA module in the LGA form factor and with the industry standard 4-wire Serial Peripheral Interface (SPI), allowing for easy integration with various host processors. Operating in the unlicensed 2.4 GHz ISM band, the RPMA network features a demonstrated link budget of up to 176 dB for superior connectivity. The module delivers unprecedented range, capacity, robustness and low power consumption, even in the most demanding of environments.

It is ideal for remote sensing applications that require up to 100 kB daily transmission. It features ultra-low power consumption for applications needing a 10-year or longer battery life.




www.u-blox.com

UBX-17048649 - R02

| Document Information | | |
|---|---|---|
| **Title** | **SARA-S200** | |
| **Subtitle** | Size and power optimized RPMA module for the Machine Network™ | |
| **Document type** | Data Sheet | |
| **Document number** | UBX-17048649 | |
| **Revision and date** | R02 | 24-Nov-2017 |
| **Disclosure restriction** | | |

| Product Status | Corresponding content status | |
|---|---|---|
| **Functional Sample** | Draft | For functional testing. Revised and supplementary data will be published later. |
| **In Development / Prototype** | Objective Specification | Target values. Revised and supplementary data will be published later. |
| **Engineering Sample** | Advance Information | Data based on early testing. Revised and supplementary data will be published later. |
| **Initial Production** | Early Prod. Information | Data from product verification. Revised and supplementary data may be published later. |
| **Mass Production / End of Life** | Production Information | Final product specification. |

## This document applies to the following products:

| Name | Type number | Firmware version | PCN reference | Product Status |
|---|---|---|---|---|
| SARA-S200 | SARA-S200-00B-00 | 8.2.2 | UBX-17053305 | Engineering Sample |

# Contents

# 1 Functional description

## 1.1 Overview

The SARA-S200 is designed to easily integrate with any sensor, enabling robust wireless communication with any application processor. An AP (Access Point) typically can communicate with up to 64,000 RPMA modules, covering an area of 50-200 sq-mi (130-518 sq-km). Ingenu is aggressively deploying the Machine Network™, providing nationwide coverage in the USA. A SARA-S200 module comes from the factory enabled to join any available network, worldwide.

## 1.2 Product features

| Module | Region | Access Technology | Interfaces | | | | Features | | | | | | | | Grade | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RPMA | UART | 7-wire SPI | USB 2.0 | GPIO | FOTA | Full hand-over | Global roaming | Ext. GNSS interface | AssistNow Software | CellLocate® | Integrated GNSS | Embedded programming | Standard | Professional | Automotive |
| **SARA-S200** | Global | 2.4 GHz | | • | | | • | • | • | | | | | | | | |

**Table 1: SARA-S200 main features summary**

## 1.3 Block diagrams

### 1.3.1 Application block diagram

Figure 1 shows how a SARA-S200 module interfaces with a host application running on an application processor.

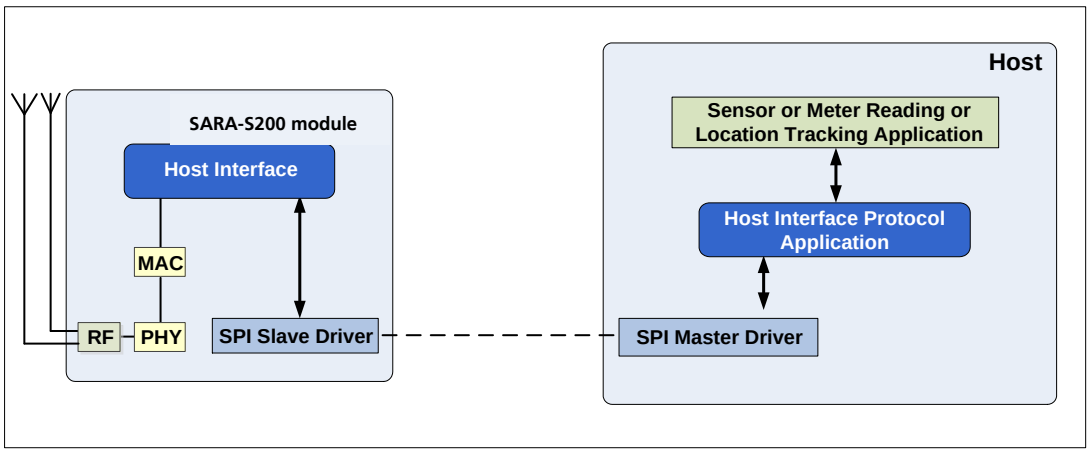


**Figure 1: Typical application diagram**

### 1.3.2 Architecture block diagram

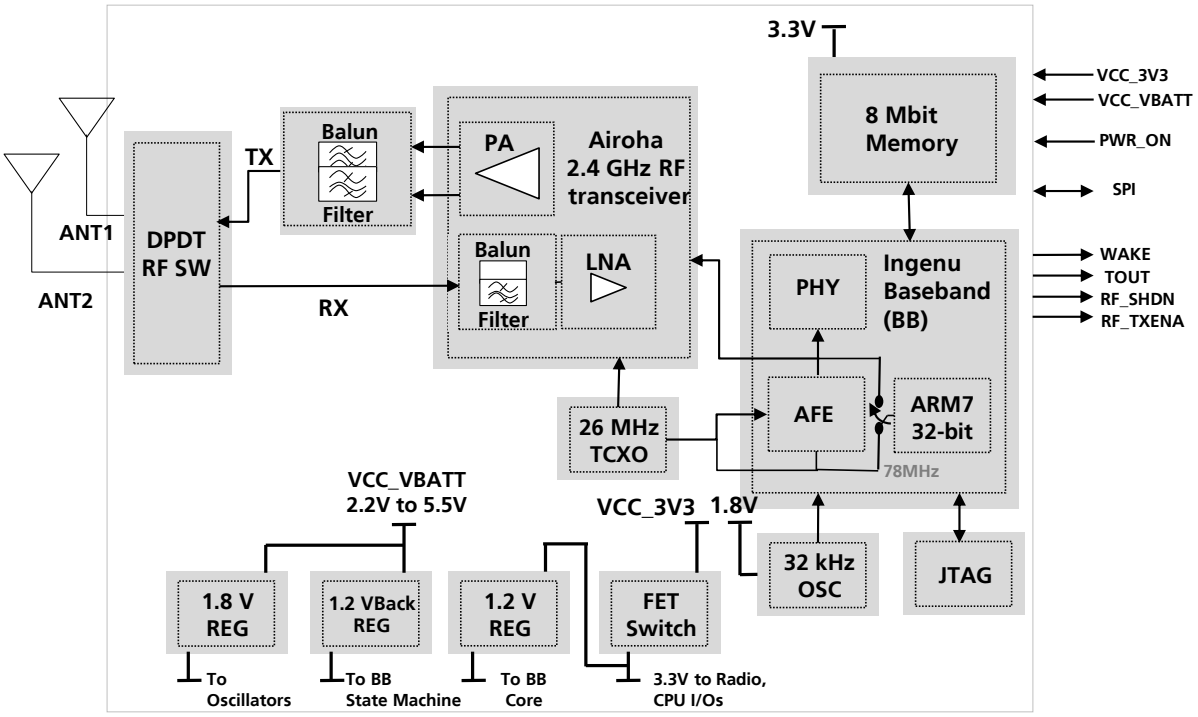


**Figure 2: Internal block diagram**

## 1.4 Product description

The SARA-S200 is a small form factor wireless network module that easily integrates with a microcontroller or application processor using a Serial Peripheral Interface (SPI). The top side of the printed circuit board (PCB) is enclosed with a radio frequency (RF) shield. The compact SARA form factor, 26.0 x 16.0 mm, with LGA pads (functionally, referred to as "pins") allows fully automated assembly with standard pick & place and reflow soldering equipment for cost-efficient, high-volume production

| SARA-S200 characteristics | |
|---|---|
| Single Band Mobile Station | |
| Single-band support:<br>• 2.4 GHz ISM band | <br>2.4 GHz |
| Rx Sensitivity<br>• 2.4 GHz ISM band | <br>-133 dBm |
| Max Tx Power conducted<br>• 2.4 GHz ISM band | <br>+22 dBm |

**Table 2: SARA-S200 characteristics**

# 2 Interfaces

## 2.1 Power management

### 2.1.1 VBATT

The pin supplies a low current of 2.2 V – 5.5 V for the module's internal supervisory circuitry. This pin should be decoupled with a 0.1 µF capacitor on the host processor board.

### 2.1.2 3V3

This pin drives the CPU, transceiver, and RF PA section of the module. It can consume up to 1300 mW. Allow for bypassing with a 47 µF low ESR cap (bulk) and a 0.1 µF ceramic cap for optimal performance. Depending on the host design, there are some nuances that are important regarding this signal:

- The **3V3** pin can be supplied continuously or only when the **WAKE** signal is asserted "high", as for battery powered applications.
- The module runs through various operating states when the **3V3** pin is supplied:
  - If the module internally is in a state that requires no RF, the supply to the **3V3** pin can be "noisy" (it can have +/-100 mV ripple). The RF state is defined by the **RF_SHDN** pin. This allows the host's 3.3 V regulator to work in low quiescent (power save) modes.
  - If the module internally is active and does require RF, the supply to the **3V3** pin must be "clean" (it can have +/-20 mV ripple). This forces the host's 3.3 V supply into a high precision mode and forces a high quiescent current of that regulator.

☞ If the module is operated in a battery mode, when the **3V3** pin is not always enabled, the **3V3** supply must power up and be stable within 2 ms of the **WAKE** signal going "high".

This switching of "noisy" and "clean" becomes clear (and important) when working with battery operated devices and optimal low power drain.

### 2.1.3 PWR_ON

This input signal controls the power-on of the LDO circuitry for the SARA-S200 module. This signal is controlled by the Host Common Library, compiled onto the user's apps processor. See the NANO-S100 / SARA-S200 u-blox Host Common Software Integration Application Note [2] for more details. For reference only: it must be shut off prior to starting the SARA-S200 power-up sequence as defined in the u-blox SARA-S200 System Integration Manual [1]. After the SARA-S200 powers up, this signal is to remain logic high during normal operational modes. This pin dually serves a power on/off function as well as a module reset function.

## 2.2 Serial interface

### 2.2.1 MRQ

The **MRQ** (Master Request) is the host's normal way of waking the SARA-S200 to initiate SPI communications. Logic "high" forces the SARA-S200 awake. This signal is controlled by the Host Common Library, compiled onto the user's application processor.

### 2.2.2 SRDY

**SRDY** (Slave Ready) is an indication from the SARA-S200 that it has fully booted its internal firmware image, initialized its hardware and interfaces, and is ready for communication (arbitration) with the host. Logic "high" indicates that the SARA-S200 is ready for communications. This signal is controlled by the Host Common Library, compiled onto the user's application processor. See the u-blox NANO-100 SARA-S200 Host Common Software Integration Application Note [2] for more details.

### 2.2.3 SRQ

The **SRQ** (Slave Request) signal is an indication from the SARA-S200 that it wants the host's attention. When **SRQ** is asserted "high," the host must read the status registers of the SARA-S200. If **SRQ** is "high," **SRDY** will also be "high." This signal is controlled/handled by the Host Common Library, compiled onto the user's application processor. See the u-blox NANO-S100 / SARA-S200 Host Common Software Integration Application Note [2] for more details.

For battery powered applications, **SRQ** must be connected to a pin that can wake the application processor from sleep.

### 2.2.4 SPI system

The SPI system is the generic term used for all SPI signals (**SPI_MOSI**, **SPI_MISO**, **SPI_CS**, **SPI_SCLK**) to be set up for SPI communications to occur between the host and the SARA-S200. The SARA-S200 SPI is the slave in the master/slave communications. For further details, see the u-blox SARA-S200 System Integration Manual [1].

**Other SPI slaves are not allowed to share the SPI signals.**

**SPI_CS must be controlled by the Host Common Library API to guarantee correct sequencing. Specifically, the user must ensure that the SPI_CS is active (low) for the whole duration of a message transfer, with no gaps. This is implemented in HOST_CMN_HAL_ExchangeMsg in host_cmn_hal_k20.c, in the rACM example code (instructions provided on how to get the starter package with example code when you receive your rACM kit), and must be duplicated for your particular apps processor.**

### 2.2.5 TOUT

This signal is a time synchronizing signal that pulses high upon specific network timing events.

### 2.2.6 RF_TXENA

This signal indicates when the device is transmitting. When transmitting, it is recommended that the host processor use this opportunity as a trigger to read the system "**VCC_VBATT**" power line to show battery voltage under maximum load.

### 2.2.7 RF_SHDN

This module signal indicates status of the RF transceiver of the SARA-S200. If low, the transceiver sleeps (no RX and no TX). This output of the module (3.3 V) indicates when the RF transceiver is on or off. When **RF_SHDN** is high, the RF is "ON" (RX or TX). In the RF "ON" mode, the module needs a "clean" 3.3 V (low ripple) to the **3V3** pin.

### 2.2.8 WAKE

If **WAKE** is used to enable the Host's **3V3** supply for battery-powered mode, then the **3V3** supply must be on and stable within 2 ms of **WAKE** going high.

The **WAKE** signal is generated by the module and is 1.8 V. It signals that it now requires a 3.3 V source to the **3V3** pin. Generally, for a powered module, the **WAKE** is not required since 3.3 V already exists. In the case of battery powered modules, the WAKE turns on the host's main supply to regulate the battery to the required 3.3 V. See the u-blox SARA-S200 System Integration Manual [1] for a powered (non-battery) example circuit and a lithium battery example schematic.

## 2.3 RF antenna interface

### 2.3.1 ANT1 and ANT2

These pins are the RF ports (RX and TX) of the module. They are DC-coupled, 50 Ω and require special host routing of the PCB. **ANT1** is the primary antenna and is always required. **ANT2** is a secondary antenna that the module can use for Antenna Diversity. A single or dual antenna (diversity) system can be configured during the provisioning process. For best results, ensure that the load termination (antenna) has a VSWR of 1.5:1 or better (return loss less than -10 dB).

### 2.3.2 Ring indicator (RING0)

Receipt of specific SMS message will cause the **RING0** line to change level and wake up the host processor.

# 3 Pin definition

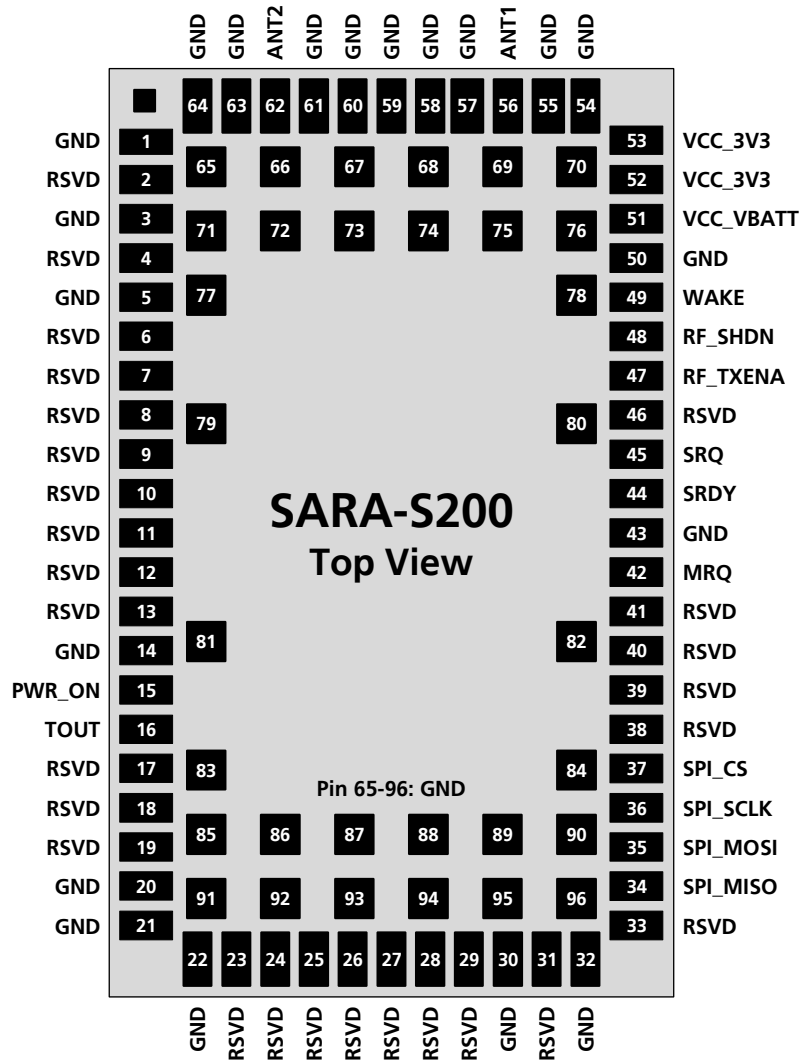


**Figure 3: SARA-S200 pin assignment**

| No | Module | Name | Power domain | I/O | Description | Remarks |
|---|---|---|---|---|---|---|
| 1 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 2 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 3 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 4 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 5 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 6 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 7 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 8 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 9 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 10 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 11 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 12 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 13 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 14 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 15 | All | PWR_ON | GDI | I | ON/OFF control line | This is used to turn ON/OFF the internal power supplies of the SARA-S200. It is controlled by the Host Common Library.<br>• Low: the module consumes less than 1 µA<br>• High: the module is active and will run through a wide range of power states. |
| 16 | All | TOUT | GDI | O | Network timing events | TOUT is a normally low signal that pulses high in response to specific network timing events. It allows an application to trigger a measurement with sub-1ms accuracy. |
| 17 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 18 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 19 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 20 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 21 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 22 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 23 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 24 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 25 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 26 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 27 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 28 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 29 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 30 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 31 | All | RSVD | - | O | RESERVED pin | RESERVED pin |
| 32 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 33 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 34 | All | SPI_MISO | GDI | O | SPI | SPI Master Input Slave Output |
| 35 | All | SPI_MOSI | GDI | I | SPI | SPI Master Output Slave Input |
| 36 | All | SPI_SCLK | GDI | I | SPI | SPI Clock |
| 37 | All | SPI_CS | GDI | I | SPI | SPI Chip Select (Note other slaves are prohibited on the SPI interface, but this pin must be controlled by the Host Common Library). It cannot be tied low on the PCB. |
| 38 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 39 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 40 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 41 | All | RSVD | - | N/A | RESERVED pin | Leave unconnected |
| 42 | All | MRQ | GDI | I | SPI Control Signal | SPI Master Request |
| 43 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 44 | All | SRDY | GDI | O | SPI control signal | SPI Slave Ready |
| 45 | All | SRQ | GDI | O | SPI control signal | SPI Slave Request. SRQ must be connected to a pin that can wake the application processor from sleep, for battery powered applications. |

| No | Module | Name | Power domain | I/O | Description | Remarks |
|---|---|---|---|---|---|---|
| 46 | All | RSVD (TIME_QUAL) | - | N/A | RESERVED pin | Leave unconnected |
| 47 | All | RF_TXENA | GDI | O | PA status | This signal is used to indicate status of the power amplifier for the SARA-S200:<br>• Low: off<br>• High: enabled (Transmitting)<br>The rise edge can be used to trigger a host CPU's ADC read of VBATT (battery voltage while under maximum load). |
| 48 | All | RF_SHDN | GDI | O | RF Transceiver status | This pin indicates the status of the RF Transceiver for the SARA-S200:<br>• Low: shut-down<br>• High: active<br>• It can be used for Wi-Fi/BT coexistence, and to reduce power supply current during low power states (see section 2.1.2) |
| 49 | All | WAKE | - | N/A | RESERVED pin | Leave unconnected. |
| 50 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 51 | All | VCC_VBAT | - | I | Module supply input | Input power to the SARA-S200. This power domain is low current but is used 100% of the time to supply internal supervisory domains |
| 52 | All | VCC_3V3 | - | I | Module supply input | Module supply input. The 3.3 V can be continuously supplied (line powered) or only when the WAKE pin is asserted "high" (battery powered). This power domain is high power (internal CPU, transceiver with RF PA) and should be decoupled with a low ESR, high capacitance capacitor. |
| 53 | All | VCC_3V3 | - | I | Module supply input | |
| 54 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 55 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 56 | All | ANT1 | RF | I/O | Primary RF path | 50 Ω antenna port, DC coupled. ANT1 is required but both ANT1 and ANT2 are desired for antenna diversity. Single port or dual antenna port can be configured in the provisioning process |
| 57 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 58 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 59 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 60 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 61 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 62 | All | ANT2 | RF | I/O | Diversity RF path | 50 Ω antenna port, DC coupled. ANT1 is required but both ANT1 and ANT2 are desired for antenna diversity. Single port or dual antenna port can be configured in the provisioning process. It is strongly recommended to adopt diversity ANT2. |
| 63 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 64 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |
| 65-96 | All | GND | - | N/A | Ground | All the GND pins must be connected to ground |

**Table 3: SARA-S200 pinout**

☞ Pins designated "RESERVED" should be left open and not connected.

☞ The VDD of the internal logic of the SARA-S200 is 3.3 V.

☞ The Host is the SPI master and the SARA-S200 is the SPI slave.

☞ CMOS_I: The module input voltages are 3.3 V CMOS levels. VIH = 2.0 V (min) and VIL = 0.8 V (max).

☞ CMOS_O: The module output voltages are 3.3 V CMOS levels (4 mA). VOH = 2.4 V (min) and VOL = 0.4 V (max).

☞ SPI inputs to the module (**SPI_SCLK**, **SPI_MOSI**, **SPI_CS**) must be tri-stated or driven low when the module may be sleeping (**MRQ** and **SRQ** are both low). See the u-blox SARA-S200 System Integration Manual [1] for more details.

# 4 Electrical specifications

**Stressing the device above one or more of the ratings listed in the Absolute Maximum Rating section may cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other than those specified in the Operating Conditions sections (section 4.2) of the specification should be avoided. Exposure to the Absolute Maximum Rating conditions for extended periods may affect device reliability.**

Operating condition ranges define those limits within which the functionality of the device is guaranteed.

Where application information is given, it is advisory only and does not form part of the specification.

## 4.1 Absolute maximum rating

| Symbol | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| VCC_VBATT | Module supply voltage | Input DC voltage at VCC_VBATT pin | 2.2 | 6.0 | V |
| VCC_3V3 | Module supply current | Input DC voltage at VCC_3V3 pin | 3.1 | 3.5 | V |
| GDI | Digital Interface Signals | Input DC at digital I/O pin | 3.0 | 3.6 | V |
| Tstg | Storage Temperature | | –40 | +85 | °C |
| Topr | Operating Temperature | | –40 | +85 | °C |

**Table 4: Absolute maximum ratings**

**The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in the table above, must be limited to values within the specified boundaries by using appropriate protection devices.**

## 4.2 Operating conditions

Unless otherwise indicated, all operating condition specifications assume an ambient temperature of +25 °C.

**Operation beyond the operating conditions is not recommended and extended exposure beyond them may affect device reliability.**

### 4.2.1 Operating temperature range

Operating outside of these ranges may damage the unit. The SARA-S200 is MSL 4-rated and should be handled as an MSL 4 device per IPC/JEDEC J-STD-020.

| Parameter | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Normal operating temperature | –40 | | +85 | °C | |
| Storage temperature | –40 | | +85 | °C | |
| Humidity | 5 | | 95 | % | Non-condensing humidity |

**Table 5: Environmental conditions**

### 4.2.2 Supply/Power pins

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC_3V3 | Module supply input voltage | 3.2 | 3.3 | 3.4 | V |
| VCC_VBATT | Module low power mode supply input voltage | 2.2 | | 5.5 | V |
| ICC | Module supply peak current consumption* | | | 390 | mA |

* Measured at +22 dBm TX output (Typ=50 Ω), 3.3 V, range includes VSWR ≤ 1.5:1 (PO not compensated).

**Table 6: Input characteristics of the Supply/Power pins**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VOL | VOL – Voltage Output, Low (4mA sink) | 0 | | 0.4 | V |
| VOH | VOH – Voltage Output High (4mA source) | 2.4 | | 3.3 | V |
| SPI | SPI Clock | 0.1 | | 8.6 | MHz |

**Table 7: Digital pin characteristics**

The SPI clock has a maximum rate of 26 MHz/3 and a minimum of 100 kHz. There is no physical limitation on the minimum clock rate but the 100 kHz is deemed "marginal" and is not absolute. Depending on the data traffic model and level of debug traffic, 100 kHz may cause a backup of SPI traffic, which then causes buffer overflow conditions. The application must be validated to ensure that the SPI clock is sufficient to support the required traffic.

### 4.2.3 Power consumption

Table 8 details the SARA-S200 module power consumption characteristics.

| Mode | Min. | Typ. | Max. | Units | Remarks |
|---|---|---|---|---|---|
| Power Off[1] | | 0.1 | 1 | µA | |
| Deep Sleep[1] | | 19 | 30 | µA | |
| Idle Mode[1] | | 21 | 23 | mA | |
| Active Mode - RX enabled[1] | | 105 | 110 | mA | |
| Active Mode - TX at max output | | 320 | 350 | mA | Measured at max +22.0 dBm TX output (Typ=50 Ω), 3.3 V, range includes VSWR ≤ 1.5:1 (PO not compensated). |

**Table 8: SARA-S200 power consumption**

Tested at 3.3 V input:

- Figure 5, Figure 6 and Figure 7 illustrate the representative characterization of power over voltage/temperature and are representative behaviors.

[1] Tested at 3.3 V input:
- Table 8 refers to a maximal current draw that the host system should be designed to accommodate.

### 4.2.4 RF performance

| Parameter | | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Frequency range SIM 2.4 GHz | Uplink | 2402 | 2482 | MHz | Module transmit |
| | Downlink | 2402 | 2482 | MHz | Module receive |

**Table 9: Operating RF frequency bands**

| Parameter | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Receiver input sensitivity | –130 | -133 | -135 | dBm | Sensitivity at maximum DL spreading factor of 11 (2048) with 10% FER. |
| Receiver Image Reject | | -37 | -25 | dBc | |
| Noise Figure | 3.5 | 4.8 | 6.5 | dB | |
| Input IP3 (high LNA gain mode) | | -17 | | dBm | |
| Maximum RF input level for specification compliance | | | -20 | dBm | |
| Condition: 50 Ω source | | | | | |

**Table 10: Receiver sensitivity performance**

| Parameter | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| Frequency Range | 2402 | - | 2482 | MHz | The upper frequency range is market dependent:<br>• FCC/ISED: CH38; 2475.63 MHz<br>• ETSI: CH40; 2475.63 Hz<br>• Japan: CH41; 2481.60 MHz |
| Channel Spacing | - | 1.99 | - | MHz | |
| Condition: 50 Ω source | | | | | |

**Table 11: General RF characteristics**

| Parameter | | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Maximum output power (FCC/IC markets) [2] | | - | 22 | - | dBm | |
| Maximum output power (ETSI markets) | | 8.5 | 9.5 | 10.0 | dBm | |
| Carrier Rejection | | | -50 | -30 | dBc | |
| Signal Modulation | | | DSSS-DBPSK | | | |
| Signal Bandwidth | | | 1.0 | | MHz | |
| BT Factor | | | 0.3 | | | |
| Peak-to-Average Ratio | | | 2.3 | | dB | |
| Spectral bandwidth at maximum RF power: | -6 dB BW | | 0.96 | | MHz | |
| | -20 dB BW | | 1.75 | | MHz | |
| ACPR | | | | -30 | dBc | Spec and test method comes from FCC 15.247(d); Band Edge Emissions, 2 MHz offset. |
| Harmonics | | | | -43 | dBm | At any TX power level, VSWR ≤ 3:1. Harmonics fall into FCC restricted |
| Transmit Power Level Accuracy | | | | +/-1.5 | dB | Estimated sum of all contributors with VSWR ≤ 1.5:1. Normal link mode. |
| | | | | | dBm | At any TX power level, VSWR ≤ 3:1. Applies to spurious, not ACPR or harmonics. Generally the largest spurious output outside the 2.40 - 2.48 GHz band is at 2/3LO and 4/3LO. |
| | | | | | | Maximum VSWR for spec compliance applies at +25 °C only. Slightly degraded ACPR/mask and power variation can be expected at temperature extremes. |

Condition: 50 Ω output load

**Table 12: Transmitter characteristics**

[2] Maximum TX RF power is limited by FCC/IC grant to 22.0 dBm in these markets. Transmit power is configured during network join time to meet country-specific deployment and regulatory requirements. The configurable range is 0 – 22.0 dBm in 1 dB integer increments.

## 4.3 Effects of temperature and voltage

The SARA-S200 module is based largely on Complementary Metal–Oxide–Semiconductor (CMOS) technology. The current drain of CMOS circuitry can vary substantially over temperature. The RF circuitry and its performance also vary substantially over temperature. The SARA-S200 utilizes two main power domains, which are linked to the pins **VCC_VBATT** and **VCC_3V3**.

### 4.3.1 Power domains

#### 4.3.1.1 VCC_VBATT (2.2-5.5V)

This pin powers the low current supervisory/housekeeping circuitry of the module, used while the module is asleep. This voltage supply must be continuous, not under software control. The module autonomously wakes up and synchronizes to the network periodically, without any knowledge by the host apps processor. Figure 4 shows the effect of **VCC_VBATT** on deep sleep power consumption at a nominal VBATT of 3.3 V.

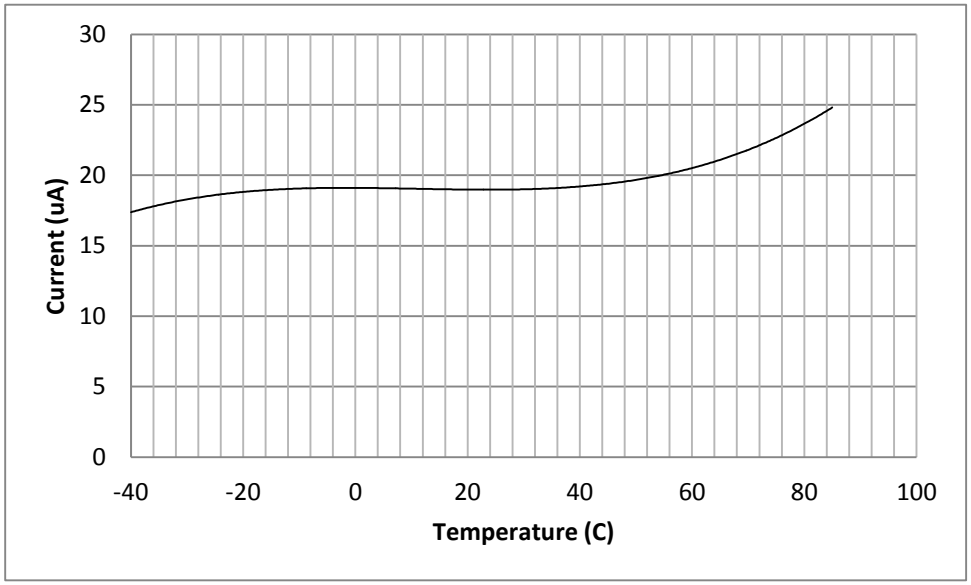


**Figure 4: SARA-S200 Deep sleep current (µA) vs. temperature (°C) at 3.3 V input to the 3V3 pin**

#### 4.3.1.2 3V3 supply

This domain needs a 3.3 V input to **VCC_3V3** when **WAKE** is asserted "high." This power domain is used for the majority of processing, transceiver, and RF Power Amplifier circuitry within the module. These blocks require a lot of power compared to the **VBATT** domain, and the module asserts **WAKE** only when this power (voltage) is required.

Figure 5, Figure 6 and Figure 7 show the relative differences across the operating voltages and their effect on current consumption.

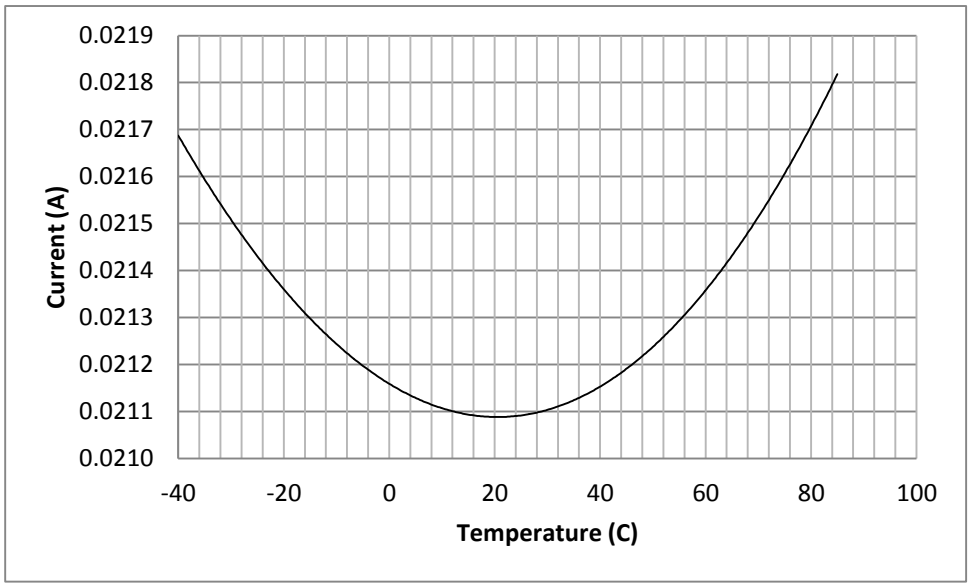


**Figure 5: SARA-S200 idle current (mA) vs. temperature (°C) at 3.3 V input to the 3V3 pin**

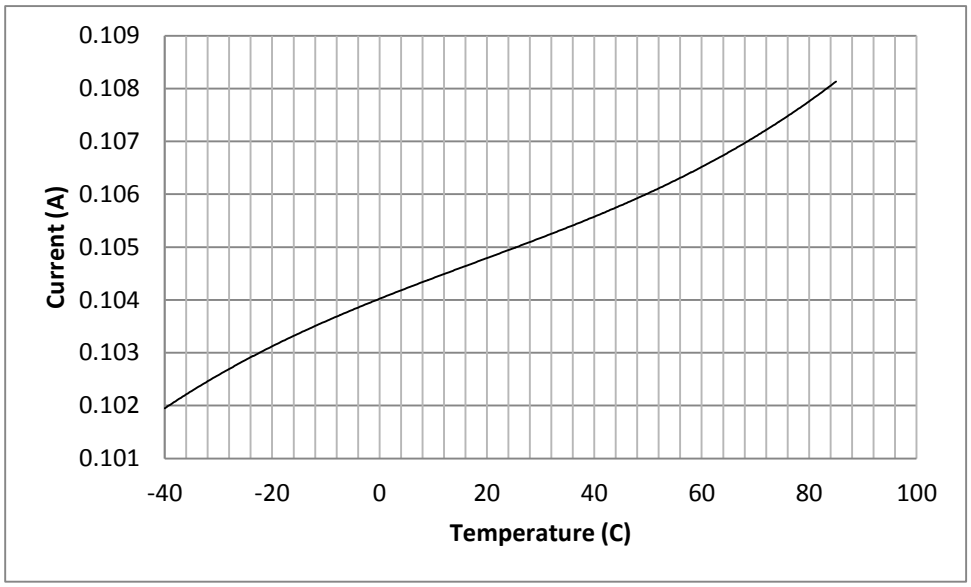


**Figure 6: Maximum Rx gain current (mA) vs. temperature (°C) at 3.3 V input to the 3V3 pin**

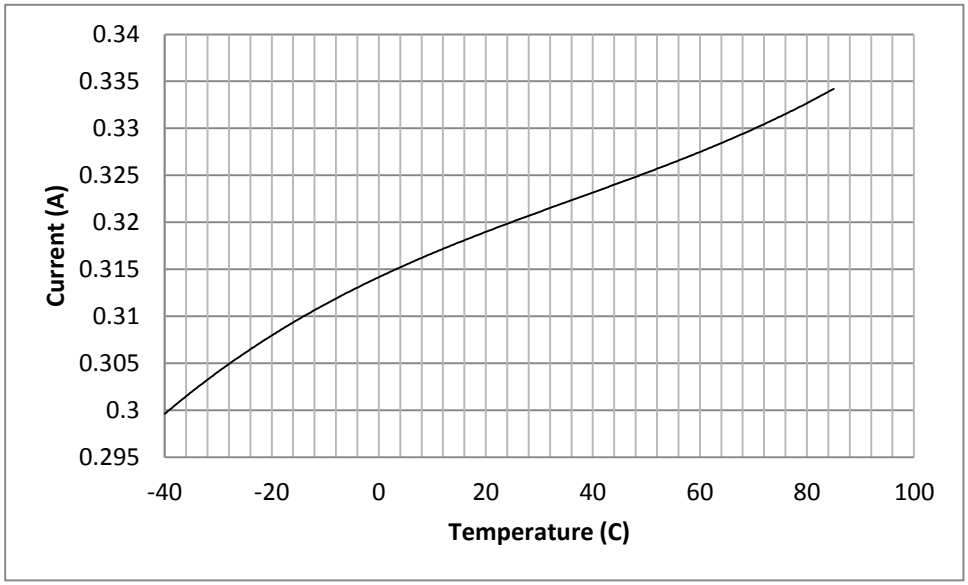


**Figure 7: Maximum target Tx (22 dBm) current (mA) vs. temperature (°C) at 3.3 V input to the 3V3 pin**

# 5 Mechanical specifications

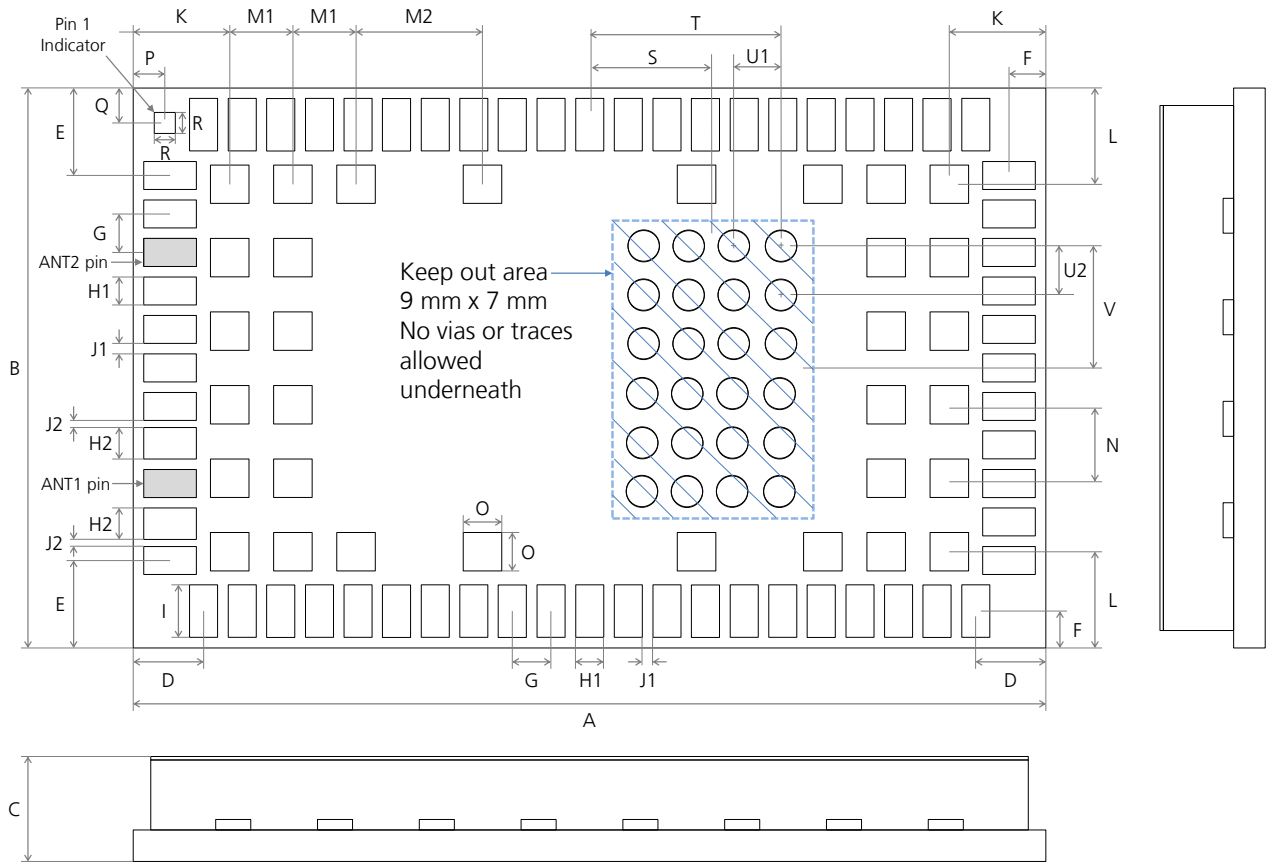


**Figure 8: Dimensions (SARA-S200 bottom, top and side views)**

The mechanical drawing provides the dimensions of the SARA-S200 only and does not reflect the current labeling of the product. See the PCB Land Pattern and Keep-outs for exacting footprint and keep-out dimensions in the SARA-S200 System Integration Manual [1].

| Parameter | Description | Typical | | Tolerance |
|---|---|---|---|---|
| A | Module Height [mm] | 26.0 | (1023.6 mil) | TBD |
| B | Module Width [mm] | 16.0 | (629.9 mil) | TBD |
| C | Module Thickness [mm] | 2.6 | (118.4 mil) | TBD |
| D | Horizontal Edge to Lateral Pin Pitch [mm] | 2.0 | (78.7 mil) | TBD |
| E | Vertical Edge to Lateral Pin Pitch [mm] | 2.5 | (98.4 mil) | TBD |
| F | Edge to Lateral Pin Pitch [mm] | 1.05 | (41.3 mil) | TBD |
| G | Lateral Pin to Pin Pitch [mm] | 1.1 | (43.3 mil) | TBD |
| H1 | Lateral Pin Height [mm] | 0.8 | (31.5 mil) | TBD |
| H2 | Lateral Pin close to ANT Height [mm] | 0.9 | (35.4 mil) | TBD |
| I | Lateral Pin Width [mm] | 1.5 | (59.1 mil) | TBD |
| J1 | Lateral Pin to Pin Distance [mm] | 0.3 | (11.8 mil) | TBD |
| J2 | Lateral Pin to Pin close to ANT Distance [mm] | 0.2 | (7.9 mil) | TBD |
| K | Horizontal Edge to Central Pin Pitch [mm] | 2.75 | (108.3 mil) | TBD |
| L | Vertical Edge to Central Pin Pitch [mm] | 2.75 | (108.3 mil) | TBD |
| M1 | Central Pin to Pin Horizontal Pitch [mm] | 1.8 | (70.9 mil) | TBD |
| M2 | Central Pin to Pin Horizontal Pitch [mm] | 3.6 | (141.7 mil) | TBD |
| N | Central Pin to Pin Vertical Pitch [mm] | 2.1 | (82.7 mil) | TBD |
| O | Central Pin Height and Width [mm] | 1.1 | (43.3 mil) | TBD |
| P | Horizontal Edge to Pin 1 Indicator Pitch [mm] | 0.9 | (35.4 mil) | TBD |
| Q | Vertical Edge to Pin 1 Indicator Pitch [mm] | 1.0 | (39.4 mil) | TBD |

| Parameter | Description | Typical | | Tolerance |
|---|---|---|---|---|
| R | Pin 1 Indicator Height and Width [mm] | 0.6 | (23.6 mil) | TBD |
| S | Horizontal center of module to horizontal center of keep out area box | 3.55 | (139.8 mil) | TBD |
| T | Horizontal center of module to center of furthest test pin towards edge of module | 5.8 | (228.3 mil) | TBD |
| U1 | Test Pin: Central Pin to Pin Horizontal Pitch | 1.5 | (59.1 mil) | TBD |
| U2 | Test Pin: Central Pin to Pin Vertical Pitch | 1.4 | (55.1 mil) | TBD |
| V | Vertical center of module to center of furthest test pin towards edge of module | 3.5 | (137.8 mil) | TBD |
| Weight | Module Weight [g] | < 3 | | |

**Table 13: SARA-S2 series dimensions**

☞ For information regarding Footprint and Paste Mask, see the SARA-S200 System Integration Manual [1].

# 6 Approvals

## 6.1 Approvals

Products marked with this lead-free symbol on the product label comply with "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

SARA-S200 modules are RoHS compliant.

No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

SARA-S200 series modules are approved under the schemes reported in Table 14.

| Country | Scope | ID |
|---|---|---|
| US | FCC | TBD |
| Canada | ISED[3] | TBD |

**Table 14: SARA-S200 certification approvals**

For more details on latest country certification and network operators, see our website www.u-blox.com.

[3] Formerly known as IC (Industry Canada)

# 7 Product handling & soldering

## 7.1 Packaging

SARA-S2 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox Package Information Guide [16].

**Figure 9: Reeled SARA-S2 modules**

### 7.1.1 Reels

SARA-S2 series modules are deliverable in quantities of 250 pieces on a reel. SARA-S2 modules are delivered using reel type B2 as described in the u-blox Package Information Guide [16].

| Parameter | Specification |
|---|---|
| Reel type | B2 |
| Delivery quantity | 250 |

**Table 15: SARA-S200 series standard delivery specifications**

☞ Quantities of less than 250 pieces are also available. Contact u-blox for more information.

### 7.1.2 Tapes

Figure 10 shows the position and the orientation of SARA-S2 series modules as they are delivered on the tape, while Figure 11 and Table 16 specify the tape dimensions.

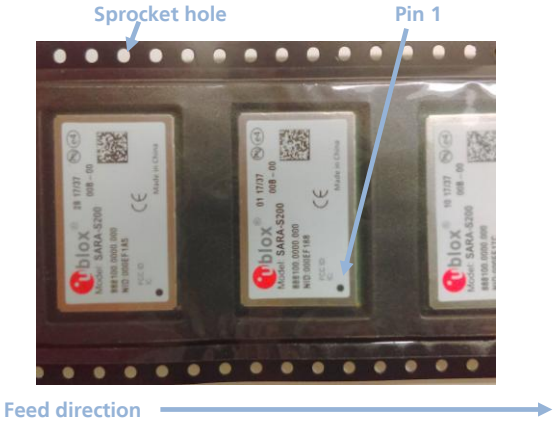


**Figure 10: Reeled SARA modules**

Note 1: 10 sprocket hole pitch cumulative tolerance ± 0.2 mm.

Note 2: Pocket position relative to sprocket hole is measured as the true position of the pocket, not the pocket hole.

Note 3: $A_0$ and $B_0$ are calculated on a plane at a distance "R" above the bottom of the pocket.

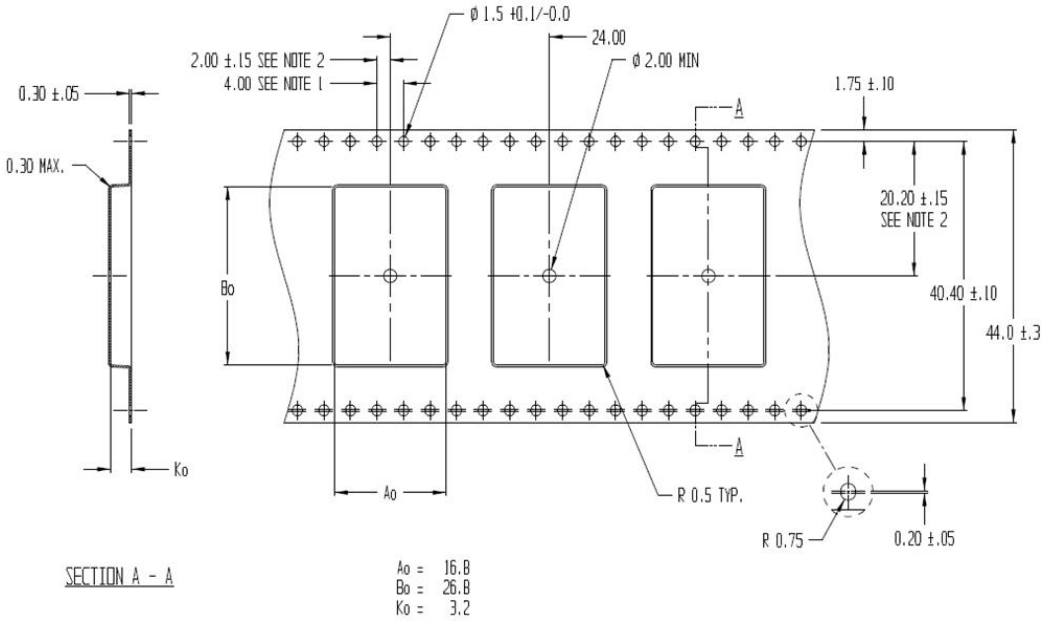


**Figure 11: SARA-S2 series tape dimensions (mm)**

| Parameter | Typical value | Tolerance | Unit |
|---|---|---|---|
| $A_0$ | 16.8 | 0.2 | mm |
| $B_0$ | 26.8 | 0.2 | mm |
| $K_0$ | 3.2 | 0.2 | mm |

**Table 16: SARA-S2 series tape dimensions (mm)**

## 7.2 Moisture Sensitivity Levels

**SARA-S200 modules are Moisture Sensitive Devices (MSD) in accordance to the IPC/JEDEC specification.**

The Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions required. SARA-S200 modules are rated at MSL level 4. For more information regarding moisture sensitivity levels, see the u-blox Package Information Guide [3].

For the MSL standards, see IPC/JEDEC J-STD-020 (can be downloaded from www.jedec.org).

## 7.3 Reflow soldering

The recommended reflow profile is SMT Reflow Profile IPC-7530.

Reflow profiles are to be selected according to u-blox recommendations (see the u-blox SARA-S200 System Integration Manual [1]).

**Failure to observe these recommendations can result in severe damage to the device!**

## 7.4 ESD precautions

**SARA-S200 modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling SARA-S2 modules without proper ESD protection may destroy or damage them permanently.**

The SARA-S200 is designed to be a truly embedded module and can almost be considered an IC. The module is to be placed as a direct-connect to the Host CPU. Therefore, the SARA-S200 has inherent minimal electrostatic discharge (ESD) protection on its I/O.

SARA-S200 modules are Electrostatic Sensitive Devices (ESD) and require special ESD precautions typically applied to ESD sensitive components.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the SARA-S200 module.

| ESD model | Class | Min. voltage |
|---|---|---|
| HBM | Class 1C | > 1000 V |

**Table 17: ESD rating**

**Failure to observe these precautions can result in severe damage to the device!**

RF pins have inherent ESD robustness due to the RF antenna cross switch and survive the 1 kV HBM test. With a shunt 27 nH inductor at the RF pin, the pin can survive direct 8 kV ESD strikes.

If the application is intended for harsh ESD or lightning strike scenarios, it is recommended that the integrator take extra precautions to guard against accidental resets or ESD damage.

## 7.5 Harsh environments

The SARA-S200 employs miniature surface-mounted components in its assembly. If the target design is intended for high humidity or salt environments and intended to have a long service life, it is recommended that the designer take the necessary precautions to guard against prolonged exposure to moisture and other contaminants. A sealed enclosure (IP67 or IP68) or potting may be required in extreme environments.

# 8 Labeling and ordering information

## 8.1 Product labeling

The label on u-blox modules includes important product information.

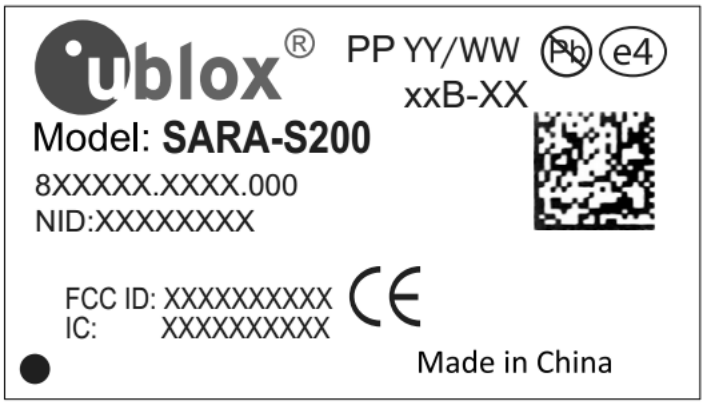


**Figure 12: SARA-S200 module label**

## 8.2 Explanation of codes

Three different product code formats are used. The **Product Name** is used in documentation such as this data sheet and identifies all u-blox products, independent of packaging and quality grade. The **Ordering Code** includes options and quality, while the **Type Number** includes the hardware and firmware versions. Table 18 details the structure of these three different formats.

| Format | Structure |
|---|---|
| **Product Name** | SARA-TGVV |
| **Ordering Code** | SARA-TGVV-MMQ |
| **Type Number** | SARA-TGVV-MMQ-XX |

**Table 18: Product code formats**

Table 19 explains the parts of the product code:

| Code | Meaning | Example |
|---|---|---|
| SARA | Form factor | SARA |
| TG | Platform (Technology and Generation)<br>• Dominant technology: G: GSM; U: HSUPA; C: CDMA 1xRTT; N: NB-IoT; S: RPMA; R: LTE low data rate (Cat 1 and below); L: LTE high data rate (Cat 3 and above)<br>• Generation: 1…9 | S1 |
| VV | Variant function set based on the same platform [00…99] | 00 |
| MM | Major product version [00…99] | 00 |
| Q | Product grade:<br>• B = professional<br>• A = automotive | B |
| XX | Minor product version (not relevant for certification) | Default value is 00 |

**Table 19: Part identification code**

## 8.3 Ordering information

| Ordering No. | Product |
|---|---|
| SARA-S200-00B | Single band 2.4 GHz RPMA module |

**Table 20: Product ordering codes**

# Appendix

# A Glossary

| Name | Definition |
|---|---|
| ACPR | Adjacent Channel Power Ratio |
| AGC | Automatic Gain Control |
| ALC | Automatic Level Control |
| AP | Access Point |
| API | Application Programming Interface |
| ASIC | Application-Specific Integrated Circuit |
| ATE | Automated Test Equipment |
| BCH | Broadcast Channel |
| BOM | Bill of Materials |
| BW | Bandwidth |
| CDLD | Code download |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| CPOL | Clock Polarity (for SPI) |
| CPU | Central Processing Unit |
| DBPSK | Differential Binary Phase Shift Keying |
| DI | Downlink Interval |
| DFS | Dynamic Frequency Selection |
| D-DSSS | Dynamic Direct Sequence Spread Spectrum |
| EIRP | Effective Isotropic Radiated Power |
| EMC | Electromagnetic Compatibility |
| ESD | Electrostatic Discharge |
| ERS | Equivalent Series Resistance |
| FCC | Federal Communication Commission |
| FER | Frame Error Rate |
| FFS | Local File System |
| GDI | Generic Digital Interfaces (power domain) |
| GND | Ground |
| H | High logic signal level |
| HBM | Human Body Model |
| I | Input (means that this is an input port of the SARA-S200) |
| IIP3 | Input Third-Order Intercept Point |
| ISR | Interrupt Service Routine |
| L | Low logic signal level |
| LDO | Low Drop Out |
| LNA | Low Noise Amplifier |
| LGA | Land Grid Array |
| LO | Local Oscillator |
| LPWA | Low Power Wide Area Networks |
| MISO | Master Input, Slave Output |
| MOSI | Master Output, Slave Input |

| Name | Definition |
|---|---|
| MRQ | Master Request |
| MSL | Moisture Sensitivity Level |
| N/A | Not Applicable (used in the I/O field of pinout) |
| NC | No Connect |
| O | Output (means that this is an output port of the SARA-S200) |
| OTA | Over the Air |
| PA | Power Amplifier |
| PCB | Printed Circuit Board |
| PD | Pull-Down |
| Po | "Power Output" for the RF Transmitter |
| POS | Power-On Sequence |
| PU | Pull-Up |
| RSSI | Receive Signal Strength Indicator |
| RPMA | Random Phase Multiple Access |
| RTC | Real Time Clock |
| RX | Receive |
| SCLK | Serial Clock |
| SNR | Serial-to-Noise Ratio |
| SPI | Synchronous Peripheral Interface |
| SRDY | Slave Ready |
| SRQ | Slave Request |
| TCXO | Temperature Compensated Crystal Oscillator |
| T | Tristate |
| TX | Transmit |
| UART | Universal Asynchronous Receiver/Transmitter |
| UI | Uplink Interval |
| VCO | Voltage Controlled Oscillator |
| VSWR | Voltage Standing Wave Ratio |
| XO | Crystal Oscillator |

**Table 21: Explanation of abbreviations and terms used**

# Related documents

[1] u-blox SARA-S200 System Integration Manual, Docu No UBX-17048719

[2] u-blox NANO-S100 / SARA-S200 Host Common Software Integration Application Note, Docu No UBX-16025680

[3] u-blox Package Information Guide, Docu No UBX-14001652

[4] Ingenu rACM Developer Guide Docu No 010-0105-00

[5] u-blox EVK-S10NANO (rACM2) NANO-S100 cellular evaluation kit User Guide, Docu No UBX-16031276

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage.

# Revision history

| Revision | Date | Name | Comments |
|---|---|---|---|
| R01 | 24-Oct-2017 | clee | Initial release |
| R02 | 24-Nov-2017 | clee | Updated power consumption and RF performance |

# Contact

For complete contact information, visit us at www.u-blox.com

**u-blox Offices**

**North, Central and South America**

**u-blox America, Inc.**
Phone: +1 703 483 3180
E-mail: info_us@u-blox.com

**Regional Office West Coast:**
Phone: +1 408 573 3640
E-mail: info_us@u-blox.com

**Technical Support:**
Phone: +1 703 483 3185
E-mail: support_us@u-blox.com

**Headquarters**
**Europe, Middle East, Africa**

**u-blox AG**
Phone: +41 44 722 74 44
E-mail: info@u-blox.com
Support: support @u-blox.com

**Asia, Australia, Pacific**

**u-blox Singapore Pte. Ltd.**
Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

**Regional Office Australia:**
Phone: +61 2 8448 2016
E-mail: info_anz@u-blox.com
Support: support_ap@u-blox.com

**Regional Office China (Beijing):**
Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

**Regional Office China (Chongqing):**
Phone: +86 23 6815 1588
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

**Regional Office China (Shanghai):**
Phone: +86 21 6090 4832
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

**Regional Office China (Shenzhen):**
Phone: +86 755 8627 1083
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

**Regional Office India:**
Phone: +91 80 4050 9200
E-mail: info_in@u-blox.com
Support: support_in@u-blox.com

**Regional Office Japan (Osaka):**
Phone: +81 6 6941 3660
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

**Regional Office Japan (Tokyo):**
Phone: +81 3 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

**Regional Office Korea:**
Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

**Regional Office Taiwan:**
Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com