

# N-Channel 40 V (D-S) MOSFET

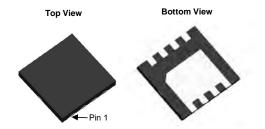
PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$ (Max.)	I <sub>D</sub> (A) <sup>f</sup>	Q <sub>g</sub> (Typ.)			
40	0.0045 at V <sub>GS</sub> = 10 V	40 <sup>g</sup>	9.8 nC			
40	0.0062 at V <sub>GS</sub> = 4.5 V	40 <sup>g</sup>	9.0110			

### **FEATURES**

- TrenchFET® Power MOSFET
- 100 % R<sub>q</sub> and UIS Tested
- Capable of Operating with 5 V Gate Drive



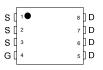
#### DFN 3x3 EP

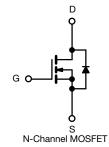


#### **APPLICATIONS**

- Synchronous Rectification
- Synchronous Buck Converters
- **ORing**
- Load Switching
- Motor Drive Switch

#### **Top View**





Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	40	v		
Gate-Source Voltage		$V_{GS}$			± 20
	T <sub>C</sub> = 25 °C		40 <sup>g</sup>		
Continuous Dunin Comment (T. 150 °C)	T <sub>C</sub> = 70 °C	1 .	40 <sup>g</sup>		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	19.3 <sup>a, b</sup>		
	T <sub>A</sub> = 70 °C		15.5 <sup>a, b</sup>	^	
Pulsed Drain Current (t = 100 μs)		I <sub>DM</sub>	100	A	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C		40 <sup>g</sup>		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	3.1 <sup>a, b</sup>		
Single Pulse Avalanche Current L = 0.1 mH		I <sub>AS</sub>	20		
Single Pulse Avalanche Energy	L = 0.1 IIII	E <sub>AS</sub>	20	mJ	
	T <sub>C</sub> = 25 °C		52		
Maximum Dawar Dissination	T <sub>C</sub> = 70 °C		33	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.7 <sup>a, b</sup>	VV	
	T <sub>A</sub> = 70 °C		2.4 <sup>a, b</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Tempera		260			

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>a, e</sup>	t ≤ 10 s	R <sub>thJA</sub>	26	33			
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.9	2.4	°C/W		

#### Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s. c. The DFN 3 x 3 EP is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components. e. Maximum under steady state conditions is 81  $^{\circ}$ C/W. f. Based on T<sub>C</sub> = 25  $^{\circ}$ C. g. Package limited.



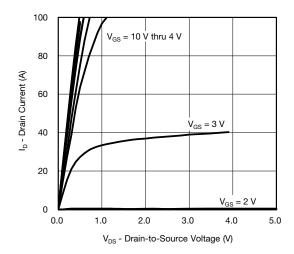
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V, } I_D = 250 \mu\text{A}$	40			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L 050 vA		56		>//06
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6		mV/°(
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1.1		2.2	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zoro Cata Valtaga Drain Current	_	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μА
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α
Drain Course On Ctata Basistanas <sup>a</sup>	Б	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	0.0045			0
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$		0.0062		Ω
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		65		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>			1330		pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1200		
Reverse Transfer Capacitance	C <sub>rss</sub>			66		
Total Octo Observe		$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		21.3	32	nC
Total Gate Charge	$Q_g$			9.8	15	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$		3.2		
Gate-Drain Charge	Q <sub>gd</sub>			2.5		
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V		32	48	
Gate Resistance	$R_{g}$	f = 1 MHz	0.2	0.9	1.5	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			22	44	
Rise Time	t <sub>r</sub>	$V_{DD} = 20 \text{ V}, R_{I} = 2 \Omega$		65	120	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		24	45	
Fall Time	t <sub>f</sub>			9	18	
Turn-On Delay Time	t <sub>d(on)</sub>			11	22	ns
Rise Time	t <sub>r</sub>	$V_{DD} = 20 \text{ V}, R_L = 2 \Omega$		11	22	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	44	
Fall Time	t <sub>f</sub>			9	18	•
Drain-Source Body Diode Characteristic						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			40	
Pulse Diode Forward Current ( $t = 100 \mu s$ )	I <sub>SM</sub>	-			100	A
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 4 A, V <sub>GS</sub> = 0 V		0.75	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	- 50		31	60	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			17	34	nC
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		13		
Reverse Recovery Rise Time	t <sub>b</sub>			18		ns

#### Notes:

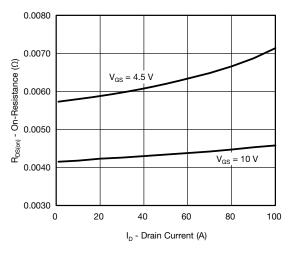
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

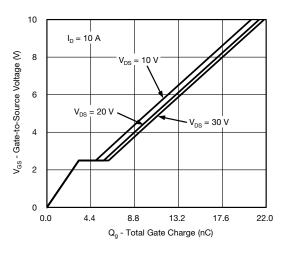




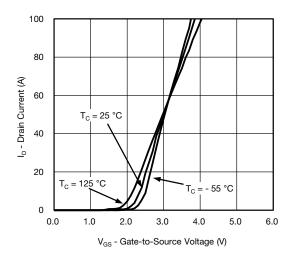
### **Output Characteristics**



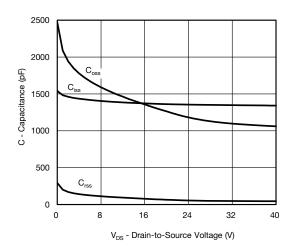
On-Resistance vs. Drain Current and Gate Voltage



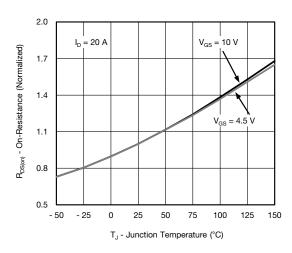
**Gate Charge** 



**Transfer Characteristics** 

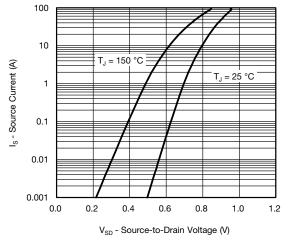


Capacitance

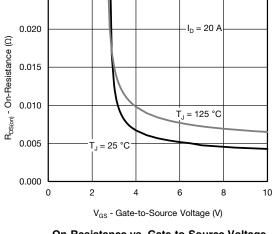


On-Resistance vs. Junction Temperature



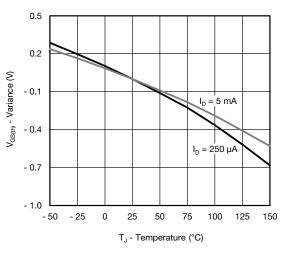


Source-Drain Diode Forward Voltage

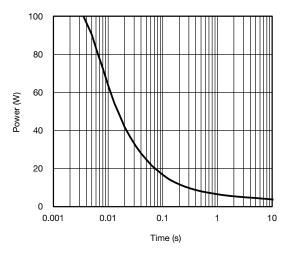


0.025

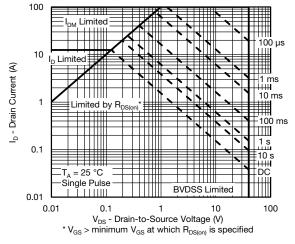
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

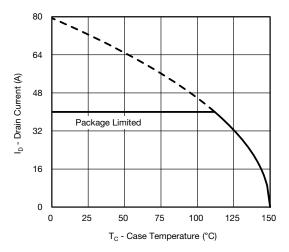


Single Pulse Power, Junction-to-Ambient

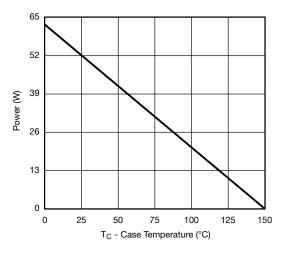


Safe Operating Area, Junction-to-Ambient

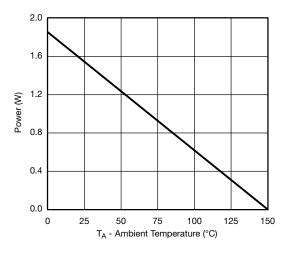




#### **Current Derating\***



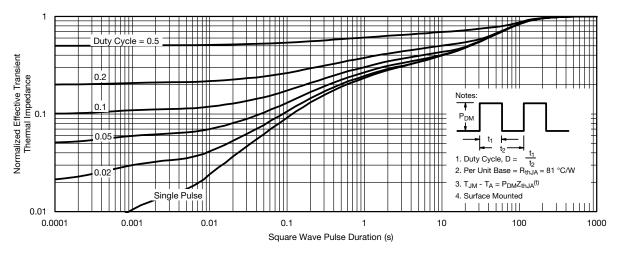




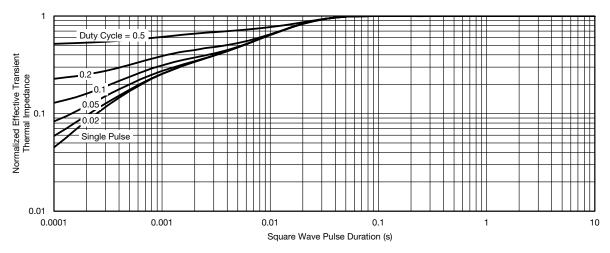
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



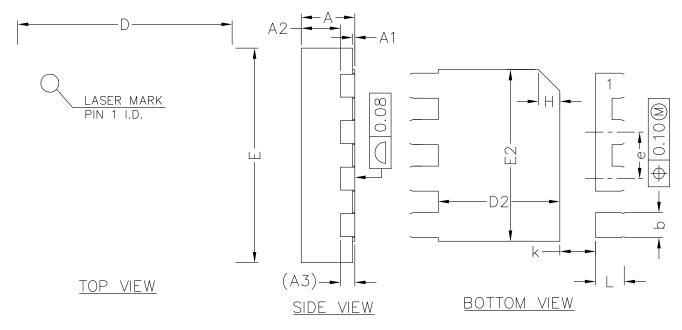


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case







COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX		
А	0.70	0.75	0.80		
A1	0.00	0.02	0.05		
A2	0.50	0.55	0.60		
А3	0.20REF				
Ь	0.30	0.35	0.40		
D	2.90	3.00	3.10		
Ε	2.90	3.00	3.10		
D2	1.60	1.70	1.80		
E2	2.30	2.40	2.50		
е	0.55	0.65	0.75		
K	0.40	0.50	0.60		
L	0.35	0.40	0.45		



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