

16-Port 10/100 + 3-Port 10/100/1000Mb Ethernet Switch

Features List

- 16-Port 10/100Mb + 3-Port 10/100/1000Mb Ethernet Switch
 - Built-in 16 10/100Mb PHYs
 - RGMII interface for 2 10/100/1000Mb PHYs
 - 1 GMII/RGMII/MII interface for external CPU (optional)
 - Support IEEE802.3az
 - Support 10/100Mb full/half duplex
 - Support 1000Mb full duplex
 - 100Mb TP and Fiber dual mode, selected by Signal Detection (SD) level
- Store & Forward, Share Memory Non-blocking Architecture
 - Built-in 4Mb SRAM for packet buffer
 - Support 16K Jumbo packet
 - Max. length 1664B without supporting jumbo packet
- Wire-Speed Operation On Every Port
- Head Of Line Blocking Prevention
- Flow Control
 - 802.3x compliant flow control in full duplex
 - Collision/Carrier_ sense based backpressure in half duplex
- Internal 16K MAC Address Entities
 - CRC/Direct hashing algorithm
 - Aging timer programmable (55s~500hrs)
 - Wire speed address learning and resolution
 - CPU accessible for security and static MAC
 - Learning enable/disable
- IGMP/MLD Snooping
 - IGMP Version 1, 2, 3 / MLD Version 1, 2
 - MLD snooping. (4 sets IP address per MLD list)
 - Snooping by Switch ASIC or CPU
- Four Trunk Group
 - Three trunk groups, trunk A~C up to 4 ports
 - Trunk D has only 2 ports
 - Load balance based on (Port ID, DA, SA, DA/SA, IP, TCP/UDP)
 - Link fault recovery
- Per Port 41 MIB Counters/port
 - RMON/ Ethernet/ MIB II
- Hardware Auto loop detection
- VLAN
 - 19 Port based
 - 4K Tag based
 - Support Tag remove/add/modify
 - IVL/SVL learning mode
 - Support Protocol VLAN
 - Support Q-in-Q (double tag)
 - 64 configurable VID for Q-in-Q tag stacking
- Class Of Service (CoS)
 - Support FIFS/SP/WRR/SP+WRR/WFQ/TWRR in Output Queue Schedule Modes
 - Port based priority
 - 802.1Q priority tag based
 - IP TOS based (IPv4/IPv6)
 - TCP/UDP port number based
 - Source MAC address based
 - ACL based
 - Privilege priority
 - 8 levels per port
- Priority queuing decision
 - DSCP/ TAG priority remarking
 - 802.1Qad PCP, DEN insert / modify
 - 802.1Q PCP, CFI insert/ modify
 - RX &TX Priority re-mapping
 - LLQ + latency
- Broadcast/multicast/DLF/ARP/ICMP Storm Control
 - 256 levels resolution for all storm control
 - Storm control can be enabled for per port
 - With option to drop all ARP to CPU
 - Unit time can be selected for all storm control
- Sniffer Function
 - Ingress 、 egress 、 ingress/egress methods
 - Two Sniffer destination port group configurations
 - Add/ Remove Tag option for packet routing to mirroring ports
 - ACL and special tag for sniffer application
- Port Security
 - MAC based
 - TCP/UDP port based
 - SIP based
 - 802.1x Port based

- Bandwidth Control
 - From 64K bps to wire speed (resolution 64k)
 - Support Flow control on/off
 - Queue based bandwidth control (resolution 64k/1M/2M/4M)
- SMI Interface Auto-Polling
 - Speed, Duplex, Flow control, Link
 - CPU accessible and interrupt
 - CPU R/W PHY register
 - Support MMD access
- Out Queue
 - Frame buffer/ queue/ port based aging
 - Bandwidth assured/ limited
 - Latency assured
 - WRED(Weight Random Early Drop)
 - Support LLQ (Low latency queue)
 - Dorm mode (WAN/LAN dual schedule mode)
- Spanning Tree Protocol Port State
 - Support Discard/Block/Learning/Forwarding four states
 - Forwarding STP frame to CPU port
 - Support RSTP/MSTP
- Access Control List
 - 128 ACL Entities
 - Ingress port
 - VLAN
 - Destination/Source MAC address
 - Destination/Source IP (specific or range)
 - TCP/UDP Destination/Source port number (specific or range)
 - IP protocol, DSCP, TCP flag
 - Action : forward, to CPU, drop, priority, Q-in-Q tag, remarking, redirect, bandwidth limited
- Configuration
 - Pin initial setting
 - 2-wire serial interface for accessing EEPROM
 - Advanced EEPROM program mode
 - 2/4-wire serial interface for low cost smart system application
- Programmable serial LED Display Function
 - 8 modes/ flashing speed selectable
 - Power on cable diagnosis indication
 - Loop indication
- Auto Test Function For Mass-production
 - Auto generate test frames
 - Show the result on LED output
- Interrupt Pin For PHY Mode/Link/SMI R/W
 - Complete notification
- Special TAG
- OAM (IEEE 802.3 ah)
 - Auto discovery
 - Fault indication
 - Remote LoopBack test
- IEEE1588 stamp
 - 16 time stamps for Ingress/Egress per port
 - Support Event trigger stamp
 - Support Pulse Per Second (PPS) output
 - Support PTP trigger out
- IC+ Remote Management Protocol (IRMP)
- Build-in SRAM Self Test (BIST)
- sFlow
- EoC cable failure auto detection and isolation hardware
- L3/L2 Protocol packets forwarding to CPU or broadcast or drop
 - LACP,LLDP,IGMP,MLD,ICMP,BPDU,802.1x, GARP
- IPv6 function
 - TCP/UDP port number and FLAG
 - Finding out next header is based on ICMPv6, authentication, encapsulation, fragment or user-defined header
- Only need one 25MHz Crystal
- Adjustable IO voltage
 - (2.5V~3.3V of RGMII/MII for port 19, 2.0V~3.3V of RGMII for port 17~ port 18)
- Built-in 2.0V regulator
- 176 TQFP , 177 E-Pad Ground

General Description

IP1819I is a non-blocking, store-and-forward architecture switch controller, which builds 16-port 10/100Mbps Fast Ethernet MAC and PHY, 3-port Gigabit Ethernet MAC including 2-port RGMII, and one-port RGMII/MII for external CPU in a single chip.

IP1819I embeds a 4Mb SRAM for the use of packet buffer. It also provides various 2-wire interfaces, such as CPU interface, SMI, and EEPROM interface, which allow the user to access the internal register, external PHY's registers and EEPROM data. The serial LED can show the status of each port (such as Link, Speed, Activity and so on) by using 74HC164 or IP403 external device through 2-wire (LED_CLK, LED_DAT) signals driving from IP1819I.

For avoiding loop occur, IP1819I supports STP, RSTP and MSTP. Even a hardware loop detection mechanism is supported.

There are 16K entries in Lookup table. Hashing method can be selected either direct or CRC hashing for MAC address learning. Lookup Table aging time can be adjustable ranging from 55 seconds to 500 hours. IP1819I also provides the MAC learning threshold to limit the number of addresses learning.

An independent Multicast table supports 256 entries. For the Internet Group Management Protocol, IP1819I supports IGMP v1/v2/v3 for IPv4 and MLD v1/v2 for IPv6 packet snooping and aging time function. For the IGMPv3 and MLDv2 application, IP1819I provides up to 10 sets IPv4 or 4 sets IPv6 address per entry for source list table.

IP1819I has 4k entries for 802.1Q VLAN, which provides more security for VLAN member, and supports Independent VLAN Learning (IVL) and Share VLAN Learning (SVL). Further, IP1819I also has add/remove C-tag, S-tag, VLAN remarking, uplink link port and inactive VID redirect functions for the flexible VLAN application.

IP1819I has 128 entries for ACL table. The ACL (Address Control List) function provides advanced and flexible control mechanism to decide what packet should do (action) if packet matches ACL rule. ACL Rule and action:

- Rules: (Port ID, DA, SA, DA/SA, DIP, SIP, TCP/UDP Port Number (DP and SP))
- Actions: (Sniffer, Insert/remove Tag, Priority, Redirection, Trap to CPU, BW limited, DSCP, sFlow, Drop, PTP, MIB Counter)

For the Quality of Service application, IP1819I supports port-based, 802.1Q tag based, ACL based, IP CoS/DSCP based, SMAC based, IP address based, IGMP based and WAN/LAN based to decide the priority of output frame. For the Remarking application, IP1819I supports remarking for the DSCP, Ctag and Stag value of transmit packet.

For the link aggregation application, IP1819I provides eight hashing methods (Port ID, DA, SA, DA/SA, DIP, SIP, DP, and SP) and support four trunk groups' sets.

For meeting the various network applications, IP1819I also supports storm control, bandwidth rate control, Output Queues functions, Sniffer, sFlow, PTP, MIB counters and eight LED display modes. Therefore, IP1819I has the best adaptability and capability for the future network conditions.

IP1819I supports the web based management interface, such as Microsoft Internet Explorer or Mozilla Firefox, Google chrome, user can more easily configure IP1819I's functions by these browsers. Besides, IP1819I also provides IRMP(IC+ remote management protocol) to let the users remotely configure the registers of IP1819I.

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Revision History

Revision #	History Description	Date
IP1819I-DS-R01	Initial release	2020/02/05
IP1819I-DS-R02	Updated power on sequence (page 173) Added thermal data of IC Plus 2 layers PCB (page 182)	2020/05/07
IP1819I-DS-R03	Removed Max. clock cycle time of CPU I/F (page 175) Updated Group 0 description of Table 23 (page 46) Updated default value of page 0x0 register 0xB5 (page 96) Updated Max. of Supply Voltage (page 172) Updated TWRR tickle unit (page 141) Updated description of forwarded IGMPv3 packet (page 57) Updated power on sequence and reset timing diagram (page 173) Updated specification of Receiver common mode voltage (page 180)	2020/09/25
IP1819I-DS-R04	Updated page 0x1 register 0xE0 (page 107) Updated Crystal & X1 Clock Input Specification (page 181)	2022/01/04

1 Pin Diagram

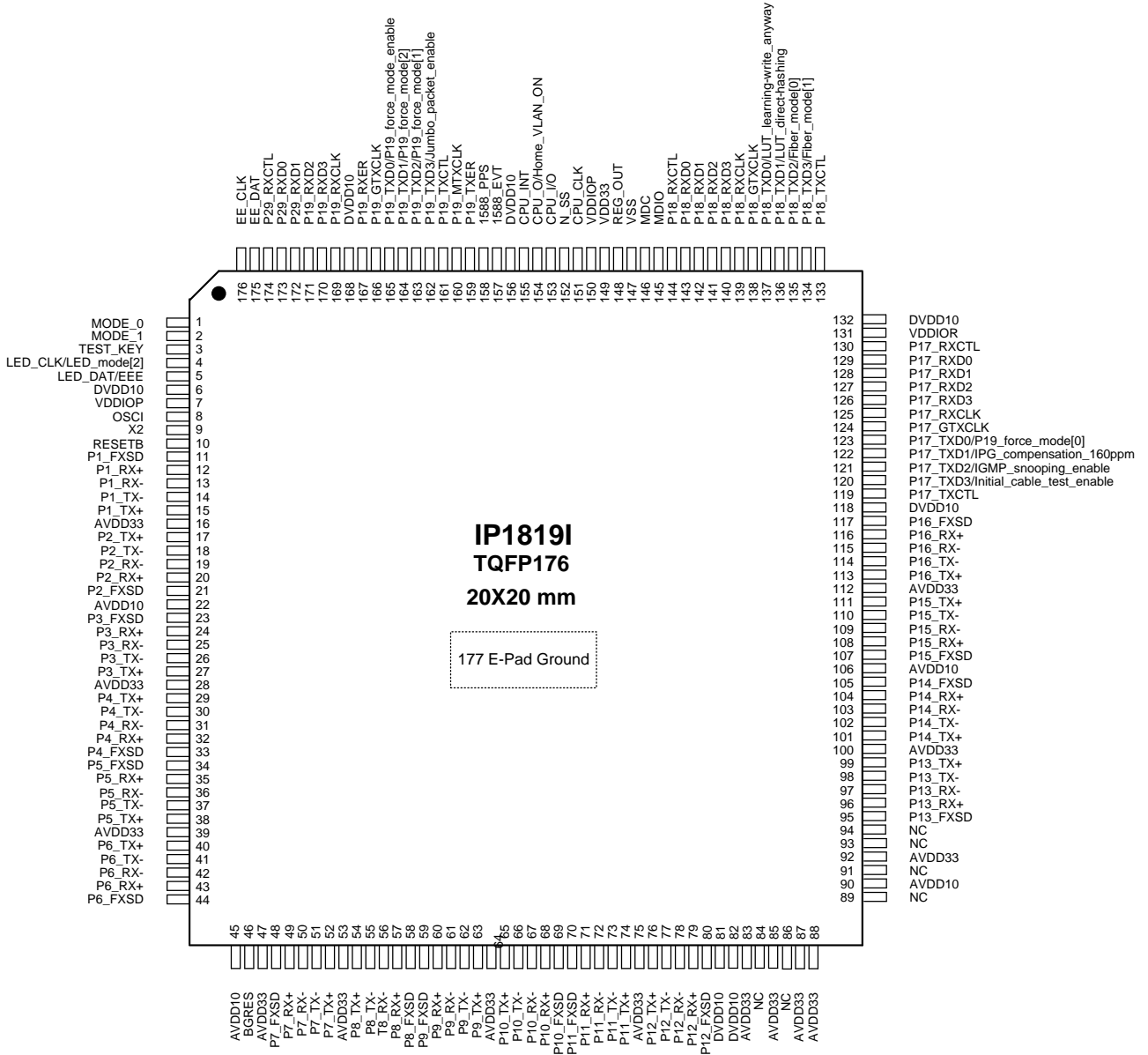


Figure 1 IP1819I TQFP 176 Pin Diagram

2 Block Diagram

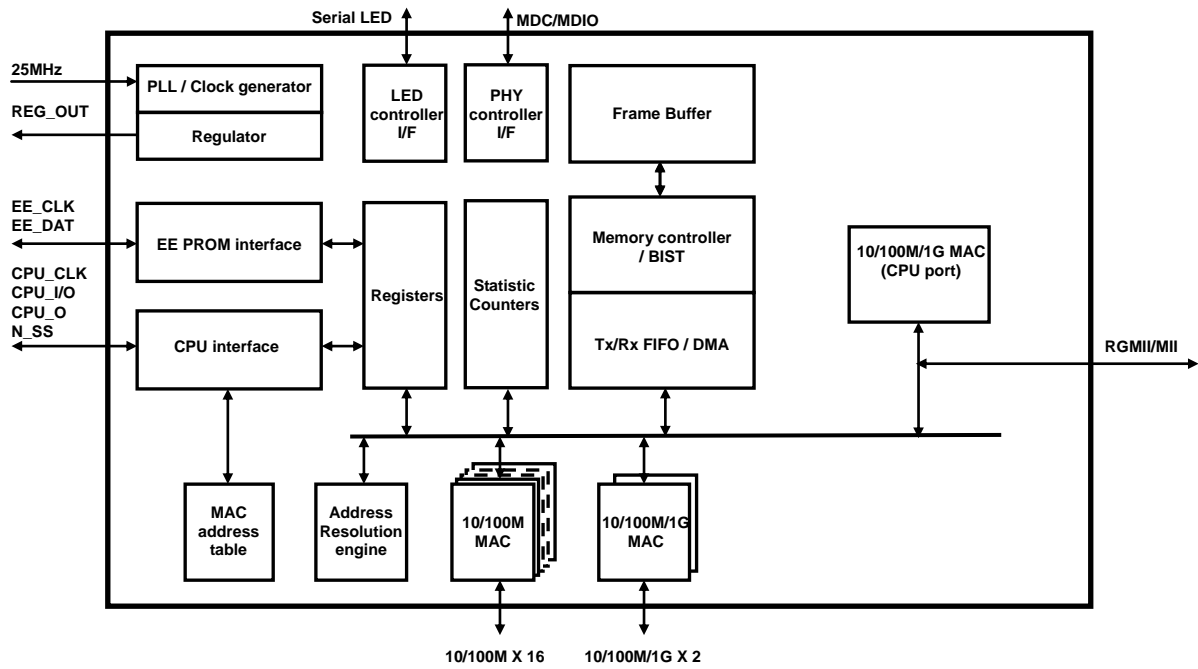


Figure 2 Block Diagram

3 Application Diagram

16 10/100M + 3G Combo Dumb Switch Application

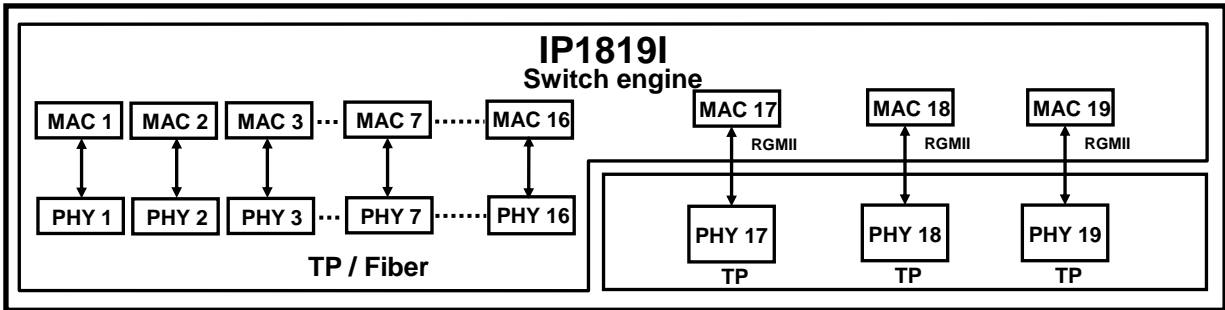


Figure 3 Dumb Switch Application Diagram

16 10/100M + 2G Combo Smart / Management Switch Application

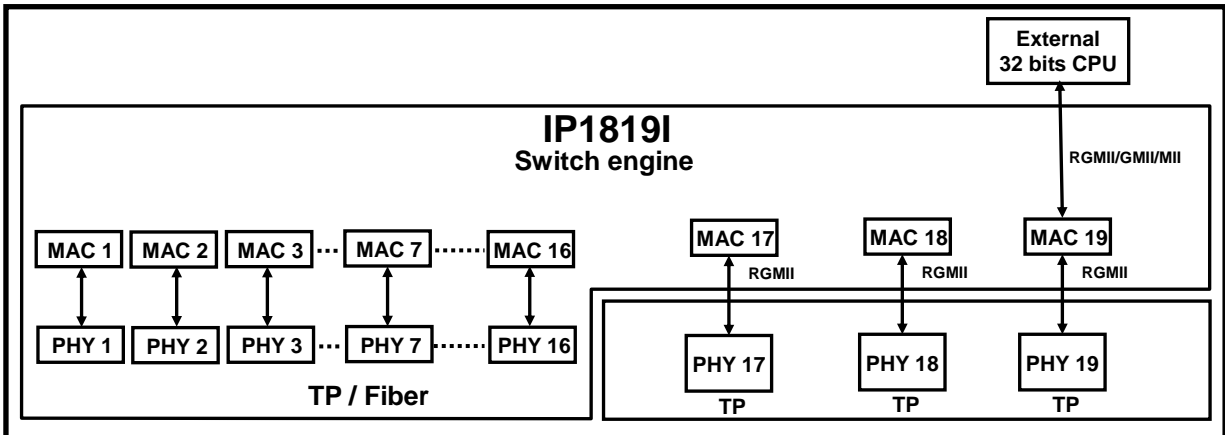


Figure 4 Smart / Management Switch Application Diagram

4 Pin Description

Table 1 Pin Symbol Abbreviation

Type	Description	Type	Description
I	Input pin	IL	Input latched upon reset
O	Output pin	PD	Pulled down with internal resistor
I/O	Bi-direction input/output	PU	Pulled up with internal resistor
P	Power or ground		

Table 2 MDI Pin

Pin No.	Label	Type	Description
Medium Dependent Interface (port 1~16,PHY address 8~19, 28~31)			
15 14 12 13	P1_TX+ P1_TX- P1_RX+ P1_RX-	O O 	Port 1 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 1. Auto MDI/MDIX can reverse the pairs P1_TX+/P1_TX- and P1_RX+/P1_RX-.
17 18 20 19	P2_TX+ P2_TX- P2_RX+ P2_RX-	O O 	Port 2 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 2. Auto MDI/MDIX can reverse the pairs P2_TX+/P2_TX- and P2_RX+/P2_RX-.
27 26 24 25	P3_TX+ P3_TX- P3_RX+ P3_RX-	O O 	Port 3 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 3. Auto MDI/MDIX can reverse the pairs P3_TX+/P3_TX- and P3_RX+/P3_RX-.
29 30 32 31	P4_TX+ P4_TX- P4_RX+ P4_RX-	O O 	Port 4 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 4. Auto MDI/MDIX can reverse the pairs P4_TX+/P4_TX- and P4_RX+/P4_RX-.
38 37 35 36	P5_TX+ P5_TX- P5_RX+ P5_RX-	O O 	Port 5 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 5. Auto MDI/MDIX can reverse the pairs P5_TX+/P5_TX- and P5_RX+/P5_RX-.
40 41 43 42	P6_TX+ P6_TX- P6_RX+ P6_RX-	O O 	Port 6 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 6. Auto MDI/MDIX can reverse the pairs P6_TX+/P6_TX- and P6_RX+/P6_RX-.
52 51 49 50	P7_TX+ P7_TX- P7_RX+ P7_RX-	O O 	Port 7 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 7. Auto MDI/MDIX can reverse the pairs P7_TX+/P7_TX- and P7_RX+/P7_RX-.

Pin No.	Label	Type	Description
54 55 57 56	P8_TX+ P8_TX- P8_RX+ P8_RX-	O O 	Port 8 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 8. Auto MDI/MDIX can reverse the pairs P8_TX+/P8_TX- and P8_RX+/P8_RX-.
63 62 60 61	P9_TX+ P9_TX- P9_RX+ P9_RX-	O O 	Port 9 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 9. Auto MDI/MDIX can reverse the pairs P9_TX+/P9_TX- and P9_RX+/P9_RX-.
65 66 68 67	P10_TX+ P10_TX- P10_RX+ P10_RX-	O O 	Port 10 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 10. Auto MDI/MDIX can reverse the pairs P10_TX+/P10_TX- and P10_RX+/P10_RX-.
74 73 71 72	P11_TX+ P11_TX- P11_RX+ P11_RX-	O O 	Port 11 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 11. Auto MDI/MDIX can reverse the pairs P11_TX+/P11_TX- and P11_RX+/P11_RX-.
76 77 79 78	P12_TX+ P12_TX- P12_RX+ P12_RX-	O O 	Port 12 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 12. Auto MDI/MDIX can reverse the pairs P12_TX+/P12_TX- and P12_RX+/P12_RX-.
99 98 96 97	P13_TX+ P13_TX- P13_RX+ P13_RX-	O O 	Port 13 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 13. Auto MDI/MDIX can reverse the pairs P13_TX+/P13_TX- and P13_RX+/P13_RX-.
101 102 104 103	P14_TX+ P14_TX- P14_RX+ P14_RX-	O O 	Port 14 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 14. Auto MDI/MDIX can reverse the pairs P14_TX+/P14_TX- and P14_RX+/P14_RX-.
111 110 108 109	P15_TX+ P15_TX- P15_RX+ P15_RX-	O O 	Port 15 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 15. Auto MDI/MDIX can reverse the pairs P15_TX+/P15_TX- and P15_RX+/P15_RX-.
113 114 116 115	P16_TX+ P16_TX- P16_RX+ P16_RX-	O O 	Port 16 Media Dependent Interface The differential data from the media is transmitted and received on two pairs for port 16. Auto MDI/MDIX can reverse the pairs P16_TX+/P16_TX- and P16_RX+/P16_RX-.

Pin No.	Label	Type	Description																				
11	P1_FXSD	I	<p>Port 1~ Port 16 fiber signal detect</p> <p>The Fiber Signal Detect input voltage level and behavior are as below table :</p> <table border="1"> <thead> <tr> <th>Voltage on Pxx_FXSD</th> <th>TP port</th> <th>Fiber port</th> <th>Fiber signal detect</th> <th>Condition</th> </tr> </thead> <tbody> <tr> <td>< 0.4V</td> <td>V</td> <td>--</td> <td>--</td> <td>TP mode</td> </tr> <tr> <td>> 1.2 V ; < 1.7 V</td> <td>--</td> <td>V</td> <td>Off</td> <td>Fiber mode / unlink</td> </tr> <tr> <td>> 1.95 V ; < 3.3 V</td> <td>--</td> <td>V</td> <td>On</td> <td>Fiber mode / link</td> </tr> </tbody> </table>	Voltage on Pxx_FXSD	TP port	Fiber port	Fiber signal detect	Condition	< 0.4V	V	--	--	TP mode	> 1.2 V ; < 1.7 V	--	V	Off	Fiber mode / unlink	> 1.95 V ; < 3.3 V	--	V	On	Fiber mode / link
Voltage on Pxx_FXSD	TP port			Fiber port	Fiber signal detect	Condition																	
< 0.4V	V			--	--	TP mode																	
> 1.2 V ; < 1.7 V	--			V	Off	Fiber mode / unlink																	
> 1.95 V ; < 3.3 V	--			V	On	Fiber mode / link																	
21	P2_FXSD																						
23	P3_FXSD																						
33	P4_FXSD																						
34	P5_FXSD																						
44	P6_FXSD																						
48	P7_FXSD																						
58	P8_FXSD																						
59	P9_FXSD																						
69	P10_FXSD																						
70	P11_FXSD																						
80	P12_FXSD																						
95	P13_FXSD																						
105	P14_FXSD																						
107	P15_FXSD																						
117	P16_FXSD																						

Table 3 RGMII Pin

Pin No.	Label	Type	Description
RGMII (port 17: PHY address 2; port 18: PHY address 3) Port 17 I/O configuration by Page C register 8 Port 18 I/O configuration by Page C register 9			
120 121 122 123 134 135 136 137	P17_TXD3 P17_TXD2 P17_TXD1 P17_TXD0 P18_TXD3 P18_TXD2 P18_TXD1 P18_TXD0	O	RGMII Transmit Data When it works in 10BASE-T or 100BASE-TX mode, TXD[3:0] present the transmit data at the rising edge of GTXCLK, and when it works in 1000BASE-T mode, TXD[3:0] present the low nibble of transmit data byte at the rising edge of GTXCLK, and present the high nibble of transmit data byte at the falling edge of GTXCLK.
119 133	P17_TXCTL P18_TXCTL	O	RGMII Transmit Enable RGMII transmit enable.
124 138	P17_GTXCLK P18_GTXCLK	O	RGMII Transmit Clock It is a 125MHz clock in 1000BASE-T mode, 25MHz clock in 100BASE-TX mode, or a 2.5MHz clock in 10BASE-T mode. IP1819I uses the clock to sample TXCTL and TXD [3:0].
126 127 128 129 140 141 142 143	P17_RXD3 P17_RXD2 P17_RXD1 P17_RXD0 P18_RXD3 P18_RXD2 P18_RXD1 P18_RXD0	I	RGMII Receive Data When the PHY works in 10BASE-T or 100BASE-TX mode, RXD[3:0] latch the receive data at the rising edge of RXCLK, and when it works in 1000BASE-T mode, RXD[3:0] latch the low nibble of receive data byte at the rising edge of RXCLK, and present the high nibble of transmit data byte at the falling edge of RXCLK.
130 144	P17_RXCTL P18_RXCTL	I	RGMII Receive Valid RGMII receive data valid.
125 139	P17_RXCLK P18_RXCLK	I/O	RGMII Receive Clock It is a 125 MHz, 25MHz, or 2.5MHz reference clock from a Gigabit PHY working in 1000BASE-T, 100BASE-TX or 10BASE-T.

Table 4 RGMII/MII Pin

Pin no.	Label	Type	Description
RGMII / MII (port 19: PHY address 1)			
166	P19_GTXCLK	O	RGMII Transmit Clock It is a 125MHz clock in 1000BASE-T mode, or a 25MHz clock in 100BASE-TX mode, or a 2.5 MHz clock in 10BASE-T mode. IP1819I uses the clock to sample TXCTL and TXD[3:0].
160	P19_TXCLK	I/O	MII Transmit Clock @ PHY mode, it's output; @ MAC mode, it's input (default) It is a 25MHz clock in 100BASE-TX mode, or a 2.5MHz clock in 10BASE-T mode. IP1819I uses the clock to sample TXER, TXEN and TXD[3:0].
161	P19_TXCTL (P19_TXEN)	O	RGMII/MII Transmit Enable Indicates the valid data is present on the data bus of TXD. It is synchronous to the rising edge of P19_GTXCLK (RGMII mode) or P19_TXCLK (MII mode). TXCTL is regarded as TXEN in MII mode.
162 163 164 165	P19_TXD3 P19_TXD2 P19_TXD1 P19_TXD0	O	RGMII/MII Transmit Data In RGMII mode, when it works in 10BASE-T or 100BASE-TX mode, TXD[3:0] present the transmit data at the rising edge of GTXCLK, and when it works in 1000BASE-T mode, TXD[3:0] present the low nibble of transmit data byte at the rising edge of GTXCLK, and present the high nibble of transmit data byte at the falling edge of GTXCLK. In MII mode, TXD[3:0] present the transmit data at the rising edge of TXCLK.
159	P19_TXER	O	MII Transmit Error MII transmit error in MII mode. A "high" state present on this pin indicates transmit data error. It is synchronous to TXCLK. It's recommended to pull low in RGMII mode.
169	P19_RXCLK	I	RGMII/MII Receive Clock. It is a 125 MHz, 25MHz, or 2.5MHz reference clock from a Gigabit PHY working in 1000BASE-T, 100BASE-TX, or 10BASE-T.
174	P19_RXCTL (P19_RXDV)	I	RGMII/MII Receive Valid Indicates the valid data is present on the data bus of P19_RXD. It is synchronous to the rising edge of P19_RXCLK. RXCTL is regarded as RXDV in MII mode.

Pin no.	Label	Type	Description
170 171 172 173	P19_RXD3 P19_RXD2 P19_RXD1 P19_RXD0	I	RGMI/MII Receive Data In RGMII mode, when the PHY works in 10BASE-T or 100BASE-TX mode, RXD[3:0] latch the receive data at the rising edge of RXCLK, and when it works in 1000BASE-T mode, RXD[3:0] latch the low nibble of receive data byte at the rising edge of RXCLK, and present the high nibble of transmit data byte at the falling edge of RXCLK. In MII mode, RXD[3:0] latch the receive data at the rising edge of RXCLK.
167	P19_RXER	I	MII Receive Error MII receive error in MII. A "high" state present on this pin indicates received data error. It is synchronous to RXCLK. It's recommended to pull low in RGMII mode.
146	MDC	O	Serial management bus clock output It's recommended to add a 30pF capacitor to ground for noise filtering.
145	MDIO	I/O	Serial management bus data input/output It's recommended to add a 1.5K ohm pull up resistor connecting to VDDIOR and a 30pF capacitor connecting to ground.

Table 5 EEPROM Pin

Pin No.	Label	Type	Description
176	EE_CLK	O	Serial EEPROM clock output
175	EE_DAT	I/O	Serial EEPROM data input/output

Table 6 CPU R/W Interface Pin

Pin No.	Label	Type	Description
151	CPU_CLK	I	Serial CPU access clock input
153	CPU_I/O	I/O	Serial CPU data input/output for 2 wire serial Write data in for 4-wire mode
154	CPU_O	O	Read data out for 4-wire mode
152	N_SS	I	Chip selection for 4-wire mode
155	CPU_INT	O	CPU Interrupt

Table 7 Serial LED Pin

Pin No.	Label	Type	Description
4	LED_CLK	O	Serial LED clock output LED clock rate setting by Page 3 register 0x17 bit[7:6] : 00 : 781 KHz 01 : 2.5 MHz 10 : 5.2 MHz 11 : 10.4 MHz (default)
5	LED_DAT	O	Serial LED data output

Table 8 IEEE-1588 PTP Pin

Pin No.	Label	Type	Description
157	1588_EVT	I	1588 Event Event trigger source input.
158	1588_PPS	O	1588 PPS Pulse per second reference output or clock/trigger output, refer to page 0x9 register 0x02.

Table 9 Miscellaneous Pin

Pin No.	Label	Type	Description
8	OSCI	I	Crystal/Oscillator 25MHz input
9	X2	O	Crystal output
10	RESETB	I	System reset (low active) Should be kept at "low" for at least 10 microseconds. The input voltage should be not higher than VDD33.
3	TEST_KEY	I	Auto Factory Test enable key input
1 2	MODE_0 MODE_1	I, PD	Test mode select 00: Normal (default) Reserved for test, should be "00" for normal operation.
46	BGRES	I	Bandgap This pin must be connected to ground through a 6.19K resistor.
84,86,89, 91,93,94,	NC		No connect

Power on Setting

The state of these pins will be latched upon reset.

Table 10 Power on Setting

Pin No.	Label / Setting	Type	Description
154	CPU_O/Home Vlan	IL, PU	Home Vlan 0 : Home VLAN on 1 : Home VLAN off Port 1 ~ port 18 are all individual VLAN and only send to CPU port. The setting can be updated by writing page 0x2 register 0x30~0x47, 0x58~0x63, 0x68 and 0x69.
4	LED_CLK/ LED_mode[2]	IL, PU	LED mode [2] 1 : 2-bit mono-color (Giga , Link/Act) (100 , Link/Act) 0 : 2-bit bi-color (operate at high speed: Giga , Link/Act) and 1-bit mono-color (operate at low speed: Link/Act) The setting can be updated by writing page 0x3 register 0x17[2].
5	LED_DAT/EEE	IL, PU	Polling PHY MMD register for EEE function 0: EEE disable 1: EEE enable The setting can be updated by writing page 0x3 register 0x2F[11:0] and 0x30[12][9:4].
123	P17_TXD0/ P19 force mode[0]	IL, PD	P19 force mode [0] (please refer to P19 force mode [1] and P19 force mode [2]) P19 force mode [2:0] 000 : P19 operation mode is not forced 001 : P19 operation mode is not forced 010 : 1000Mb/ Full 011 : reserved 100 : 100Mb / Full 101 : 100Mb / Half 110 : 10Mb / Full 111 : 10Mb / Half
122	P17_TXD1/ IPG compensation	IL, PD	IPG compensation 0: IPG compensation 40ppm 1: IPG compensation 160ppm The setting can be updated by writing page 0x0 register 0x1[1].
121	P17_TXD2/IGMP EN	IL, PD	IGMP enable 0: IGMP snooping disable 1: IGMP snooping enable The setting can be updated by writing page 0x1 register 0x29[0].
120	P17_TXD3/ Initial cable test	IL, PD	Initial cable test 0: Initial cable test disable 1: Initial cable test enable The setting can be updated by writing page 0x3 register 0x16[14].

Pin No.	Label / Setting	Type	Description
137	P18_TXD0/ LUT entry R/W method	IL, PD	LUT entry R/W method 0 : overwrite L1/L2 according to the aging time 1 : never overwrite before aging out The setting can be updated by writing page 0x1 register 0x2[0].
136	P18_TXD1/ LUT hashing	IL, PD	LUT hashing 0 : LUT CRC-hashing 1 : LUT direct -hashing The setting can be updated by writing page 0x1 register 0x2[3].
135	P18_TXD2/ Fiber mode[0]	IL, PD	Fiber mode[0] Fiber mode[1] 00/01 : {P1~P16} TP ports 10 : {P1~P8} TPports , {P9~P16} FB ports 11 : {P1~P16} FB ports The setting can be updated by writing page 0xC register 0xB[11:0] and 0xC[12][9:4].
134	P18_TXD3/ Fiber mode[1]		
165	P19_TXD0/ P19 force link	IL, PD	P19 force link 0: P19 force link disable 1: P19 force link enable The setting can be updated by writing page 0x3 register 0x12[0].
164	P19_TXD1/ P19 force mode [2]	IL, PD	P19 force mode [2]
163	P19_TXD2/ P19 force mode [1]	IL, PD	P19 force mode [1]
162	P19_TXD3/ Jumbo packet	IL, PD	Jumbo packet 0 : Jumbo packet disable 1 : Jumbo packet enable The setting can be updated by writing page 0x0 register 0x2[11:0] and 0x3[12][9:4].

Table 11 Power & Ground Pin

Pin No.	Label	Type	Description
6,81,82, 118,132, 156,168	DVDD10	P	1.08V power for core circuit
22,45, 90,106	AVDD10	P	1.08V power for analog circuit
148	REG_OUT	P	2.0V regulator output for RGMII I/O
147	VSS	P	Digital power ground for regulator
131	VDDIOR	P	2.0V/2.5V/3.3V input for port 17 ~ port 18 I/O PAD power
149	VDD33	P	3.3V power for digital circuit
7,150	VDDIOP	P	2.5V/3.3V input for EEPROM, CPU I/F, LED I/F, RESET and port 19 I/O PAD power
16,28,39, 47,53,64, 75,83,85, 87,88,92, 100,112	AVDD33	P	3.3V power for analog circuit
177	E-PAD GND	P	Digital power ground

I/O Power configuration refer Table 13

5 Function Description

5.1 Switch Engine and Queue Management

5.1.1 Packet forwarding

IP1819I utilizes the “store & forward” method to handle packet transfer. IP1819I begins to forward a packet to a destination port after the entire packet is received. A received packet will be forwarded to the destination port only if it is error free; otherwise, it will be discarded.

5.1.1.1 Address Learning and Hashing

Related registers	0x02[3:0], 0x03[11:0], 0x04[12][9:4]	PAGE 0x01
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IP1819I has 16384 entries for MAC address learning tables. It provides two hashing methods to access the MAC address table. One is the direct mapping and the other is the CRC algorithm. For the direct mapping method, if page 0x01 register 0x02[3] is set to “0”, the MAC address directly employs the least significant 13 bits of the MAC address. For the CRC algorithm method, if page 0x01 register 0x02[3] is set to “1”, IP1819I uses CRC algorithm to obtain 13bits MAC address from the 48-bits MAC.

The MAC address learning function can be either enabled or disabled for each port by programming page 0x01 register 0x03[11:0] and 0x04[12][9:4], and MAC address with all 0s can be learned to MAC address table by programming page 0x01 register 0x02[2] if the MAC address learning function is enabled.

IP1819I provides three kinds of methods for the MAC address learning. The first method is enabled by programming page 0x01 register 0x02[1:0] to “00”, means LUT can be written even when the entry is valid. The second method is enabled by programming page 0x01 register 0x02[1:0] to “01 or 10”, means LUT can not be written before aging out. The third method is enabled by programming page 0x01 register 0x02[1:0] to “11”, means only the second layer LUT can be written before aging out,.

The packet with the following conditions will not be learned in MAC address table.

- Erroneous packet
- 802.3x pause packet(option)
- 802.1D Reserved Group packet(option)
- Multicast source MAC address

IP1819I provides the MAC address learning count threshold function to limit source MAC address number learning in MAC address table. The number of learning MAC address must not be more than threshold, the extra MAC address will not be learnt in MAC address table if learning MAC address number higher than the threshold. The threshold values can be set by programming page 0x01 register 0x07[8:0] and each port is enabled individually by programming the corresponding bits of page 0x01 register 0x05[11:0] and 0x06[12][9:4].

5.1.1.2 Port Based Address Flush

Related registers	0x1A[11:0], 0x1B[13:12][9:4]	PAGE 0x01
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IP1819I can clear the MAC address that bind to specific port. The specific port can be enabled by programming the corresponding bits of page 0x01 register 0x1A[11:0] and 0x1B[12][9:4] to “1”, and trigger the port based address flush function by programming page 0x01 register 0x1B[13] to “1”.

5.1.1.3 Aging Time

Address Aging

Related registers	0x01[15], 0x01[14:0]	PAGE 0x01
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IP1819I supports programmable aging time to meet various system requirements, ranging from 55 sec to 1802295 sec $\pm 3.8\%$. The user can set aging time by programming page 0x01 register 0x01[14:0]. The address aging function can be also disabled by programming page 0x01 register 0x01[15] to “1”.

Packet Aging

Related registers	0x66[7:0], 0x67 to 0x6C, 0x71 to 0x73, 0x75	PAGE 0x08
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IP1819I supports packet aging (out queue aging). (If a packet stays in Queue too long, IP1819I will age out according to aging time defined in page 0x08 register 0x66[7:0]). IP1819I will drop the packet to improve the efficiency of packet buffer. The packet aging function can be enabled individually for each port by programming page 0x08 register 0x67 to 0x6C, 0x71 to 0x73 and 0x75.

5.1.1.4 802.1D packet forwarding

Related registers	0x06[15:0], 0x07[4:0]	PAGE 0x00
	0x03[0]	PAGE 0x0C

Except that the erroneous packet and the IEEE802.3x pause packet will not be forwarded, 802.1D Reserved Group packet with MAC address from 01-80-c2-00-00-00 to 01-80-c2-00-00-3F can be forwarded, dropped or “To CPU port” by programming page 0x00 register 0x06[15:0] and 0x07[3:0]. If the corresponding bits of page 0x00 register 0x06[15:0] and 0x07[3:0] are set to “11”, the 802.1D packets for each port will be dropped. Under this situation, if page 0x00 register 0x07[4] is also set to “1”, the 802.1D packet coming from CPU port can be forwarded.

Inter Frame Gap Compensation

Related registers	0x01[1:0]	PAGE 0x00
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IP1819I supports an option to transmit a packet with IPG shrank 40 ppm, 80 ppm or 160 ppm to compensation the data accumulation due to TX clock frequency difference between local machine and link partner. Programming page 0x00 register 0x01[1:0] can enable this function.

5.1.2 Flow Control

IP1819I supports two kinds of flow control mechanisms, backpressure for half duplex operation and IEEE 802.3x for full duplex operation.

5.1.2.1 IEEE802.3x

Related registers	0x08[11:0] to 0x0B[12][9:4]	PAGE 0x03
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When operating in full duplex mode, IP1819I supports IEEE802.3x flow control, both symmetric pause and asymmetric pause function. Each port's flow control function can be enabled individually by programming page 0x03 register 0x08[11:0] to 0x0B[12][9:4]. When the packets in buffer reach the threshold, IP1819I generates a "Xoff" pause packet immediately or right after the current packet has been transmitted. When receiving a pause packet, the link partner stops transmission for a period of time defined in the pause packet. This prevents the buffer of IP1819I from overrun. When the packets in buffer lower than threshold, IP1819I generates a "Xon" pause packet to notify the link partner the receive buffer is available.

5.1.2.2 Backpressure

Related registers	0x01[3:2]	PAGE 0x00
	0x0C[11:0], 0x0D[12][9:4]	PAGE 0x03

When operating in half duplex mode, IP1819I supports backpressure flow control. Each port's backpressure function can be enabled individually by programming page 0x03 register 0x0C[11:0] and 0x0D[12][9:4]. When the packets in buffer reach the threshold, IP1819I generates a jam pattern to back off the link partner. IP1819I supports the collision based and carrier-based backpressure. When the collision based backpressure is enabled, page 0x00 register 0x01[2] set to "1", IP1819I generates a jam pattern only when the link partner is transmitting data and the receive buffer in IP1819I is not available. When detecting a collision on line, the link partner stops transmission until a back off time expires. When the carrier based backpressure is enabled, page 0x00 register 0x01[2] set to "0", IP1819I transmits null packets continuously to prevent link partner's transmission when the buffer is not available.

To prevent the packet loss due to excessive collision caused by backpressure mechanism, user can program page 0x00 register 0x01[3] to "0" to disable the drop function due to 16 consecutive collisions defined in IEEE802.3.

5.1.2.3 Flow control auto off for high priority packet

Related registers	0x01[5]	PAGE 0x00
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To prevent the flow control function from blocking the high priority traffic, each port of IP1819I can auto turn off flow control function for a period of time automatically when receiving a high priority packet. This function can be enabled by programming page 0x00 register 0x01[5] to "1".

5.1.3 Bandwidth Control

Related registers	0x87 to 0x92, 0x9B to 0xA0, 0xA3 (Ingress)	PAGE 0x00
	0x85 to 0x90, 0x99 to 0x9E, 0xA1 (Egress), 0xB1[6:4]	PAGE 0x08

IP1819I implements a sophisticated data rate control mechanism, which is very useful for the bandwidth-limited network. By controlling both the ingress and the egress data rate, IP1819I provides a variety of bandwidth configurations. It limits the maximum byte counts in one second, for each port to send or receive packets. If the transmit byte counter or receive byte counter of a port reaches a pre-defined threshold, it will stop transmitting or receiving data in one second.

Each port's Ingress/egress data rate can be programmable individually. The bandwidth rate for port 1 to port 19 is defined in page 0x00 register 0x87 to 0x92, 0x9B to 0xA0 and 0xA3(Ingress) and page 0x08 register 0x85 to 0x90, 0x99 to 0x9E and 0xA1(Egress). The egress bandwidth parameter is defined in page 0x08 register 0xB1[6:4]. Note that its bandwidth should not be more than the link speed of a port.

5.1.4 Broadcast Storm Control

Related registers	0x0D[9:0] to 0x0F[12][9:4]	PAGE 0x01
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To prevent the broadcast storm, the IP1819I implements a broadcast storm control mechanism. By enabling this function, a port begins to drop the incoming broadcast packets if the number of received broadcast packets reach the threshold in selected period, which is defined in page 0x01 register 0x0D[7:0] and 0x0D[9:8]. Each port's broadcast storm protection function can be enabled individually by programming page 0x01 register 0x0E[11:0] and 0x0F[12][9:4]. IP1819I also provides four kinds of time period, which can be selected by programming page 0x01 register 0x0D[9:8] for 1G/100M/10M. The detailed configuration is shown in the following table.

5.1.4.1 Multicast and DLF Storm Control

Related registers	0x0D[9:0], 0x10[11:0] to 0x13[12][9:4]	PAGE 0x01
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Multicast storm and DLF storm use the same threshold setting defined in page 0x01 register 0x0D[7:0]. Multicast means the bit[40] of the destination MAC address is set to "1". DLF(Destination Lookup Failure) means the MAC address doesn't exist in MAC address table, is regarded as broadcast. multicast storm is configured by programming page 0x01 register 0x10[11:0] and 0x11[12][9:4] and DLF storm is configured by programming page 0x01 register 0x12[11:0] and 0x13[12][9:4].

5.1.4.2 ARP Storm Control

Related registers	0x14[9:0] to 0x16[12][9:4]	PAGE 0x01
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To prevent the ARP storm, IP1819I implements an ARP storm control mechanism. By enabling this function, a port begins to drop the incoming ARP packets if the number of received ARP packets reach the threshold in selected period, which is defined in page 0x01 register 0x14[7:0] and 0x14[9:8].

Each port's ARP storm protection function can be enabled individually by programming page 0x01 register 0x15[11:0] and 0x16[12][9:4]. IP1819I also provides four kinds of time period, which can be selected by programming page 0x01 register 0x14[9:8] for 1G/100M/10M. The detailed configuration is shown in the following table.

5.1.4.3 ICMP Storm Control

Related registers	0x17[9:0] to 0x19[12][9:4]	PAGE 0x01
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To prevent the ICMP storm, IP1819I implements an ICMP storm control mechanism. By enabling this function, a port begins to drop the incoming ICMP packets if the number of received ICMP packets reach the threshold in selected period, which is defined in page 0x01 register 0x17[7:0] and 0x17[9:8].

Each port's ICMP storm protection function can be enabled individually by programming page 0x01 register 0x18[11:0] and 0x19[12][9:4]. IP1819I also provides four kinds of time period, which can be selected by programming page 0x01 register 0x17[9:8] for 1G/100M/10M. The detailed configuration is shown in the following table.

Table 12 Broadcast /ARP/ICMP Storm Counter Clear Period Selection Table

0x0D[9:8] 0x14[9:8] 0x17[9:8]	1000Mbps	100Mbps	10Mbps
00	200us	2ms	20ms
01	1ms	10ms	100ms
10	10ms	10ms	10ms
11	100ms	100ms	100ms

5.1.5 Interface

5.1.5.1 MDI (port 1 ~ port 16)

IP1819I builds up 16 100M/10Mb internal PHYs, which individually connect with each TP port by TX/RX differential signals, ranging from port 1 to port 16.

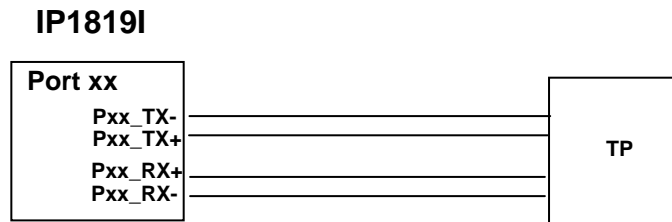


Figure 5 MDI Application diagram

5.1.5.2 RGMII(port 17 ~ port 19) / MII(port 19)

IP1819I sends out data TXD[3:0] and control signal TXCTL at the rising and falling edge of GTXCLK. Two GMII like signals TXEN and TXER are embedded in the TXCTL. GMII like information TXD[7:0] is embedded in the TXD[3:0]. By recognizing the decoded TXEN, TXD[7:0] and TXER, a PHY can capture the correct data stream.

A PHY sends out data RXD[3:0] and control signal RXCTL at the rising and falling edge of RXCLK. Two GMII like signals RXDV and RXER are embedded in the RXCTL. GMII like information RXD[7:0] is embedded in the RXD[3:0]. By recognizing the decoded RXDV, RXD[7:0] and RXER, IP1819I can capture the correct data stream. IP1819I samples the correct data at the rising edge of RXCLK.

To fit the timing requirement, the delay on GTXCLK and RXCLK can be adjusted by programming the bit[5:0] of page 0x0C register 0x08 to 0xA. The driving current can be also adjusted by programming the bit[8:6] of page 0x0C register 0x08 to 0xA.

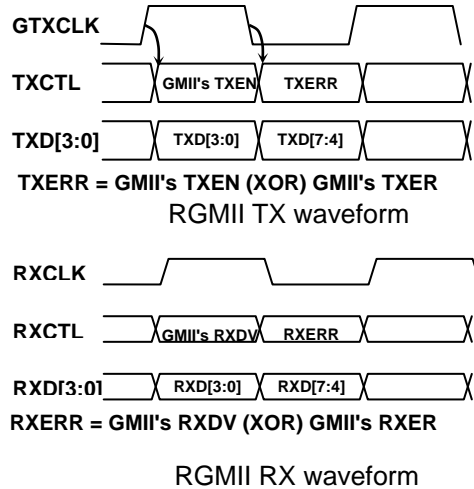


Figure 6 Waveform of RGMII

IP1819I's port 19 uses RGMII/MII interface to connect with external PHY

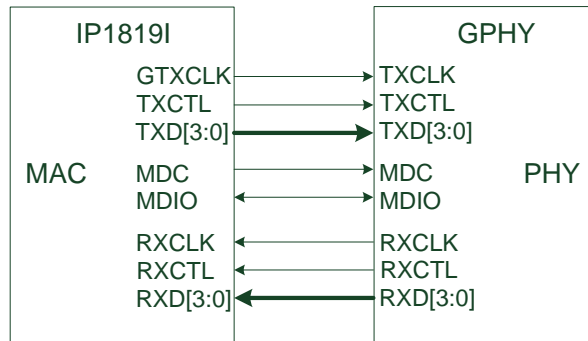


Figure 7 RGMII Application diagram

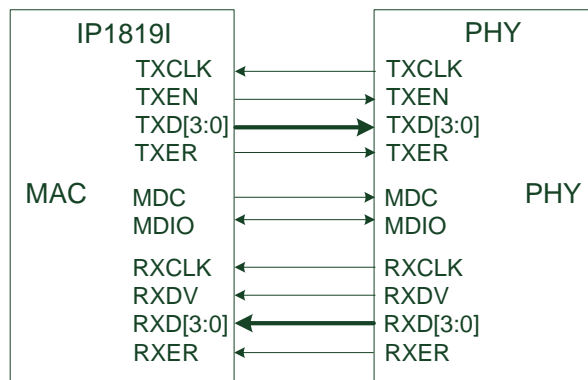


Figure 8 MII Application diagram

IP1819I's port 19 uses RGMII/MII interface to connect with external CPU.

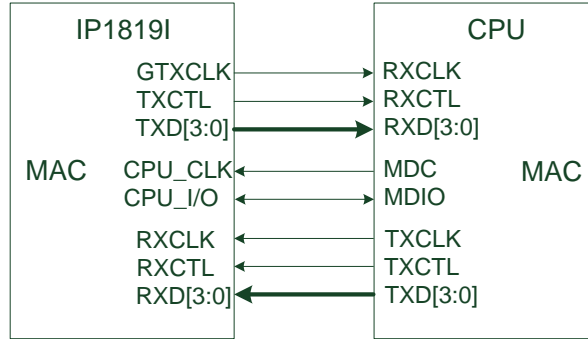


Figure 9 RGMII Application diagram

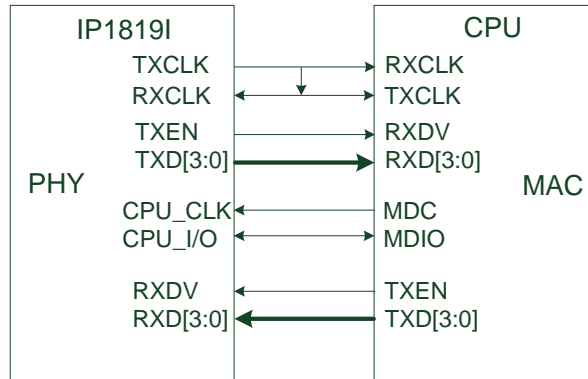


Figure 10 MII Application diagram

Table 13 I/O Power Configuration Table

Ports & I/O		Port 17 ~ port 18		Port 19		Other I/Os		
VDDIOR	VDDIOP	RGMII	SMI	RGMII	MII	CPUx	EEPROM	LEDx
2.0V	3.3V	2.0V	2.0V	3.3V	3.3V	3.3V	3.3V	3.3V
2.5V	3.3V	2.5V	2.5V	3.3V	3.3V	3.3V	3.3V	3.3V
2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V
3.3V	2.5V	3.3V	3.3V	2.5V	2.5V	2.5V	2.5V	2.5V
3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V

5.1.6 External CPU Read / Write interface

There is no need to program the register of the IP1819I for the generic application. However, it's probably necessary to program the internal register to fit some special applications. IP1819I supports two kinds of access interfaces, one is two wire interface, one is serial peripheral interface. The two interfaces between the IP1819I and the external CPU are all serial buses, which comprise a clock and an I/O signal for two serial interface and a clock and two separate I/O and SS signals for 4-wire. Like the access cycle of the serial management interface, the interface includes the serial interface comprising the switch ID, the read and write cycle, the address and the data. The access cycle is depicted as below.

The access cycle is much like the access cycle of MDC, MDIO. Care should be taken that the switch ID is 2-bit wide rather than 5-bit wide.

Besides, IP1819I also supports normal mode and fast mode for 2 wire and 4 wire application, the only difference between normal mode and fast mode, the "00" is followed by address in fast mode.

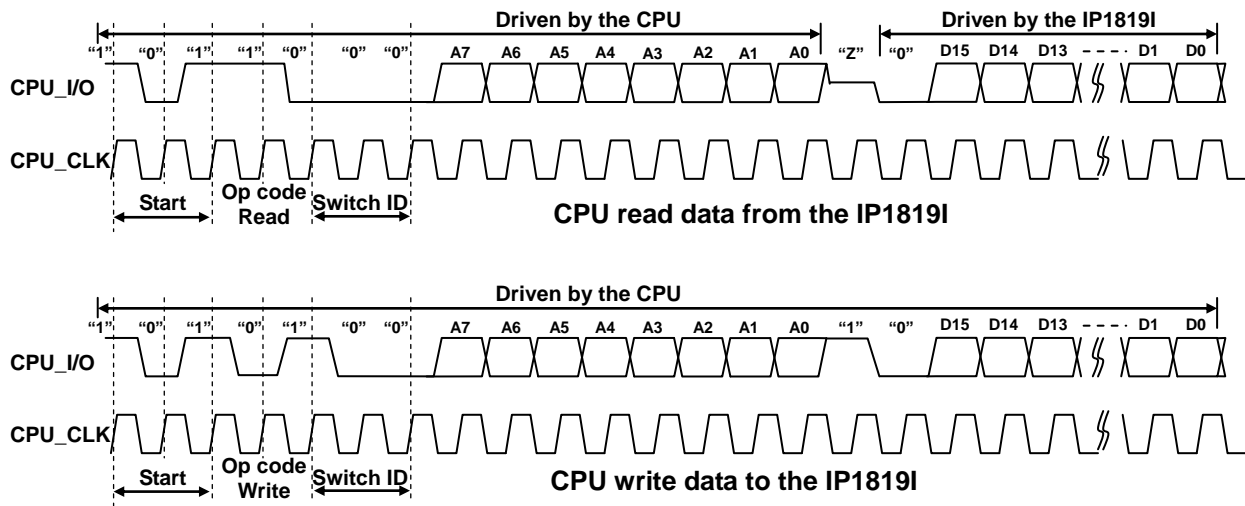


Figure 11 External CPU for 2 wire interface Read / Write diagram

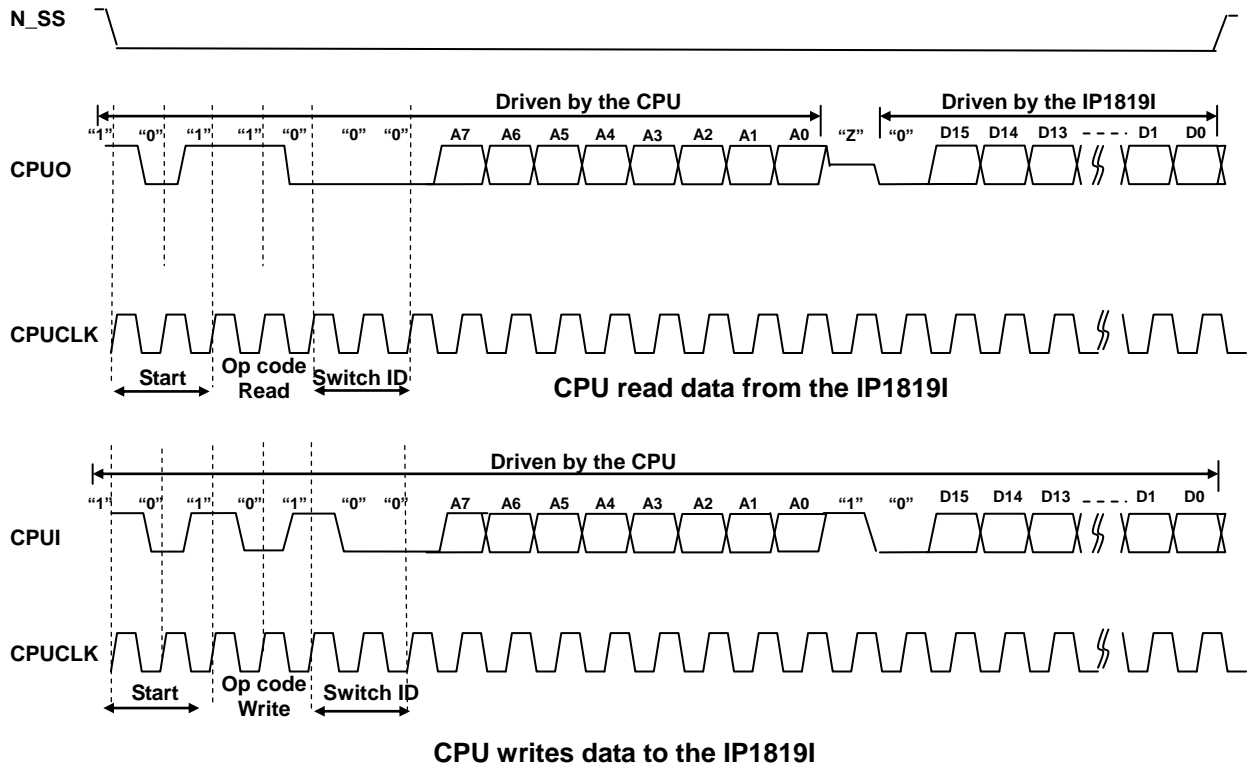


Figure 12 External CPU for 4-wire Read/Write Diagram

High speed mode

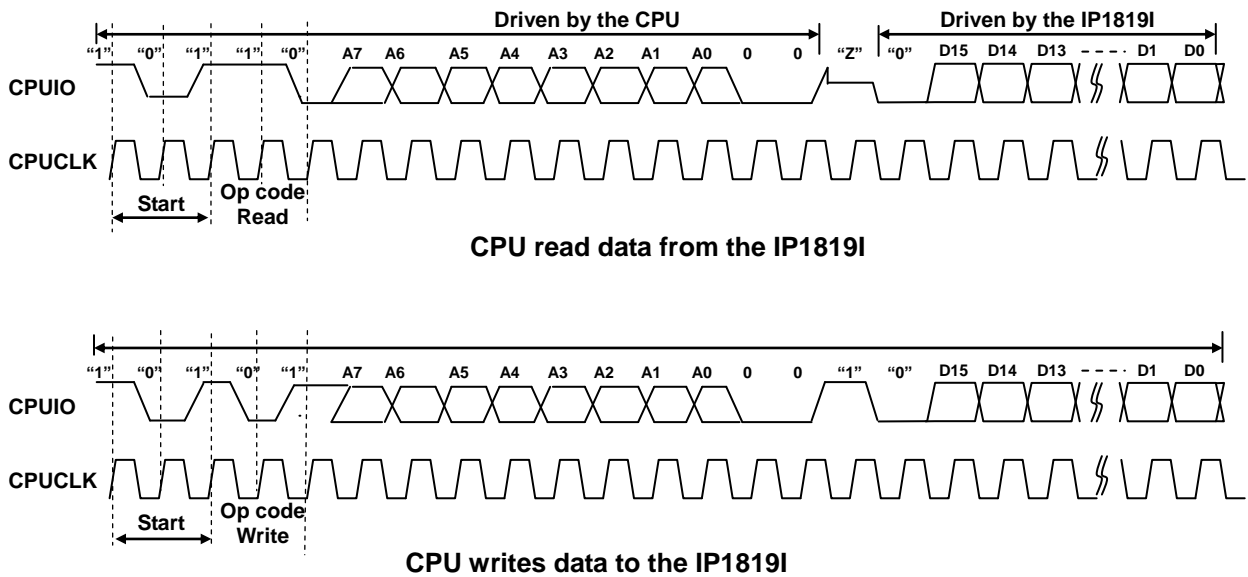


Figure 13 External CPU for high speed mode Read/Write Diagram

5.1.7 EEPROM Interface

Related registers	0x01 to 0x0F	PAGE 0x0B
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IP1819I supports EEPROM I/F to access 24C01 to 24C16. After detecting the rising edge of a reset input, IP1819I will start to read the content of EEPROM (acting like an EEPROM master). Being an EEPROM master, IP1819I provides command mode to download the content of EEPROM. The content of the first byte should be “00h” to be identified as IP1819I EEPROM. If the content of the second byte is “0Bh” for command mode of 24C01 to 24C16 EEPROM capacity.

In the command mode, one command occupies 4 EEPROM bytes. The content includes 1 bytes command and 1 bytes register address and 2 bytes data. If command byte < 0x40, it stands the register page address. If command byte >=0x40, it stands for the advance commands. (The detail explanation for advance commands please refer to advanced EEPROM application notes)

The following is a normal EEPROM example for IP1819I.

Table 14 Command Mode Format of EEPROM

Command mode		
EEPROM address	EEPROM content	Description
0x00	0x00	EEPROM start
0x01	0x0B	(EEPROM capacity at Command Mode)
0x02	0x00	Don't care
0x03	0x00	Don't care
0x04	0x03	Page address or advance Command In this case, page address is 0x03
0x05	0x0A	Register address In this case, register address is 0x0A
0x06	0x34	bit[15:8] Register data In this case, write 0x34 to register 0x0A[15:8]
0x07	0x12	bit[7:0] Register data In this case, write 0x12 to register 0x0A[7:0]
0x08	0xFF	Page address or advance Command
0x09	0xFF	Register address
0x0a	0xFF	bit[15:8] Register data
0x0b	0xFF	bit[7:0] Register data
0x0c	0xFF	Page address or advance Command
0x0d	0xFF	Register address
0x0e	0xFF	bit[15:8] Register data
0x0f	0xFF	bit[7:0] Register data
⋮		
XX	0xFF (or 0x00)	Page address or advance Command
XX	0xFF (or 0x00)	Register address
XX	(Do not care)	Stop Initial Reading (Follow by the command byte and register address are both 0xFF)
⋮	(Do not care)	

5.1.8 MIB Counter

Related registers	0x01[9], 0x64 to 0x66	PAGE 0x00
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IP1819I provides a set of RX and TX counters for statistic, IP1819I can monitor a variety of packets, including different length packet, illegal packet(over size, symbol error), unicast packet, multicast packet broadcast packet, and even byte count for packet, etc. To enable the counter, page 0x00 register 0x01[9] must set to "1". The user can read the content of the counter through page 0x00 register 0x64 to 0x66. The detailed description is shown in the following table.

Table 15 Address Format of Port MIB Counter

address	RX counter	TX counter
00	RX_64B	TX_64B
01	RX_65_127B	TX_65_127B
02	RX_128_255B	TX_128_255B
03	RX_256_511B	TX_256_511B
04	RX_512_1023B	TX_512_1023B
05	RX_1024_1518	TX_1024_1518
06	RX_Oversize	TX_Oversize
07	RX_Bcst	TX_Bcst
08	RX_Mcst	TX_Mcst
09	RX_Ucst	TX_Ucst
0A	RX_Pause	TX_Pause
0B	RX_Pkt	TX_Pkt
0C	Byte_L	Bytes_L
0D	Byte_H	Bytes_H
0E	RX_Drop (buff)	TX_Drop (buff)
0F	RX_DROP others	Single Col
10	RX_CRC	Multiple Col
11	RX_Alignment	Late Col
12	RX_Runt	Deferred TX
13	RX_Frag	Excessive Col
14	RX_Jabber	
15	Symbol Error	
16	ACL	
17	ACL	

5.1.9 Auto Factory Test (AFT)

IP1819I implements an AFT mechanism, which is very useful for switch pre-test. When this function is triggered by hardware pin 5 TEST_KEY, IP1819I's physical ports are connected either port-pairs LoopBack or self-LoopBack and then IP1819I will generator frames for TX of all ports .

In the AFT mode, the light-on period is within 1 second, then show the test result on the LED. The status of test result will keep the LED status while this hardware pin AFT is still triggered.

For example, port 1 and port 2 are connected to each other (LoopBack). Check the LED of port 1 and port 2 is light-on, and then trigger this AFT function. If the test result is passed (no CRC or packet loss), show LED of port 1 and port 2 light-on. Otherwise, show LED light-off when CRC or packet loss is happened.

5.1.10 LED display mode

Related registers	0X17 to 0X1F[12][9:4]	PAGE 0x03
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The bit stream is output sequentially through LED_DAT and LED_CLK and its sequence starts from port 19 to port 1. In the other word, port 1 LED status is present on the latest LED bit, as shown in the table. To store the serial LED stream, a serial-to-parallel shift register should be used.

Table 16 LED display behavior vs. LED mode

Pin Setting	0x17 bit[2:0]	LED mode	LED display behavior	
			Giga port	10/100M port
-	000	3-bit M	Giga-Spd, L/A, Dupx/Col	100-Spd, L/A, Dupx/Col
-	001	3-bit M	Giga-L/A, 100/10-L/A, Dupx/Col	100-L/A, 10-L/A, Dupx/Col
-	010	3-bit M	Giga-Spd, 100/10-Spd, /A	100-Spd, 10-Spd, /A
1	011	2-bit M	Giga-Spd, L/A	100-Spd, L/A
-	100	2-bit B, 1-bit M	Spd & L/A, PSE	Spd1 & L/A, PSE
-	101	2-bit M	L, /A	
-	110	2-bit B	Spd & L/A	Spd1 & L/A
0	111	2-bit B 1-bit M	Spd & L/A	L/A

(B : bi-color; M : mono-color)

(Spd & L/A : 1G & 100M/10M bi-color; Spd1 & L/A : 100M & 10M bi-color)

Table 17 LED display Sequence

0x17 bit[2:0]	LED mode	LED Display Sequence.
		[1], [2]..... indicate the bit stream sequence shifted from LED_DAT.
000	3-bit M	[1] port 19 Giga-Spd, [2] port 19 L/A, [3] port 19 Dupx/Col,, [55] port 1 100-Spd, [56] port 1 L/A, [57] port 1 Dupx/Col(last one)
001	3-bit M	[1] port 19 Giga-L/A, [2] port 19 100/10-L/A, [3] port 19 Dupx/Col,, [55] port 1 100-L/A, [56] port 1 10-L/A, [57] port 1 Dupx/Col(last one)
010	3-bit M	[1] port 19 Giga-Spd, [2] port 19 100/10-Spd, [3] port 19 Active,, [55] port 1 100-Spd, [56] port 1 10-Spd, [57] port 1 Active(last one)
011	2-bit M	[1] port 19 Giga-Spd, [2] port 19 L/A, [3] port 18 Giga-Spd, [4] port 18 L/A,, [37] port 1 100-Spd, [38] port 1 L/A(last one)
100	2-bit B, 1-bit M	[1][2] port 19 Spd & L/A, [3] port 19 PSE, [4][5] port 18 Spd & L/A, [6] port 18 PSE,, [55][56] port 1 Spd1 & L/A, [57] port 1 PSE(last one)
101	2-bit M	[1] port 19 Link, [2] port 19 Active, [3] port 18 Link, [4] port 18 Active,, [37] port 1 Link, [38] port 1 Active(last one)
110	2-bit B	[1][2] port 19 Spd & L/A, [3][4] port 18 Spd & L/A,, [37][38] port 1 Spd1 & L/A(last one)
111	2-bit B 1-bit M	[1][2] port 19 Spd & L/A, [5][6] port 17 Spd & L/A, [7] port 16 L/A,, [22]port 1 L/A(last one)

IP1819I also provides CPU control LED mode, if page 0x03 register 0x17[15] is asserted, then LED will show results according to the settings of page 0x03 register 0x1A[11:0] to 0x1F[12][9:4]. More detail description, please refer to the LED application note.

Bi-color description



An example for port 1 ~ port 18 using 2-bit stream mono-color LED display mode with IP403 is shown below.

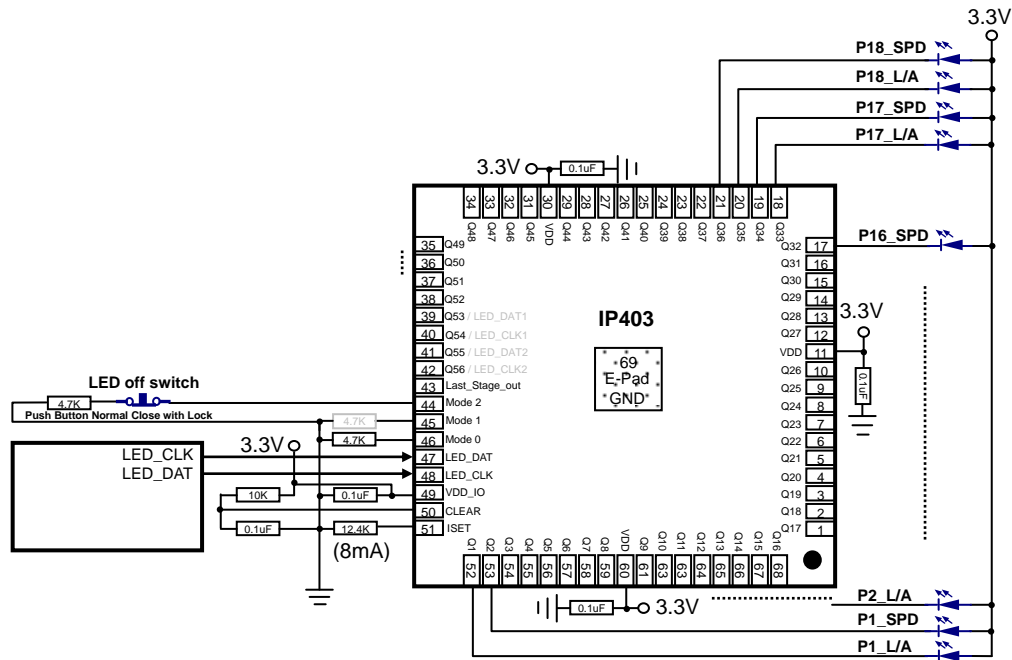


Figure 14 2-bit stream mono-color LED application diagram

5.2 VLAN

IP1819I supports port based VLAN, tag based VLAN and protocol based VLAN to implement flexible VLAN function, the detailed description is as follows.

5.2.1 Port Based VLAN

Related registers	0x30[11:0] to 0x47[12][9:4], 0x58[11:0] to 0x63[12][9:4], 0x68[11:0], 0x69[12][9:4]	PAGE 0x02
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IP1819I provides port-based VLAN configurations. For each port, there are two registers to describe its port-based VLAN configuration. The VLAN group can be defined in page 0x02 registers 0x30[11:0] to 0x47[12][9:4], 0x58[11:0] to 0x63[12][9:4], 0x68[11:0] and 0x69[12][9:4].

Take the following example for the detail description. The data incoming from port 1 can be forwarded to the corresponding port defined in page 0x02 register 0x30 and 0x31. For example, if page 0x02 register 0x30 is written with 16'h000F, the packet from port 1 can be forwarded to port 2/3/4 only. Similarly, the forwarding rule for the data incoming from port 2 will refer to page 0x02 register 0x32 and 0x33. The forwarding rule for the data incoming from port 19 will refer to page 0x02 register 0x68 and 0x69.

5.2.2 Tag Based VLAN

Related registers	0x06[1], 0x09[11:0], 0x0A[12][9:4], 0x13 to 0x1E, 0x27 to 0x2C, 0x2F, 0xD2 to 0xD8	PAGE 0x02
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IP1819I provides 4096 VLAN entries in VLAN table, the user can configure the VLAN table by programming page 0x02 register 0xD2 to 0xD8. If tag VLAN function is enabled and IP1819I receive a tagged packet, IP1819I will use the VID to lookup the VLAN entry in the VLAN table. If it is invalid, IP1819I drops the packet. If it is valid, IP1819I will forward the packet to destination port which belongs to the members of the VLAN, if this destination port is not a VLAN members, the packet will be dropped. Besides, If the source port is not a member of the VLAN, the packet can be either forwarded or dropped by programming page 0x02 register 0x09[11:0] and 0x0A[12][9:4].

When an un-tagged packet is received, IP1819I uses the PVID of the source port to look up the VLAN entry from VLAN table, the default PVID of the ports are defined in page 0x02 register 0x13 to 0x1E, 0x27 to 0x2C and 0x2F. IP1819I forwards the packet in the same way as mentioned above. For example, if port 1 receives a un-tag packet, IP1819I adopts the PVID of port 1 defined in bit[11:0] of page 0x02 register 0x13 to search the VLAN table, if the VLAN entry is valid, the packet will be forwarded to destination port which belongs to the members of the VLAN, the behavior of priority tag packet (VID equals to "000h") is the same as an un-tagged packet.

5.2.3 Protocol Based VLAN

Related registers	0x06[0], 0x6A to 0x71	PAGE 0x02
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IP1819I can configure a list of protocol types (Ether type, LLC,RFC1042) mapping to VLAN membership by programming page 0x02 register 0x06[0] and page 0x02 register 0x6A to 0x71. IP1819I provides 4 entries for the protocol based VLAN to use, each entry primarily consists of "type for protocol" and "protocol selection" settings.

IP1819I will check whether an incoming packet matches in “protocol selection” and “type for protocol” settings in corresponding register. For example, if the incoming packet format matches page 0x02 register 0x6A and 0x6B (entry 01), the VLAN membership refers to the VID of specific protocol type. (Note that the VID won’t be added to output port, IP1819I only use to the VID to look up the VLAN member for the packets forwarding.

When protocol selection is invalid, the default VLAN membership refers to PVID index.

Table 18 PVID index search VLAN table

Protocol selection	Ingress packet	According to VID index	According to PVID index
Invalid	Ether type	---	By PVID
	LLC	---	By PVID
	RFC1042	---	By PVID
Ether Type	Ether type	By VID	---
	LLC	---	By PVID
	RFC1042	---	By PVID
LLC	Ether type	---	By PVID
	LLC	By VID	---
	RFC1042	---	By PVID
RFC1042	Ether type	---	By PVID
	LLC	---	By PVID
	RFC1042	By VID	---

5.2.4 VLAN Function

Related registers	0x06, 0x13 to 0x1E, 0x27 to 0x2C, 0x2F, 0xCC[11:0] to 0xCF[12][9:4], 0xD2 to 0xD8	PAGE 0x02
	0x07[11:0], 0x08[12][9:4]	PAGE 0x07
	0x03[0]	PAGE 0x0C

5.2.4.1 Add/modify VLAN Tag

IP1819I provides two methods for adding VLAN tag. One is port-based tagging, and the other is VID-based tagging. For port-based tagging, if the corresponding bits of page 0x02 register 0xCC[11:0], 0xCD[12][9:4] are set to “1” and page 0x02 register 0x06[1] is set to “1”, the packet will be added tag. For VID-based tagging, if the corresponding bits of “add tag field” of the VLAN entry are set to “1” and page 0x02 register 0x6[3] is set to “1” and page 0x02 register 0x06[1] is set to “1”, the packet will be added tag.

5.2.4.2 Remove VLAN Tag

IP1819I also provides two methods for removing VLAN tag. One is port-based, and the other is VID-based. For port-based, if the corresponding bits of page 0x02 register 0xCE[11:0], 0xCF[12][9:4] are set to “1” and page 0x02 register 0x06[1] is set to “1”, the packet will be stripped tag. For VID-based, if the corresponding bits of “remove tag field” of the VLAN entry are set to “1” and page 0x02 register 0x6[3] is set to “1” and page 0x02 register 0x06[1] is set to “1”, the packet will be stripped tag”.

Besides, if page 0x02 register 0x06[4] is set to “0” and page 0x0C register 0x03[0] is set to “1”, the packets that send to CPU Port will not add or remove tag. The operation is illustrated as follows. It is note that the VID-based tagging defined in the VLAN entry table is also used for 802.1Q tag-based VLAN.

Table 19 Forward the Packet with VLAN Configuration Table

Frame type of the received packet	The operation on a switch with VLAN configuration	
	Forward to a untagged field	Forward to a tagged field
Untagged	Forward the packet without modification	<ol style="list-style-type: none"> 1. Insert a tag using the default VLAN tag value of the source or output port 2. Calculate new CRC 3. The default VLAN tag value will be added to output port by writing register 0xCC[11:0] and 0xCD[12][9:4].
Priority-tagged (VLAN ID=0)	<ol style="list-style-type: none"> 1. Strip tag 2. Calculate new CRC 	<ol style="list-style-type: none"> 1. Keep priority field. 2. Replace the tag with the default VLAN tag value of the source or output port 3. Calculate new CRC 4. The default VLAN tag value is defined in the registers bit[11:0] in the 0x13 to 0x1E, 0x27 to 0x2C and 0x2F.
VLAN-tagged	<ol style="list-style-type: none"> 1. Strip tag 2. Calculate new CRC 	Forward the packet without modification

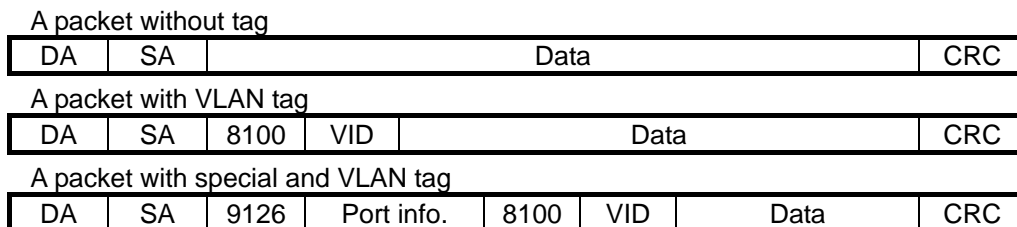


Figure 15 Frame Format of Inserting VLAN or/and Special Tag

5.2.4.3 VLAN up Link

Related registers	0xD0[11:0], 0xD1[12][9:4]	PAGE 0x02
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When source port forwards packet to destination port in different VLAN group. For example, source port is in VLAN1, destination port is in VLAN2, and the packet will be sent to “uplink port” in VLAN1 if uplink port function is enabled, When source port forwards packet to destination port in different VLAN group, the packet will be dropped if uplink port function is disabled. Uplink port function is enabled by programming page 0x02 register 0xD1[13] to “1”, uplink port is configured by programming the corresponding bits of page 0x02 register 0xD0[11:0] and 0xD1[12][9:4].

5.2.4.4 Force the Incoming Packet Use PVID

Related registers	0x13[15] to 0x1E[15], 0x27[15] to 0x2C[15], 0x2F[15]	PAGE 0x02
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IP1819I provides a kind of the mechanism for VLAN packets forwarding. If the bit[15] of page 0x02 register 0x13 to 0x1E, 0x27 to 0x2C and 0x2F is set to “1” for each port, IP1819I will use PVID for VLAN checking instead of VID for VLAN checking, that is, IP1819I will use PVID to lookup VLAN member for the packets forwarding. The function can be enabled individually for each port by programming each bit[15] from page 0x02 register 0x13 to 0x1E, 0x27 to 0x2C and 0x2F.

5.2.4.5 VLAN Ingress Check

Related registers	0x09[11:0] to 0x0E[9:8][3:0]	PAGE 0x02
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For packets forwarding, IP1819I provides two kinds of mechanism for the VLAN ingress check.

1. By port, IP1819I will check whether the source port of incoming packet belong to the same VLAN group by setting page 0x02 register 0x09[11:0] and 0x0A[12][9:4] to "1". If the ingress port is not in VLAN membership, IP1819I will drop it.
2. By frame type, IP1819I will decide which type of the incoming packets should be forwarded by programming the corresponding bits of page 0x02 register 0x0B[15:0], 0xC[7:0], 0xD[15:8] and 0x0E[9:8][3:0], 2 bits for each port, which is represented in as follows, 00: "all packet are forwarded", 01: "only tag packet is forwarded", 10: "priority and non-tag packet are forwarded", 11: "priority and tag packet are forwarded".

5.2.4.6 VLAN Egress Rule

Related registers	0x0F[11:0], 0x10[15:13][12][9:4]	PAGE 0x02
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For egress rule, IP1819I implements a set of VLAN egress rules, which defined port based, unicast, multicast and ARP. If an incoming packet matches specific rule. For example, if page 0x02 register 0x10[15] is set to "1", the ARP packet will use the default group setting for forwarding.

5.2.4.7 VLAN Exclusive port

Related registers	0xCA[11:0] to 0xCB[12][9:4]	PAGE 0x02
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In order to provide flexible network management, IP1819I provides the VLAN exclusive port function which can block any packet for each exclusive port. However, exclusive port can communicate with non exclusive port. For example, if page 0x02 register 0xCA is set to 0x03, port 1 and port 2 can not receive packet from each other, but port 3 can receive packet from both port 1 and port 2.

5.2.4.8 Inactive VID redirect

Related registers	0x6[15][14:10][1]	PAGE 0x02
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The inactive VID means the specific VLAN field in the VLAN entry is set to 1'b0. If a packet refers to inactive VID, the packet will be dropped. However, IP1819I can also redirect the packet to specific port, broadcast or drop it. For example, if bit[15] and bit[14:10] of page 0x02 register 0x06 are separately set "1" and "00000", IP1819I will force the packet to port 1.

5.3 Class Of Service (CoS)

5.3.1 Output Queue Schedule Mode with Priority

Related registers	0x01 to 0x2B, 0x3C to 0x47, 0x4C, 0x4D, 0x76 to 0x84	PAGE 0x08
	0x01[5]	PAGE 0x00

IP1819I implements eight levels of priority queues (priority queue 0 to 7). The priority for each packet is based on the following schemes:

1. Port based
2. 802.1Q tag
3. IP TOS/DSCP
4. TCP Flag
5. TCP/UDP port number
6. Supreme priority (including ACL, IP address, source MAC address)

When CoS function is enabled, the following seven scheduling modes can be selectable. If CoS function is not enabled, the first-in/first-out (FIFO) forwarding method will be used to forward packets. The detailed configuration is shown in the following table. For the WRR scheduling mode, which is defined in page 0x08 register 0x01, the order of transmitting packet is sent out from high to low priority queue, Q7 is the highest queue, Q0 is the lowest queue.

Out queue schedule function also can be set for port group A and port group B. The default is group A. If bit[9] of page 0x08 register 0x76 is set to "1", out queue schedule mode for group B also is enabled. In this condition, group A and group B can individually run their own out queue schedule mode simultaneously.

Table 20 Output Queue Schedule Mode Description Table

Reg 0x01[2:0]	Schedule Mode	Function description
00	FIFO Schedule	All output packets are queued to queue 0, first comes first outs.
01	WRR/WFQ/BW/TWRR	Queue method is selected by setting page 0x8 register 0x01[6:5]
02	SPx1+WRR/WFQ/BW/TWRRx7	Mixed mode, Q7 is SP , queue6~0 are WRR/WFQ/BW/TWRR.
03	SPx2+WRR/WFQ/BW/TWRRx6	Mixed mode, Q7 and Q6 are SP , queue5~0 are WRR/WFQ/BW/TWRR.
04	SPx4+WRR/WFQ/BW/TWRRx4	Mixed mode, Q7~Q4 are SP , queue3~0 are WRR/WFQ/BW/TWRR.
05	SPx8	unless the high priority queue is empty, otherwise, low priority cannot transmit packets.
06	LLQx1+WFQ/BW/TWRRx7	Mixed mode, Q7 is LLQ , queue6~0 are WFQ/BW/TWRR.
07	LLQx2+WFQ/BW/TWRRx6	Mixed mode, Q7 and Q6 are LLQ , queue5~0 are WFQ/BW/TWRR.

Note: FIFO(First In First Out), WRR(Weighted Round Robin), WFQ(Weighted Fair Queue), BW(Bandwidth), TWRR(Timing Weighted Round Robin), SP(Strict Priority), LLQ(Low Latency Queue).

IP1819I provides privilege priority to decide which priority of packet should be used. When these priorities are set to the packet of certain port, the order of the privilege priority is ACL > PTP > IGMP > IP address > MAC (LUT) > VID priority > TCP/UDP port number based priority > TCP flag > IP CoS based priority > VLAN tag based priority > port based priority.

IP1819I provides an option to suspend flow control function avoiding the extra delay for a high priority packet. A port's flow control function will be suspended for 1.5sec automatically when IP1819I receives a high priority packet. This function can be enabled by programming page 0x00 register 0x01[5] to "1".

Besides, IP1819I also supports SBM(static bandwidth management) and DBM(dynamic bandwidth management) mechanism to facilitate the use of out queue buffer, SBM and DBM is set for per port, means some port can be configured as either SBM or DBM.

5.3.2 Port Based Priority

Related registers	0x3A[14:0] to 0x3C[5:0], 0x3E[14:0], 0x3F[11:9][2:0]	PAGE 0x00
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The port-based priority only concerns the physical port location corresponding to switch. A packet received is regarded as the high priority packet from the high priority port. Each port of IP1819I can be configured as a high priority port individually by programming page 0x00 register 0x3A[14:0] to 0x3C[5:0], 0x3E[14:0] and 0x3F[11:9][2:0]. For example, page 0x00 register 0x3A[2:0] is corresponding to port 1.

5.3.3 802.1Q VLAN Tag Based Priority

Related registers	0x40[11:0], 0x41[14][12][9:4]	PAGE 0x00
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When the 802.1Q VLAN tag-based priority is enabled, the 802.1Q tag priority edition can be selected by programming page 0x00 register 0x41[14]. It will examine 3 bits of the priority field carried by a VLAN tag and map it to the corresponding priority. The priority mapping is shown in the following table. The 802.1Q tag-based priority function for each port can be enabled individually by programming page 0x00 register 0x40[11:0] and 0x41[12][9:4].

Priority field	Queue0	Queue1	Queue2	Queue3	Queue4	Queue5	Queue6	Queue7
First Ver.	2	0	1	3	4	5	6	7
Second Ver.	1	0	2	3	4	5	6	7

5.3.4 IP ToS/ DSCP CoS Based Priority

Related registers	0x42[11:0], 0x43[12][9:4] to 0x49	PAGE 0x00
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IP1819I provides the IP layer CoS function by recognizing the priority octet and mapping it to the corresponding priority. For an IPv4 packet, it is embedded in the ToS (Type of Service) Octet. For an IPv6 data packet, the Traffic Class Octet is used to differentiate the Class of Service. When this function is enabled, IP1819I will automatically recognize the IP version and capture either the TOS field (IPv4) or the Differentiated Services field (IPv6).

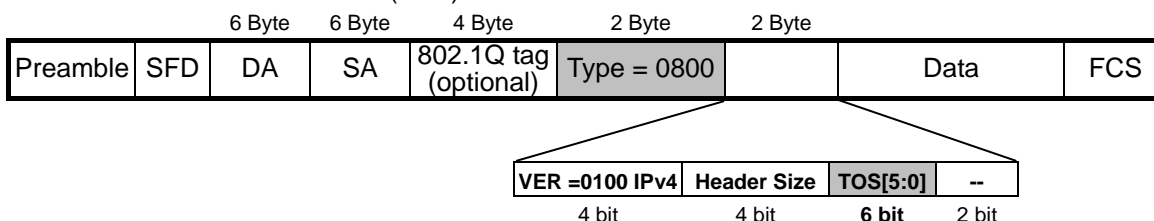


Figure 16 Frame Format of IPv4 TOS

The eight bits were allocated to a TOS field in the IP header. They can be divided into 5 sub fields:

0	1	2	3	4	5	6	7
Precedence			D	T	R	Unused	

0=Most Significant bit : 7 = Least Significant bit.

The value of the 3 precedence bits are from 0 to 7 and are used to indicate the importance of a datagram (default is 000, higher is better).

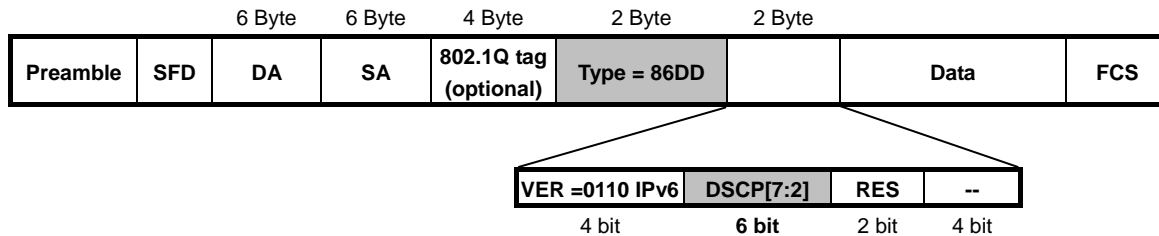


Figure 17 Frame Format of IPv6 DSCP

The IP TOS/DS priority function can be enabled individually for each port by programming page 0x00 register 0x42[11:0], and 0x43[12][9:4], and user can define IP TOS/DS priority setting for seven kinds of code point. If IP1819I receives a packet with IP TOS/DS code point, which is not defined in corresponding register, IP1819I provides two kinds of methods to handle undefined code point for the packet. One is the zero priority method, the packet will be treated as a lowest priority packet by programming page 0x00 register 0x45[9] to “0”. The other is the Tag/Port based method, and the packet will be assigned a priority according to its priority setting on tag/port by programming page 0x00 register 0x45[9] to “1”.

5.3.5 TCP/UDP Port Number Based Priority

Related registers	0x0A to 0x1C[12][9:4]	PAGE 0x00
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When the TCP/UDP port number function is enabled, IP1819I will examine the TCP/UDP destination port number of the packet to decide its priority.

The user can define the priority for TCP/UDP packets by programming the corresponding bits of page 0x00 register 0x12 to 0x16. For example, that a packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a highest priority packet if page 0x00 register 0x12[3:0] is set as 4b’0111(Q7). That a packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a lowest priority packet if page 0x00 register 0x12[3:0] is set as 4b’0000.(Q0)

A packet with TCP/UDP port number matches the user-defined port number, which is defined in page 0x00 register 0x0A to 0x11, the packet will be treated as a priority packet depending on the setting in page 0x00 register 0x15[15:12] and 0x16[15:0]. IP1819I provides three groups for user-define port number range. For example, if port number group C is set to “highest priority” by programming page 0x00 register 0x16[7:4], and the range of port number is set from 100 to 1 by programming page 0x00 register 0x0C and 0x0D, the incoming packet(port number=10) will be forwarded to highest priority queue. The TCP/UDP port number based priority function of each port can be enabled individually by programming page 0x00 register 0x1B[11:0] and 0x1C[12][9:4].

For the setting of TCP/UDP port number, user-defined range setting will override the setting of page 0x00 register 0x12 to 0x15. For example, if the priority of FTP (20, 21) is set to low and the priority of the port number (1~21) is set to high for user-defined range setting, the priority of port number (20, 21) will be treated as high priority rather than low priority.

Table 21 TCP/UDP Port Number priority Selection Table

Register (PAGE 0)		Port number	Definition
FTP	0x12[3:0]	20,21	0000: Queue 0 0001: Queue 1 0010: Queue 2 0011: Queue 3 0100: Queue 4 0101: Queue 5 0110: Queue 6 0111: Queue 7
SSH	0x12[7:4]	22	
TELNET	0x12[11:8]	23	
SMTP	0x12[15:12]	25	
DNS	0x13[3:0]	53	
BOOTP/DHCP	0x13[7:4]	67,68	
TFTP	0x13[11:8]	69	
HTTP_0,1	0x13[15:12]	80	
POP3	0x14[3:0]	110	
NEWS	0x14[7:4]	119	
SNTP	0x14[11:8]	123	
NETBIOS0,1,2	0x14[15:12]	137~139	
IMAP_0,1	0x15[3:0]	143,220	
SNMP_0,1	0x15[7:4]	161,162	
HTTPS	0x15[11:8]	443	
USR A	0x15[15:12]	User define A	
USR B	0x16[3:0]	User define B	
USR C	0x16[7:4]	User define C	
USR D	0x16[11:8]	User define D	
USR E	0x16[15:12]	User define E	

5.3.6 Source MAC address Priority

Related registers	0x02[3], 0xE0 to 0xE5	PAGE 0x01
	0x4A[11:0], 0x4B[12][9:4]	PAGE 0x00

IP1819I has an option to support the Source MAC Address based Priority. IP1819I will check the corresponding bits of the LUT entry to decide the priority of the packet if source MAC address priority function is enabled, the LUT table can be configured by programming page 0x01 register 0xE0 to 0xE5. The MAC address priority function can be enabled individually for each port by programming the corresponding bits of page 0x00 register 0x4A[11:0] and 0x4B[12][9:4].

5.3.7 VID Based VLAN Priority

Related registers	0x4C[11:0], 0x4D[12][9:4]	PAGE 0x00
	0x06[1], 0xD2 to 0xD8	PAGE 0x02

IP1819I has an option to support VID based priority. This function can be enabled individually for each port by programming the corresponding bits of page 0x00 register 0x4C[11:0] and 0x4D[12][9:4]. IP1819I will recognize the VID of incoming packets, and then check VLAN Table to find out corresponding priority setting. Each VID priority field of VLAN Table can be configured individually by programming page 0x02 register 0xD2 to 0xD8. If priority Field in VLAN entry is set to “111”, means highest queue, If priority Field in VLAN entry is set to “000”, means lowest queue.

5.3.8 IP address Priority

Related registers	0x4E[11:0], 0x4F[12][9:4]	PAGE 0x00
	0x2F to 0x3A	PAGE 0x01
	0x02[15]	PAGE 0x02

IP1819I has an option to support the source IP address priority. If the function is enabled, IP1819I will look up the IP entry from IP table to decide its priority. IP table can be configured by programming page 0x01 register 0x2F to 0x3A. For example, if the PRI field of IP entry is set to “1111”, the IP packet will be forward to highest priority queue. If the PRI field of IP entry is set to “1000”, the IP packet will be forward to lowest priority queue. IP address priority function is enabled individually for each port by programming the corresponding bits of page 0x00 register 0x4E[11:0] and 0x4F[12][9:4] to “1”. The Hashing algorithm for IP address can be set either CRC or direct method by programming page 0x02 register 0x02[15].

5.3.9 IP multicast Priority

Related registers	0x2F to 0x39	PAGE 0x01
	0x50[11:0] 0x51[12][9:4]	PAGE 0x00

IP1819I has an option to support IP multicast priority. IP multicast priority function can be enable individually for each port by programming the corresponding bits of page 0x00 register 0x50[11:0] and 0x51[12][9:4]. The user can set the priority for the IP multicast entry by programming page 0x01 register 0x2F to 0x39, the packet will be forward to out queue by programming PRI field of IP multicast table.

5.3.10 ACL Priority

Related registers	0x52[11:0] 0x53[12][9:4]	PAGE 0x00
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The ACL function also has an action for priority assignment. User can set the priority for the ACL rule. The ACL priority function can be enable individually for each port by programming the corresponding bits of page 0x00 register 0x52[11:0] and 0x53[12][9:4]. The packet will be forward to out queue by ACL action if it matches ACL rule.

5.4 Capture Ethernet protocol frame & IP packet to CPU port

5.4.1 In Band Management Frame

Related registers	0x01[6], 0x5C to 0x5E, 0x21, 0x22	PAGE 0x00
	0x03[0]	PAGE 0x0C

IP1819I's default MAC address is 00-90-c3-00-00-03. If the DA of an incoming packet matches IP1819I's MAC address, it will be sent to the CPU port if page 0x00 register 0x01[6] is set to "1" and page 0x0C register 0x03[0] is set to "1". IP1819I's MAC address can be changed by programming page 0x00 register 0x5C to 0x5E.

IP1819I also provides in-band management restriction function. By checking the content of the related packet to decide the packet should be forwarded or dropped. For example, If page 0x00 register 0x01[6] is set to "1" and page 0x00 register 0x22[15] is set to "1", and the DA of the packet meets to the switch MAC address, IP1819I will forward or drop the packet, according to the corresponding bits of page 0x00 register 0x21[15:0] and page 0x00 register 0x22[14:0], if the corresponding bit is set to "1", the packet will be forwarded, otherwise, the packet will be dropped.

5.4.2 Block Broadcast Frames to CPU Port

Related registers	0x0D[11:10]	PAGE 0x01
	0x03[0]	PAGE 0x0C

In order to prevent broadcast packets to impact the performance of CPU port, IP1819I can drop broadcast and multicast frames to CPU port if page 0x01 register 0x0D[10] is set to "1" and page 0x0C 0x03[0] is set to "1", IP1819I also can only forward IPv4 /IPv6 broadcast and multicast frames to CPU port if page 0x01 register 0x0D[11] is set to "1" for specific application for CPU.

5.4.3 ARP and ICMP Storm Control

Related registers	0x14 to 0x19[12][9:4]	PAGE 0x01
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In order to prevent the ARP and ICMP storm to affect the performance of IP1819I, IP1819I implements ARP and ICMP storm control mechanism to drop excessive ARP/ICMP packets in specific period, ARP storm is enabled for each port by programming the corresponding bits of page 0x01 register 0x15[11:0] and 0x16[12][9:4] to "1", ICMP storm is enabled for each port by programming the corresponding bits of page 0x01 register 0x18[11:0] and 0x19[12][9:4] to "1".

A port begins to drop incoming ARP packets if the received ARP packet reaches the threshold defined in page 0x01 register 0x14[7:0], a port begins to drop the incoming ICMP packets if the received ICMP packet reaches the threshold in page 0x01 register 0x17[7:0]. Besides, IP1819I provides four kinds of periods to be selected by programming page 0x01 register 0x14[9:8] for ARP storm control and 0x17[9:8] for ICMP storm control to "00~11".

Table 22 ARP and ICMP Storm Counter Clear Period Selection Table

0x14[9:8] & 0x17[9:8]	1000Mbps	100Mbps	10Mbps
00	200us	2ms	20ms
01	1ms	10ms	100ms
10	10ms	10ms	10ms
11	100ms	100ms	100ms

5.4.4 Block ARP to CPU Port

Related registers	0x14[10]	PAGE 0x01
	0x03[0]	PAGE 0x0C

In order to prevent ARP storm to reduce the performance of CPU port, IP1819I can drop ARP frames to CPU port If page 0x01 register 0x14[10] is set to “1” and page 0x0C register 0x03[0] is set to “1”. The default setting is ARP packets to be forwarded to CPU port.

5.4.5 Ethernet L2 protocol packet capture

Related registers	0x06 to 0x07	PAGE 0x00
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IP1819I recognizes layers 2 protocol frames (BPDU, 802.1x, LLDP, Slow Protocol, GxRP, ARP, and PPPoE) to decide packet should be forwarded, dropped or “To CPU” by programming page 0x00 register 0x06 and 0x07 and page 0x0C register 0x03[0], the detailed description is shown in the following table ,IP1819I also provides L2 protocols for user-defined by programming page 0x00 register 0x07[14] and page 0x00 register 0x23.

Table 23 Layers Two Protocol Frames Selection Table

L2 Protocol	DA	Register (PAGE 0)	Definition
BPDU	(01-80-C2-00-00-00)	0x06[1:0]	00: forward 01: reserved 10: To CPU port only. 11: drop
Slow Protocol	(01-80-C2-00-00-02)	0x06[3:2]	
802.1x	(01-80-C2-00-00-03)	0x06[5:4]	
LLDP	(01-80-C2-00-00-0E)	0x06[7:6]	
Group 0	(01-80-C2-00-00-05, 06, 09~0C, 0F)	0x06[9:8]	
	01-80-C2-00-00-04, 07, 08, 0D	0xB5[7:0]	
All Bridge address	(01-80-C2-00-00-10)	0x06[11:10]	
Group 1	(01-80-C2-00-00-11~1F)	0x06[13:12]	
GARP	(01-80-C2-00-00-20, 21)	0x06[15:14]	
Group 2	(01-80-C2-00-00-22~2F)	0x07[1:0]	
Group 3	(01-80-C2-00-00-30~3F)	0x07[3:2]	
ARP ether type = 0806		0x07[7]	0 : Forward depend on DA 1 : To DA and CPU port
IPv6 ether type = 86DD		0x07[10]	0 : Forward depend on DA 1 : To CPU port

5.4.6 Ethernet L3 protocol packet capture

Related registers	0x08 to 0x09	PAGE 0x00
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IP1819I recognizes layer 3 protocol frame (ICMP, TCP, UDP, OSPF ,and ICMP) to decide the packet should be forwarded, dropped or “To CPU” by programming page 0x00 register 0x08 and page 0x0C register 0x03[0]. The detailed configuration is shown in the following table.IP1819I also provides two L3 protocols for user-defined through page 0x00 register 0x08[11:8] and 0x09.

Table 24 Level Three Protocol Frames Selection Table

L3 Protocol	Register (PAGE 0)	Definition
ICMP	0x08 [1:0]	00: forward 01: reserved 10: To CPU port only. 11: drop
TCP	0x08 [3:2]	
UDP	0x08 [5:4]	
OSPF	0x08 [7:6]	
User define 1	0x08 [9:8]	
User define 2	0x08 [11:10]	
Ipv4 Other protocol	0x08 [13:12]	

5.4.7 PPPoE Protocol Check

Related registers	0x07[9:8], 0x56 to 0x59	PAGE 0x00
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IP1819I will check session ID of the PPPoE packets if page 0x00 register 0x07[9:8] are set to "11", if it matches, the header of the PPPoE packet will be removed ,if it doesn't match, the PPPoE header won't be removed. The PPPoE session ID can be configure by programming the corresponding bits of page 0x00 register 0x56 to 0x59.

5.5 Security

5.5.1 MAC Address Based Security

Related registers	0x02[6:4], 0x03[11:0], 0x04[12][9:4]	PAGE 0x01
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In order to drop illegal MAC packets, IP1819I supports the MAC address based security function. When this function is enabled, IP1819I has an option to drop the packet with the SA that does not find in the MAC table. This function is valid only if the MAC learning process is disabled by programming page 0x01 register 0x03[11:0] and 0x04[12][9:4].

For an unknown SA packet, If page 0x01 register 0x02[5] is set to “1”, the unknown SA packet will be forwarded. If page 0x01 register 0x02[5:4] is set to “01”, the unknown SA packet will be dropped. If page 0x01 register 0x02[5:4] is set to “00”, the unknown SA packet will be forwarded to CPU port.

IP1819I also supports SA associated with source port if page 0x01 register 0x02[6] is set to “1”. For example, if a packet with specific SA is learnt by port 1 in LUT, when the same SA of the packet on port 2 want to be sent to other port, the packets will not be forwarded. The packets with specific SA can send from any port if page 0x01 register 0x02[6] is set to “0”.

5.5.2 802.1x Port Based Security

Related registers	0x01[6], 0x06[5:4], 0x54[11:0], 0x55[12][9:4]	PAGE 0x00
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IP1819I supports 802.1x port based security function. If this function is enabled, IP1819I only forwards 802.1x EAPOL packets (DA=01 80 C2 00 00 03 and packet type=88 8E or DA= switch’s MAC address, packet type=88 8E and 0x01[6]=1) to CPU port and drops other types of packets. However, the ARP packets are not affected by this function and are forwarded according to their destination address.

The User can enable the 802.1x security function through programming page 0x00 register 0x06[5:4] to “10”. If the page 0x00 register 0x06[5:4] is set to “11”, all the EAPOL packets will be dropped. This function can be enabled individually for each port by programming page 0x00 register 0x54[11:0] and 0x55[12][9:4].

5.5.3 IP Address Based Security

Related registers	0x01[11:0], 0x02[15:13][12][9:4]	PAGE 0x02
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IP1819I supports IPv4/IPv6 address based security function by examining the SIP address of an incoming packet. User can set each port of IP1819I to check source IP address by programming page 0x02 register 0x01[11:0] and 0x02[12][9:4], and select one of the 2 filter modes by programming page 0x02 register 0x02[13] as shown in the following table.

To perform IP security, user has to fulfill the IP entries, if bit[183:181] in IP table are set to “111”, IP1819I will check IP address, MAC address, and source port of incoming packet whether matches the setting of IP table or not, if it matches, the packet will based on filter rule by programming page 0x02 register 0x2[13] to decide packet should be forwarded or dropped, There are two hashing methods to decide the location of an IP entry, hashing methods can support direct and CRC by programming page 0x02 register 0x02[15].

5.5.4 TCP/UDP Port Number Based Security

Related registers	0x12 to 0x20	PAGE 0x00
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IP1819I supports TCP/UDP port number based security function by checking the port number in an incoming packet. User can enable the function by programming register 0x1B[11:0] and 0x1C[12][9:4]. For instance, port 1 is corresponding to bit 0 of page 0x00 register 0x1B and port 13 is corresponding to bit 4 of page 0x00 register 0x1C.

When this function is enabled, a packet will have one of three behaviors: 1. to CPU 2. to CPU and ports 3. Drop it, if the TCP/UDP port number matches the conditions, which defined in page 0x00 register 0x12 to 0x16. For example, a packet with TCP/UDP port number (FTP: 20 or 21) will be dropped if page 0x00 register 0x12[3:0] is set to "1010". A packet with TCP/UDP port number (SMTP: 25) will be forwarded to CPU if page 0x00 register 0x12[15:12] is set to "1001".

IP1819I provides two user-define port number setting and three user-define port number range setting to let user define port number he wants.(reg. 0x0A to 0x11).

The well known TCP/UDP port is shown in following Table (defined in page 0x00 register. 0x12 to 0x15[11:0]), user-defined port number range setting of the TCP/UDP will override the well known TCP/UDP setting if the TCP/UDP port number is the same. For example, if FTP (20, 21) is set to drop and the port number (1~21) is set to forward to CPU port for user-defined range setting, a packet with port number (20, 21) will be forwarded to CPU port rather than dropped. There is a privilege for user-define range port number.

Table 25 TCP/UDP Port Number Based Security Selection Table

Register (PAGE 0)	Port number	Definition
_FTP	0x12 [3:0]	20, 21
SSH	0x12 [7:4]	22
TELNET	0x12 [11:8]	23
SMTP	0x12 [15:12]	25
DNS	0x13 [3:0]	53
BOOTP/DHCP	0x13 [7:4]	67, 68
TFTP	0x13 [11:8]	69
HTTP_0,1	0x13 [15:12]	80
POP3	0x14 [3:0]	110
NEWS	0x14 [7:4]	119
SNTP	0x14 [11:8]	123
NETBIOS0,1,2	0x14 [15:12]	137~139
IMAP_0,1	0x15 [3:0]	143, 220
SNMP_0,1	0x15 [7:4]	161, 162
HTTPS	0x15 [11:8]	443
USR A	0x15 [15:12]	User define A
USR B	0x16 [3:0]	User define B
USR C	0x16 [7:4]	User define C
USR D	0x16 [11:8]	User define D
USR E	0x16 [15:12]	User define E

1001: To CPU
1010: drop
1011: To CPU and ports

5.5.5 Port Mirroring Security (Sniffer)

Related registers	0x1E[11:0] to 0x23[12][9:4], 0x24[7:5]	PAGE 0x01
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In some circumstances, the network administrator requires to monitor the network traffic. The port mirroring function will help the network administrator to diagnose the content of network traffic.

IP1819I provides sniffer function to meet different actual requirement. It provide two destination port group configuration and several trigger criteria. These Sniffer function are illustrated as follows.

First Sniffer destination port group configuration function:

A port mirroring function is accomplished by assigning monitored ports (source ports), snooping ports (destination ports) and snooping method. IP1819I will copy the monitored packets to all snooping ports. The IP1819I supports three kinds of snooping methods: the ingress, egress and ingress + egress, which is defined in page 0x01 register 0x1F[14:13], the ports to be monitored (mirroring source), which is defined in register 0x22[11:0] and 0x23[12][9:4], the ports to snoop (mirroring destination), which is defined in page 0x01 register 0x1E[11:0] and 0x1F[12][9:4].

For example, if user wants to monitor the output traffic of port 16 and port 17 from port 1 as shown in the following figure. He has to write “01” to page 0x01 register 0x1F[14:13] to choose monitor method to be egress traffic, write 0x0800 and 0x0010 to page 0x01 register 0x22 and page 0x01 register 0x23 to select port 12 and port 13 to be monitored ports, write 0x0001 and 0x0000 to page 0x01 register 0x1E and page 0x01 register 0x1F to select port 1 as a monitoring port. IP1819I will copy the egress traffic port 12 and port 13 to port 1.

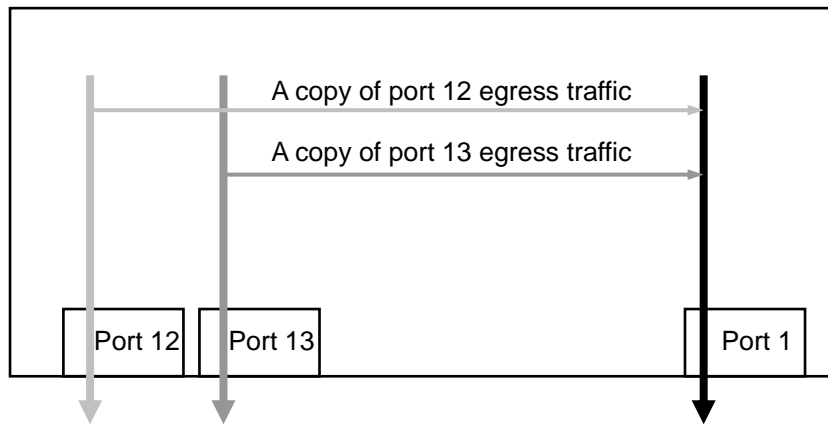


Figure 18 Port Mirroring Security Block Diagram

IP1819I also has options to keep the mirrored packet with the original tagging. The source of the mirrored packets can be separated into three groups. Their tagging status can be controlled through page 0x01 register 0x1F[15] and 0x24[7:5].

The above description is summarized as follows.

Sniffer Add/Rem Tag option for ACL routing

Original packet	Action(add/remove tag) by register 0xCC~0xCF(page 0x02)	behavior	
		Reg1f[15]=1, Reg24[6]=0(page 0x01)	Reg1f[15]=1, Reg24[6]=1(page 0x01)
		Destination port	Destination port
Untag	Add tag	Untag	Tag
Tag	Remove tag	Tag	Untag

Destination port must be assigned in the field of mode entry of ACL

Sniffer Add/Rem Tag option for CPU special tag routing

Original packet	Action(add/remove tag) by register 0xCC~0xCF(page 0x02)	behavior	
		Reg1f[15]=1, Reg24[5]=0(page 0x01)	Reg1f[15]=1, Reg24[5]=1(page 0x01)
		Destination port (only for CPU port)	Destination port (only for CPU port)
Untag	Add tag	Untag	Tag
Tag	Remove tag	Tag	Untag

Sniffer Add/Rem Tag option for other packet

Original packet (monitored port)	Action (add/remove tag) by register 0xCC~0xCF (page 0x02)	behavior	
		Reg1f[15]=1, Reg24[7]=0(page 0x01)	Reg1f[15]=1, Reg24[7]=1(page 0x01)
		Destination port	Destination port
Untag	Add tag	Untag	Tag
Tag	Remove tag	Tag	Untag

Destination port must be assigned in the field of special tag.

Second Sniffer destination port group configuration function:

IP1819I also provides second sniffer destination port group configuration function for MAC/IGMP/IP/ACL sniffing. IP1819I will forward packets to destination port for either first sniffer group or second sniffer group, according to MAC/IGMP/IP/ACL sniffing. Besides, DA or SA trigger can be selected for MAC address table by programming page 0x01 register 0x21[14:13], which can individually support first sniffer destination group configuration and second sniffer destination group configuration.

5.6 WAN/LAN Port Filtering

Related registers	0x0A to 0x11, 0x17 to 0x1A[12][9:4]	PAGE 0x00
	0x0D to 0x16[9:8][3:0]	PAGE 0x06

IP1819I supports TCP/UDP port number based filter function by checking both the port number in an incoming packet and an outgoing packet. User can enable the function by programming page 0x00 register 0x17 to 0x1A[12][9:4]. IP1819I also supports positive and negative filter. User can select either positive or negative filter to use, in positive filter, if a packet with TCP/UDP port number doesn't match the corresponding bit of TCP/UDP port number setting, the packet should be dropped according to WAN/LAN port filtering by programming page 0x06 register 0x0D to 0x16[9:8][3:0]. In negative mode, If a packet with TCP/UDP port number matches the corresponding bits of TCP/UDP port number setting, the packet should be dropped according to WAN/LAN port filtering by programming page 0x06 register 0x0D to 0x16[9:8][3:0]. WAN/LAN port filtering can be configured as “disable filter”, RX drop, TX drop, or TX/RX drop. For example. If “disable filter” is set, means that packet will be forwarded, if “RX drop” is set, means that packet will be dropped at host port.

IP1819I can choose either WAN port or LAN port by programming page 0x06 register 0x11[11:0] and 0x12[12][9:4]. For example, if the host port(port 1) is set to “forward to LAN port only” by programming page 0x06 register 0x0D[1:0] to “10” and client port(port 2) is set to LAN port by programming page 0x06 register 0x11[1] to “0” , the drop on ACT filtering only work at client port, and then the packet will be forwarded or dropped by programming page 0x06 register 0x0D[3:2] to “01” and programming page 0x06 register 0x13[3:2] to “00~1X”, if client port is WAN port, the packet is always dropped. If the host port is set to “forward to WAN port only” and client port is set to WAN port, the filtering only work at client port, if client port is LAN port, the packet is always dropped.

If host port(port 1) is set to “drop on ACT filtering” by programming page 0x06 register 0x0D[1:0] to “01” and programming page 0x06 register 0x13[1:0] to “00”(RX drop) , the packet will be dropped at host port(port 1), If client port(port 2) is set to “drop on ACT filtering” by programming “page 0x06 register 0x0D[3:2] to “01” and programming page 0x06 register 0x13[3:2] to “01”(TX drop) the packet will be dropped at client port(port 2). If host port and client port are set to “Disable Forwarding WAN/LAN& Packet drop”, the packet is always forwarded.

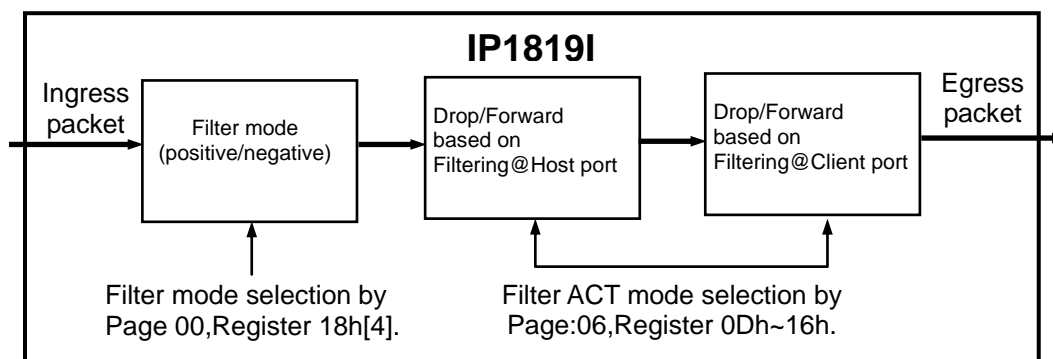


Figure 19 WAN Port Filtering Block Diagram

IP1819I's TCP/UDP port number filter mode (positive or negative) and the filter method conditions (disable, drop on act, Forwarding to WAN port only ,forward to LAN port only) is summarized as follows, please refer to the following table:

Table 26 Host / Client Forwarding WAN / LAN and Packet drop setting Condition Table

Host / Client Forwarding WAN / LAN and Packet drop setting Condition														
Host / Client		Client Port setting												
		Client is LAN Port						Client is WAN Port						
		00	01 Drop			10	11	00	01 Drop			10	11	
		Disable	RX	RX+TX	TX	LAN	WAN	Disable	RX	RX+TX	TX	LAN	WAN	
Host port setting	00	Disable	V	V	X	X	V	V	V	V	X	X	V	V
	01 Drop	Act on RX	X						X					
		Act on TX+RX	X						X					
		Act on TX	V	V	X	X	V	V	V	V	X	X	V	V
	10	FWD LAN	V	V	X	X	V	V	X	X	X	X	X	X
11	FWD WAN	X	X	X	X	X	X	V	V	X	X	V	V	

(1) V : PASS

(2) X : Drop

(3) Host port Switch Port to receive packet

(4) Client port Switch Port to transmit packet

5.7 IEEE 1588 Precision Timing Protocol (PTP)

Related registers	0x00 to 0x36	PAGE 0x09
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IP1819I implements the precision timing protocol (including IEEE1588/IEEE802.1as) function. For the PTP application, IP1819I uses the PTP dedicated hardware to capture the timestamp of PTP frame and store them into internal buffer; the software processes the various protocol message and co-work with PTP dedicated hardware.

To synchronous the master clock, IP1819I offers the adjustable real time clock (RTC), which could increases, decreases the clock frequency and set the specific time-value into RTC. If the PTP packet is detected, the PTP dedicated hardware will capture the time-value of SFD position for PTP or event signal. After the PTP synchronization process, the CPU uses the ingress/egress time-stamp to obtain the compensation parameter. Then, the CPU will pass the relating compensation value into PTP dedicated hardware. After the long duration, the PTP dedicated RTC is synchronous with the remote master clock.

For each port, IP1819I supports 32 depth timestamp FIFO(16 for ingress, 16 for egress) to record PTP time-stamp. When all time stamps are occupied, user also set overwrite bit enable to over write time stamps cyclically. Another, IP1819I also supports 8 time stamps for incoming event trigger signal.

For the monitor system application, IP1819I support three different output synchronous signals. These output signals are pulse-per second, the programming clock duration signal and trigger-out signal. Further, please refer to PTP application note in detail.

5.8 Hardware Loop detection

Related registers	0x6B[11:0] to 0x73, 0xA5[11:0], 0xA6[12][9:4]	PAGE 0x00
	0x24[3]	PAGE 0x01

IP1819I support hardware loop detection ,Each port can configure loop detection by programming page 0x00 register 0x6B[11:0] and 0x6C[12][9:4]. IP1819I will send loop detect packet to detect whether or not loop happen, IP1819I can check loop status of each port by reading the corresponding bits of page 0x00 register 0xA5[11:0] and 0xA6[12][9:4], if loop occur, IP1819I will block redundant until loop release. For blocking redundant path, page 0x01 register 0x24[3] must be set to “1”.

Hardware loop detection and EEE function can not be enabled at the same time. Because loop detect packet can not be sent at EEE mode.

5.9 Trunk Channel

Related registers	0x1C to 0x1D[9:8][3:0]	PAGE 0x01
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5.9.1 Trunk Channel Behavior

IP1819I provides two kinds of trunk methods to configure trunk group by programming page 0x01 register 0x1C and 0x1D[9:8][3:0]. one is the single trunk group and the other is the double trunk group, IP1819I supports 4 single trunk groups and 1 double trunk groups by programming page 0x01 register 0x1C[5]. The single trunk group A to C consist of 2 to 4 ports and trunk group D consist of 2 ports. The two single trunk groups can merge into one trunk group, for example, trunk A and B can be combined as a large trunk group, the members of double trunk group can be set as port 1~8(at least 2 ports), and so on. User can configure either the members of single trunk group or double trunk group individually by writing “1” to the corresponding bits of the port for each trunk in page 0x01 register 0x1C[15:8] and 0x1D[9:8][3:0]. A trunk channel works as if a “big” port with multiple times of bandwidth. If the destination port of a packet is un-link, IP1819I forwards the packet to the other port of the trunk (auto recovery).

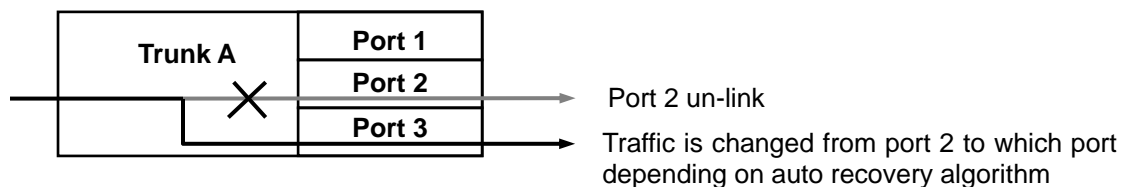


Figure 20 Trunk Channel Behavior Block Diagram

5.9.2 Load Balance

To fully utilize the bandwidth in a trunk channel, IP1819I supports load balance function. A physical port of a trunk forwards a packet only if the trunk ID of the packet matches the ID setting of the port. That is, when a packet is forwarded to a port in a trunk, its destination port is according to trunk ID.

IP1819I provides 8 kinds of hashing methods to support trunk function, user can select one of hashing methods to generate hashing ID by programming page 0x01 register 0x1C[2:0], the hashing ID0 means to select first port of the trunk group, hashing ID1 means to select second port of the trunk group, etc.

The sequence of the hashing methods can be set by programming page 0x01 register 0x1C[3], the behavior is illustrated as follows.

Case 1: disable sequence option: if incoming packet is not TCP/UDP packet and hashing method of the trunk group is set to TCP/UDP/SP, the hashing method will change to use DA/SA. If incoming packet is not TCP/UDP packet and hashing method of the trunk group is set to TCP/UDP/DP, the hashing method will change to use DA.

Case 2: enable sequence option: If incoming packet is not TCP/UDP packet and hashing method of the trunk group is set to TCP/UDP/SP, and then the hashing method will change depending on the type of packet. If the packet is IP packet, the hashing method will change to use SIP. If the packet is not IP packet, the hashing method will change to use DA/SA. If incoming packet is not TCP/UDP packet and hashing method of the trunk group is set to TCP/UDP/DP, if the packet is IP packet, the hashing method will change to use DIP. If the packet is not IP packet, the hashing method will change to use DA.

Each hashing method is described as follows

Hashing method	Port	SA	DA	SA/DA	SIP	DIP	TCP/UDP DP	TCP/UDP DP
Single trunk	By port	bit[1:0]	bit[1:0]	bit[1:0] XOR bit[1:0]	bit[3 XOR 2] bit[1 XOR 0]			
Double trunk	By port	bit[2:0]	bit[2:0]	bit[2:0] XOR bit[2:0]	bit[2 XOR 1]; bit[3 XOR 2]; bit[1 XOR 0]			

If the destination port of a trunk is un-link, the packet will be forward the port shifted by -1. If the port is un-link, too, the packet will be forward the port shifted by +2. For example, if port 4 is un-link, its packet will be forwarded to port 3. If port 3 is un-link, too, the packet will be forwarded to port 1.

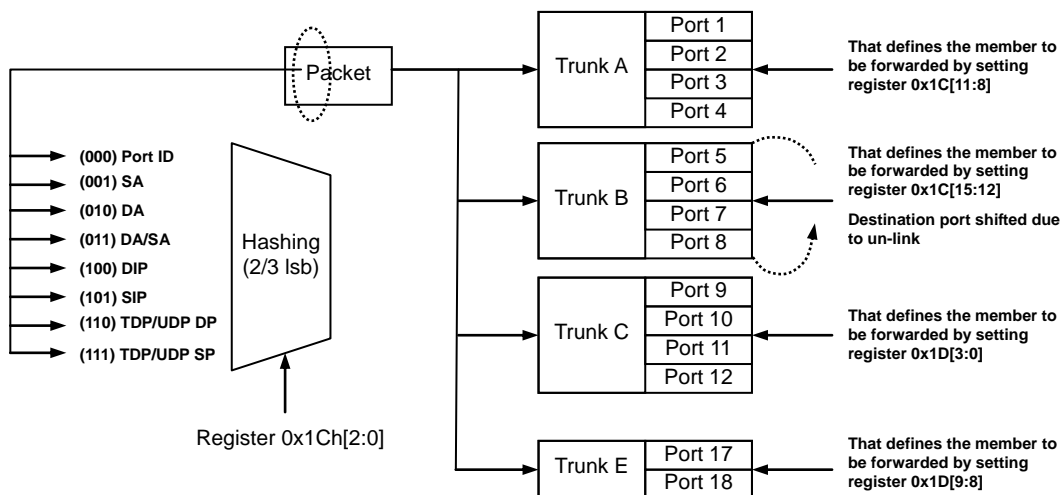


Figure 21 Load Balance Block Diagram

If the double trunk group is selected, the trunk hashing algorithm is changed from 2 bit to 3 bit, single trunk group uses 2 bits hashing algorithm to generate Hashing ID, ranging from 0 to 3, double trunk group use 3 bits hashing algorithm to generate Hashing ID, ranging from 0 to 7.

5.10 Spanning Tree

Related registers	0x06 [1:0]	PAGE 0x00
	0x57 to 0x96	PAGE 0x01
	0x03[1:0], 0x04[15:0]	PAGE 0x0C

5.10.1 BPDU Packet Forwarding

IP1819I support spanning tree function with the following steps:

1. Detect BPDU frames by examining multicast address (01-80-c2-00-00-00).
2. Forward BPDU packets to CPU and add special tag with port information.
3. Special tag type is defined in page 0x0C register 04[15:0] and the special tag enable by writing "1" to page 0x0C register 0x03[1]. The BPDU packets is forwarded to CPU port by writing "01" to page 0x00 register 0x06[1:0] and CPU port is enabled by writing "1" to page 0x0C register 0x03[0].

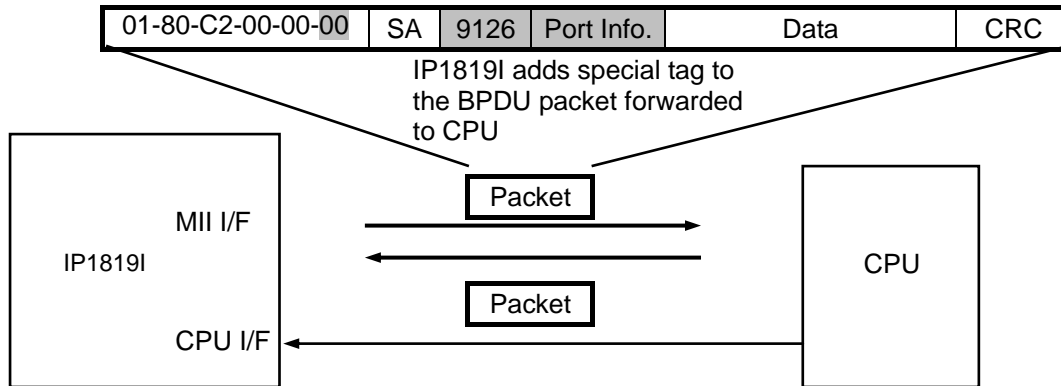


Figure 22 BPDU Packet Forwarding Block Diagram

5.10.2 Port States

Related registers	0x57[15:0] to 0x96[9:8][3:0]	PAGE 0x01
	0x06[6], 0xD2 to 0xD8	PAGE 0x02

To support IEEE802.1D spanning tree protocol, each port of IP1819I supports four states (discard state, blocking state, learning state, forwarding state), is shown in the following table. Each port of IP1819I can be set in one of the four spanning tree states individually by programming page 0x01 register 0x57[15:0] to 0x5A[9:8][3:0] for STP and page 0x01 register 0x57[15:0] to 0x96[9:8][3:0] for MSTP.

IP1819I also supports multiple STP. IP1819I will use MSTP registers to set up state for each port, IP1819I use FID field of VLAN table to mapping to corresponding register. IP1819I provides 16 set of VLAN settings for MSTP.

Table 27 Port States Selection Table

Status in 802.1D	Corresponding function (register)			
	BPDU packets		Normal packets	
	Port_RX(to CPU)	Port_TX(from CPU)	Port_RX (to CPU)	Port_TX(from CPU)
Discard(00)	X	X	X	X
Blocking(01)	O	X	X	X
Learning(10)	O	O	learning	X
Forwarding(11)	O	O	O	O

Note: O; means “ forward”, X: means “ not forward”

5.11 IGMP Snooping

Related registers	0x29 to 0x56	PAGE 0x01
	0x03[0]	PAGE 0x0C

IP1819I supports IGMPv1, v2 snooping and IGMPv3 aware specified in RFC1112,2236 and 3376 respectively. Because IGMP is used between hosts and multicast routers, IP1819I listens the IGMP messages that communicate between router and host to establish multicast group membership. Based on the group membership information, IP1819I forwards IP multicast data to its members which is registered in group table. IGMP snooping function can be configured by page 0x01 register 0x29 to 0x56. For hardware IGMPv1, v2 snooping, IP1819I receives query, report and leave packets to build multicast table. IP1819I also has an option to support timeout mechanism, If a host port is time expired in this group, the host port will leave the multicast group.

Except for hardware IGMPv1, v2 snooping, IP1819I also supports software IGMP snooping and IGMP snooping with CPU assistance. Software IGMP snooping implies that CPU must handle IP multicast traffic which includes IGMP packet and IP multicast data packet, and then forwards them to multicast group member after processing done. For the IGMP snooping with CPU assistance, the switch directly forwards the report and leave packets into CPU port, and then CPU will build multicast table according to report and leave packets. Besides, multicast data packet will be forwarded according to multicast table by IP1819I.

IP1819I supports not only IGMP snooping for IPv4 but also MLD snooping for IPv6. MLDv1 is similar to IGMPv2 and MLDv2 is similar to IGMPv3. When the IGMPv3 or MLDv2 multicast packets are coming, they will be forwarded depending on multicast table and source list table to forward packets by CPU.

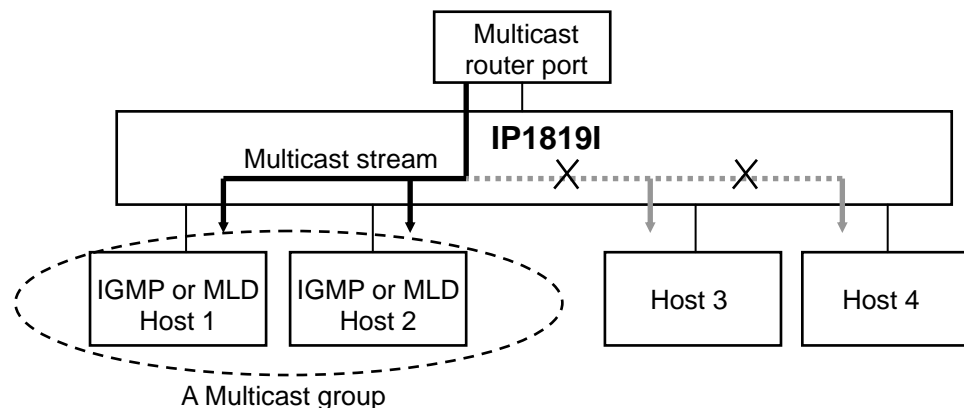


Figure 23 IGMP Snooping Block Diagram

5.12 IRMP(ICPLUS remote management protocol)

Related registers	0x01 to 0x0B	PAGE 0x0A
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IP1819I implements IRMP for accessing register in remote condition, IRMP is ICPLUS remote management protocol, all IP1819I registers can be easily accessed via running the IRMP protocol. All configurations of the IRMP protocol can be set by writing page 0x0A register 0x01 to 0x0B. In order to accomplish remote control, IRMP uses handshaking mechanism to complete the all IRMP actions, such as hello request /acknowledge action, login request /acknowledge, etc. The IRMP PDU frame structure is illustrated as follows (detail description please refers to application note).

Table 28 ICPLUS remote management protocol format

DA (6B) = Destination MAC address		SA (6B) = Source MAC address			Service tag (4B) (optional) [0x88A8_xxxx]	
Customer tag (4B) (optional)[0x8100_xxxx]	EtherType (2B) [0x8931]	SubType (2B) [0xFFFE]	Flag (1B)	Op (1B)	Vender ID (4B) [0x0090_C300]	Device ID(2B) [0x8290]
Password (4B) or Port information		Conn. ID(2B)	Reg Add 0(2B)	Reg Data 0(2B)	Reg Add 1(2B)	Reg Data 1(2B)
Reg Data 2(2B)	Reg Add 3(2B)	Reg Data 3(2B)	PAD [0x00]			CRC (4B)

5.13 IPv6 related functions configuration

Related registers	0xA7 to 0xAC	PAGE 0x00
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IP1819I also supports IPv6 protocol, IP1819I examines IPv6 header to support specific purpose for IPv6 protocol. IP1819I will check next header in IPv6 header, if it matches, IPv6 packet will be forwarded, dropped, "To CPU and DA", or To CPU by programming page 0x00 register 0xA8 to 0xAC, IP1819I supports the following header table.

Table 29 IPv6 Header

Order	Header type	Next header code(DEC)
1	Fragment Header	44
2	Encapsulation header	50
3	Authentication Header	51
4	ICMPv6	58
5	User-defined header	xx

NDP (neighbor discovery protocol) is defined in RFC 2461. It uses ICMPv6 to exchange the messages necessary for its functions.

Table 30 NDP Header

Order	Type	Next header code(DEC)
1	Router solicitation	133
2	Router Advertisement	134
3	Neighbor solicitation	135
4	Neighbor Advertisement	136
5	redirect	137

MLD (Multicast Listener Discovery) the protocol is embedded in ICMPv6 instead of using a separate protocol. MLDv1 is similar to IGMPv2 and MLDv2 is similar to IGMPv3. The protocol is described in RFC 3810.

Table 31 MLD Header

Order	Type	Next header code(DEC)
1	MLDv1 query	130
2	MLDv1 listener report	131
3	MLDv1 listener done	132
4	MLDv2 listener report	143

5.14 ACL

Related registers	0x52[11:0], 0x53[12][9:4]	PAGE 0x00
	0x24 & 0x99	PAGE 0x01
	0x8A[11:0] to 0xED	PAGE 0x02
	0x01[11:0] to 0x6F[12][9:4]	PAGE 0x07

IP1819I supports 128-entries for ACL rule. The ACL function is enabled if page 0x01 register 0x24[0] is set to "1" , When a packet is received, IP1819I will examine whether the incoming packet meet in specific ACL rule entries in mode table, each mode comprises of some rules, such as SIP, DIP, TCP/UDP, SMAC, DMAC, VLAN and physical port, and so on. If it matches, the packet will act according to corresponding ACT entry.

5.15 OAM

Related registers	0x01 to 0x08[12][9:4]	PAGE 0x04
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IEEE802.3ah OAM (Operation, Administration and Maintenance) is a point to point slow protocol and is used to maintain the health of the link. The main functions are provided as follow :

- Auto Discovery
- Fault Indication
- Remote LoopBack Test

6 bytes	6 bytes	2 bytes	1 bytes	2 bytes	1 bytes		
DA(01-80-C2-00-00-02)	SA	8809	03	flags	code	Data	FCS

Figure 24 802.3 OAM Frame Format

IP1819I supports OAM functions, including Auto Discovery/ Fault Indication/ Remove LoopBack Test/ Remote R/W registers.

IP1819I OAM functions and controls are set via accessing the indirect register per port. Detail information please refers to the OAM application note.

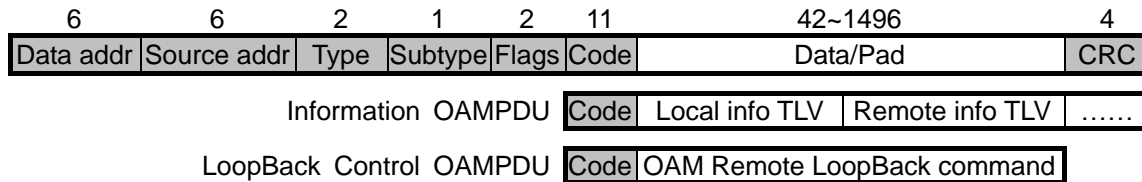


Figure 25 OAMPDU messages Frame Format

5.16 Special tag

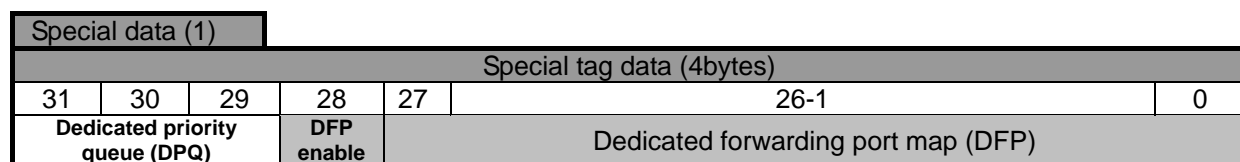
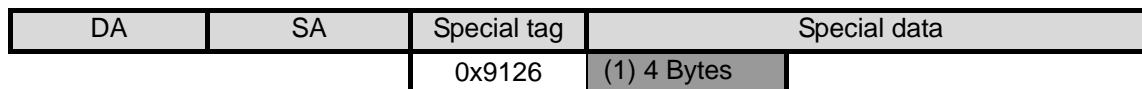
Related registers	0x41[13]	PAGE 0x00
	0x03[1:0], 0x04	PAGE 0x0C

The purpose of special tag is:

- To allow a frame (switch to CPU) to carry ingress port number ,Queue ID ,PTP and sFlow information carriers in special tag header
- To allow a frame (CPU to switch) to indicate the output port mask and output queue number carriers in special tag header

5.16.1 Special Tag for TX (From CPU to switch)

Frame direction is from CPU to switch. IP1819I enables special tag function by programming register page 0x0C register 0x03[1]. This function provides dedicated forwarding port decision and priority assignment information. This information is embedded in special tag header, which can be set by CPU. The special data will be removed by switch itself when the dedicated port had received packet, if DFP is set to 0 , the frame will be based on its DA to be forwarded.



DPQ Enable bit : 0x41[13] page0 (0:Q0 , 1:Q1 , , 7: Q7)

Figure 26 Special Tag for TX Frame Format (From CPU to switch)

5.16.2 Special Tag for RX (From switch to CPU)

Frame direction is from switch to CPU. IP1819I enables special tag function by programming page 0x0C register 0x03[1]. The special tag information consists of source port number and QID, if the incoming packet with OAM information is forwarded to CPU, CPU will showed off OAM packet Flag field and code, these information carrier in special tag header 0x9126 (Page 0x0C Reg. 0x04).

DA	SA	Special tag	Special data		
		0x9126	(1) 4 Bytes		
		0x9127(+1)	(1) 4 Bytes	(3) 8 bytes	PTP stamp info
		0x9128(+2)	(1) 4 Bytes	(2) 28 bytes	sFlow info
		0x9129(+3)	(1) 4 Bytes	(2) 28 bytes	sFlow info
				(3) 8 bytes	PTP stamp info

Special data (1)															
Special tag data (4bytes)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PTP/ normal (0)			Stamp	U/M	ACL redirect	Snif	U-SA	CCPU	DLF	PTP	SEQ3	SEQ2	SEQ1	SEQ0	-
CFM opcode (6,5,4,3,2,1)			U/M	U/M	ACL redirect	Snif	U-SA	CCPU	DLF	MD_Level			-		
OAM (7)			OAMPDU Flag field						OAMPDU code			-			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-								Queue ID			Source port				

CFM opcode&OAM &others	7: OAM	6: others CFM opcode		
	5: LTM	4: LTR		
	3: LBM	2: LBR		
	1: CCM	0: PTP or normal packet (not include CFM,OAM)		
OAMPDU Flag & code	OAMPDU Flag		OAMPDU code	
	bit[6]:remote stable	6.7 : others		
	bit[5]:remote evaluating	5: organization specific		
	bit[4]:local stable	4: LoopBack control		
	bit[3]:local evaluating	3: variable request		
	bit[2]:critical event	2: variable response		
	bit[1]:dying gasp	1: Event notification		
	bit[0]:link fault	0: information		
U/M	Uni port / Multi port output			
ACL redirect	ACL action redirect			
Snif	Sniffer packet			
U-SA	Unknown SA			
CCPU	Capture to CPU			
DLF	Destination lookup Fail			
STAMP	PTP packet is stamped			
PTP	PTP packet [31:29] =0 , PTP packet [21]=1			
SEQ0,1,2,3	PTP RX stamp sequence			
QID	Out Queue from which Queue ID			
SP	Source port			

Figure 27 Special Tag for RX Frame Format (From switch to CPU)

If PTP special tag data is enabled by programming "1" to page 0x07 register 0x7A[5], the PTP special data will be added to incoming packet, and then the packet will be forwarded to CPU, the special tag is 0x9127. If sFlow special tag data is enabled by programming "1" to page 0x07 register 0x7A[4], the sFlow special data will be added to incoming packet, and then the packet will be forwarded to CPU, the special tag is 0x9128. If PTP and sFlow special tag data is enabled by programming "11" to page 0x07 register 0x7A[5:4], the both PTP and sFlow special data will be added to incoming packet, and then the packet will be forwarded to CPU, the special tag is 0x9129.

Special data (2)																
Special tag data (28bytes)																
223	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	
Customer tag Remove/Add [57:42]																
207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192	
Customer tag Remove/Add [41:26]																
191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176	
Customer tag Remove/Add [25:10]																
175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160	
Customer tag Remove/Add [9:0]										arl_route_result [28:23]						
159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144	
arl_route_result [22:7]																
143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128	
arl_route_result [6:0]						PRI [2:0]				Mac rx count [14:9]						
127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	
Mac rx count [8:0]								VID[11:5]								
111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96	
VID [4:0]					ACL SF	Egress SF	Ingress SF	SF_Rate [15:8]								
95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	
SF_Rate [7:0]								0								
79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	
0								Service tag Remove/Add [57:48]								
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	
Service tag Remove/Add [47:32]																
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	
Service tag Remove/Add [31:16]																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Service tag Remove/Add [15:0]																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0												PPPoE remove	QID			

Special data (3)															
Special tag data (8bytes)															
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Time stamp second [31:16]															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Time stamp second [15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
full	0	Time stamp nano second [29:16]													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time stamp nano second [15:0]															

5.17 sFlow

Related registers	0x97[11:0] to 0xD8	PAGE 0x01
	0x7A[3:0]	PAGE 0x07

IP1819I supports sFlow function, which can monitor the content of the packet, IP1819I provides various methods to sample sFlow packet to CPU port, such as inbound, outbound, VID, ACL and MAC Lookup table, which can be set by programming page 0x01 register 0x99, 0x9A, 0x9B[5:0], 0x9D and 0x9E[11:9][2:0]. sFlow can be configured individually for each port, such as sampling rate, etc. IP1819I also provides global counter or independent counter, which can be set by programming page 0x01 register 0x9E[12]. For example, if global counter is set by programming page 0x01 register 0x9E[12] to “1” and inbound method is set by programming the corresponding bits of page 0x01 register 0x99, 0x9A, 0x9B[5:0], 0x9D and 0x9E[11:9][2:0] to “000”, packets start to accumulate for all ports during incoming packet is received, when accumulated packets reach threshold value, then one sampled packet will be forwarded to CPU port.

Besides, IP1819I also supports length cutoff mechanism for sFlow packet. According to the setting of the cutoff in page 0x07 register 0x7A[3:0]. If the sFlow packet length is less than the setting of the length cutoff, the sFlow packet length will keep unchanged. If the sFlow packet length is more than the setting of the length cutoff, the sFlow packet length will be cutoff.

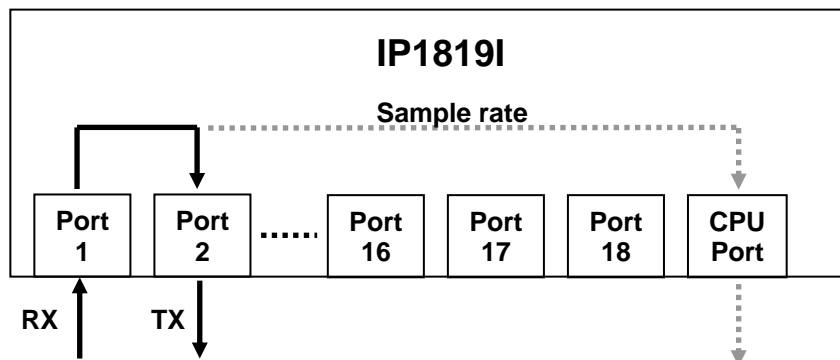


Figure 28 sFlow function diagram

5.18 WOL+

IP1819I provides WOL+ function for WOL+ port that can speed down to 10Mbps in the idle status and recover to the previous speed status by detecting WOL+ events. For example, if WOL+ port have no activity exceeds pre-defined idle time, the WOL+ ports will link to 10Mbps, If IP1819I detects WOL+ events in down speed period, IP1819I will change the speed status of ports to 100Mbps from 10Mbps for WOL+ port 1~16 and change the speed status of the port to 1000Mbps/100Mbps from 10Mbps for WOL+ port 17~18.

The WOL+ function is enabled and disabled for port 1~16 by writing both page 0 register 0xAD[11:0] and 0xAE[7:4], and PHY’s page 4 register 0x16[13]. WOL+ function for port 17~18 are enabled and disabled by writing both page 0 register 0xAE[9:8] and page 3 register 0x10[1:0], the WOL+ event for port 17~18 also be configured as detecting magic packet and any packet by writing page 3 register 0x10[7:4].

IP1819I also supports 4 kinds of time units, the unit of idle time can be set to 00: “disable”, 01: “10s”, 10: “1min”, and 11: “10 min” by writing page 0 register 0xAF[6:5], if the idle time of the WOL+ port reaches threshold, the WOL+ port will link to 10Mbps.

IP1819I also provides WOL+ master and slave modes, only the difference between master mode and slave mode. In slave mode, WOL+ port is enabled by writing page 0 register 0xB0[11:0] and 0xB1[12][9:4], and reading page 0 register 0xB2[11:0] and 0xB3[12][9:4] for WOL+ port status to complete WOL+ action by CPU. In master mode, HW can automatically finish the WOL+ action.

6 Register Description

6.1 PHY Register Map

Read / Write PHY register by page 3 register 0x13, 0x14

Table 32 PHY Register Map

Page	PHY address	Register	Description	Default
0	PHY 08~19, 28~31	0	Control Register	
0	PHY 08~19, 28~31	1	Status Register	
0	SHARE X 1	2	PHY Identifier 1 Register	
0	SHARE X 1	3	PHY Identifier 2 Register	
0	PHY 08~19, 28~31	4	Auto-Negotiation Advertisement Register	
0	PHY 08~19, 28~31	5	Auto-Negotiation Link Partner Ability Register	
0	PHY 08~19, 28~31	6	Auto-Negotiation Expansion Register	
0	PHY 08~19, 28~31	7	Auto-Negotiation Next Page Transmit Register	
0	PHY 08~19, 28~31	8	Auto-Negotiation Link Partner Next Page Register	
0	PHY 08~19, 28~31	13	MMD Access Control Register	
0	PHY 08~19, 28~31	14	MMD Access Address Data Register	
0	PHY 08~19, 28~31	3.0	PCS control 1 register	
0	PHY 08~19, 28~31	3.1	PCS status 1 register	
0	PHY 08~19, 28~31	3.20	EEE capability	
0	PHY 08~19, 28~31	3.22	EEE wake error count	
0	PHY 08~19, 28~31	7.60	EEE advertisement register	
0	PHY 08~19, 28~31	7.61	EEE link partner ability	
0	SHARE X 3	16	Special Control Register (APS)	
0	PHY 08~19, 28~31	18	Special Status Register	
X	SHARE X 3	20	Page Control Register	
4	SHARE X 3	16	WOL+ Control Register	
0	PHY 08~19, 28~31	23	MDI/MDIX Control Register	
1	PHY 08~19, 28~31	23	10BaseT Control Register	

Share x 1: 16 ports share the register

Share x 3: 8 ports, 4 ports and 4 ports share the register

X16 Each port has its individual register

X: indicate do not care.

Table 33 Register Symbol Abbreviations

Type	Description
R	Read
W	Write
R/W	Read/Write
SC	Self-Clearing
RO	Read Only
LL	Latching Low
LH	Latching High

6.1.1 MII Register

MII register 0 of PHY08~19,28~31 (Each PHY has its own MII register 0 with different PHY address)

PHY	MII	R/W	Description	Default
Control Register				
08~19, 28~31	0.15	RW/ SC	Reset The PHY is reset if user writes "1" to this bit. The reset period is around 2ms. User has to wait for at least 2ms to access IP1819I.	0
08~19, 28~31	0.14	R/W	Loop back 1 = Loop back mode 0 = normal operation When this bit set, IP1819I will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN.	0
08~19, 28~31	0.13	RW	Speed Selection 1 = 100Mbps 0 = 10Mbps It is valid only if bit 0.12 is set to be 0.	1
08~19, 28~31	0.12	RW	Auto-Negotiation(AN) Enable 1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable	1
08~19, 28~31	0.11	R/W	Power Down 1: power down mode 0: normal operation	0
08~19, 28~31	0.10	-	Isolate IP1819I doesn't support this function.	0
08~19, 28~31	0.9	RW/ SC	Restart Auto-Negotiation 1 = re-starting Auto-Negotiation 0 = Auto-Negotiation re-start complete	0
08~19, 28~31	0.8	R/W	Duplex mode 1 = full duplex 0 = half duplex It is valid only if bit 0.12 is set to be 0.	1
08~19, 28~31	0.7	R/W	Collision test	0
08~19, 28~31	0.6	RO	Reserved	0
08~19, 28~31	0.5	R/W	Unidirectional enable When bit 0.12 is one or bit 0.8 is zero or bit 0.13 is zero, this bit is ignored. When bit 0.12 is zero and bit 0.8 is one and bit 0.13 is one : 1 = Enable transmit from MII regardless of whether the PHY has determined that a valid link has been established. 0 = Enable transmit from MII only when the PHY has determined that a valid link has been established.	0
08~19, 28~31	0[4:0]	RO	Reserved	0

MII register 1 of PHY08~19,28~31 (Each PHY has its own MII register 1 with different PHY address)

PHY	MII	R/W	Description	Default
Status Register				
08~19, 28~31	1.15	RO	100Base-T4 capable 1 = 100Base-T4 capable 0 = not 100Base-T4 capable IP1819I does not support 100Base-T4. This bit is fixed to be 0.	0
08~19, 28~31	1.14	RO	100Base-X full duplex Capable 1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable	1
08~19, 28~31	1.13	RO	100Base-X half duplex Capable 1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable	1
08~19, 28~31	1.12	RO	10Base-T full duplex Capable 1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable	1
08~19, 28~31	1.11	RO	10Base-T half duplex Capable 1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable	1
08~19, 28~31	1.10	RO	100Base-T2 full duplex Capable 1 = 100Base-T2 full duplex capable 0 = not 100Base-T2 full duplex capable	0
08~19, 28~31	1.9	RO	100Base-T2 half duplex Capable 1 = 100Base-T2 half duplex capable 0 = not 100Base-T2 half duplex capable	0
08~19, 28~31	1.8	RO	Extended Status	0
08~19, 28~31	1.7	RO	Unidirectional ability 1 = PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established. 0 = PHY able to transmit from MII only when the PHY has determined that a valid link has been established.	1
08~19, 28~31	1.6	RO	MF preamble Suppression 1 = preamble may be suppressed 0 = preamble always required	1
08~19, 28~31	1.5	RO	Auto-Negotiation Complete 1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0

MII register 1 of PHY08~19,28~31 (Each PHY has its own MII register 1 with different PHY address)

PHY	MII	R/W	Description	Default
Status Register				
08~19, 28~31	1.4	RO LH	Remote fault 1 = remote fault detected 0 = not remote fault detected When read as logic 1, indicates that IP1819I has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP1819I reset.	0
08~19, 28~31	1.3	RO	Auto-Negotiation Ability 1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable When read as logic 1, indicates that IP1819I has the ability to perform Auto-Negotiation.	1
08~19, 28~31	1.2	RO LL	Link Status 1 = Link Pass 0 = Link Fail When read as logic 1, indicates that IP1819I has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
08~19, 28~31	1.1	RO LH	Jabber Detect 1 = jabber condition detected 0 = no jabber condition detected When read as logic 1, indicates that IP1819I has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP1819I reset. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loop back functions will be disabled and the COL is active. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled.	0
08~19, 28~31	1.0	RO	Extended capability 1 = Extended register capabilities 0 = No extended register capabilities IP1819I has extended register capabilities.	1

MII register 2 of PHY08~19,28~31 (16 PHYs share the MII register)

PHY	MII	R/W	Description	Default
PHY Identifier 1 Register				
08~19, 28~31	2	RO	IP1819I OUI (Organizationally Unique Identifier) ID, the MSB is 3 rd bit of IP1819I OUI ID, and the LSB is 18 th bit of IP1819I OUI ID. IP1819I OUI is 0090C3.	16'h0243

MII register 3 of PHY08~19,28~31 (16 PHYs share the MII register)

PHY	MII	R/W	Description	Default
PHY Identifier 2 Register				
08~19, 28~31	3[15:10]	RO	PHY identifier IP1819I OUI ID, the MSB is 19 th bit of IP1819I OUI ID, and LSB is 24 th bit of IP1819I OUI ID.	6'h03
08~19, 28~31	3[9:4]	RO	Manufacture's Model Number IP1819I model number	6'h01
08~19, 28~31	3[3:0]	RO	Revision Number IP1819I revision number	0

MII register 4 of PHY08~19,28~31 (Each PHY has its own MII register 4 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Advertisement Register				
08~19, 28~31	4.15	R/W	1 = Next pages are supported 0 = Next pages are not supported	0
08~19, 28~31	4.14	RO	Reserved by IEEE, write as 0, ignore on read	0
08~19, 28~31	4.13	R/W	Remote Fault 1 = Advertises that this port has detected a remote fault. 0 = There is no remote fault.	0
08~19, 28~31	4.12	RO	Reserved for future IEEE use, write as 0, ignore on read	0
08~19, 28~31	4.11	RW	Asymmetric PAUSE 1 = Asymmetric flow control is supported 0 = Asymmetric flow control is not supported	1
08~19, 28~31	4.10	RW	PAUSE 1 = Symmetric flow control is supported 0 = Symmetric flow control is not supported	1
08~19, 28~31	4.9	RO	100BASE-T4 Not supported	0
08~19, 28~31	4.8	R/W	100BASE-TX full duplex 1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	1
08~19, 28~31	4.7	R/W	100BASE-TX 1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	1
08~19, 28~31	4.6	R/W	10BASE-T full duplex 1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	1
08~19, 28~31	4.5	R/W	10BASE-T 1 = 10BASE-T is supported 0 = 10BASE-T is not supported	1
08~19, 28~31	4[4:0]	RO	Selector Field Use to identify the type of message being sent by Auto-Negotiation.	5'b00001

MII register 5 of PHY08~19,28~31 (Each PHY has its own MII register 5 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Link Partner Ability Register				
08~19, 28~31	5.15	RO	Next Page 1 = Next Page ability is supported by link partner 0 = Next Page ability does not supported by link partner	0
08~19, 28~31	5.14	RO	Acknowledge 1 = Link partner has received the ability data word 0 = Not acknowledge	0
08~19, 28~31	5.13	RO	Remote Fault 1 = Link partner indicates a remote fault 0 = No remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.	0
08~19, 28~31	5.12	RO	Reserved by IEEE for future use, write as 0, and read as 0.	0
08~19, 28~31	5.11	RO	Asymmetric PAUSE 1 = Link partner support Asymmetric PAUSE 0 = Link partner does not support Asymmetric PAUSE When local or link partner is Auto-negotiation disabled, this bit is read as 1. The pause resolution is determined by MII Reg4[11:10].	0
08~19, 28~31	5.10	RO	PAUSE 1 = Link partner support Symmetric PAUSE 0 = Link partner does not support Symmetric PAUSE When local or link partner is Auto-negotiation disabled, this bit is read as 1. The pause resolution is determined by MII Reg4[11:10].	0
08~19, 28~31	5.9	RO	100BASE-T4 1 = Link partner support 100BASE-T4 0 = Link partner does not support 100BASE-T4	0
08~19, 28~31	5.8	RO	100BASE-TX full duplex 1 = Link partner support 100BASE-TX full duplex 0 = Link partner does not support 100BASE-TX full duplex	0
08~19, 28~31	5.7	RO	100BASE-TX 1 = Link partner support 100BASE-TX 0 = Link partner does not support 100BASE-TX	0
08~19, 28~31	5.6	RO	10BASE-T full duplex 1 = Link partner support 10BASE-T full duplex 0 = Link partner does not support 10BASE-T full duplex	0
08~19, 28~31	5.5	RO	10BASE-T 1 = Link partner support 10BASE-T 0 = Link partner does not support 10BASE-T	0
08~19, 28~31	5[4:0]	RO	Selector Field Protocol selector of the link partner	5'b000 00

MII register 6 of PHY08~19,28~31 (Each PHY has its own MII register 6 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Expansion Register				
08~19, 28~31	6[15:5]	RO	Reserved	0
08~19, 28~31	6.4	RO/ LH	Parallel Detection Fault 1 = a fault has been detected via parallel detection function. 0 = a fault has not been detected via parallel detection function.	0
08~19, 28~31	6.3	RO	Link Partner Next Page Able 1 = Link partner is next page able. 0 = Link partner is not next page able. In 100FX or AN disabled, then this bit is always equal to 0.	0
08~19, 28~31	6.2	RO	Next Page Able 1 = IP1819I next page able. 0 = IP1819I is not next page able.	1
08~19, 28~31	6.1	RO/ LH	Page Received 1 = A new page has been received. 0 = A new page has not been received.	0
08~19, 28~31	6.0	RO	If AN is enabled, this bit means: 1 = Link partner is Auto-Negotiation able. 0 = Link partner is not Auto-Negotiation able. In 100FX or AN disabled, then this bit is always equal to 0.	0

MII register 7 of PHY08~19,28~31 (Each PHY has its own MII register 7 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Next Page Transmit Register				
08~19, 28~31	7.15	RW	Next Page Transmit Code Word bit 15	0
08~19, 28~31	7.14	RO	Reserved Transmit Code Word bit 14	0
08~19, 28~31	7.13	RW	Message Page Transmit Code Word bit 13	1
08~19, 28~31	7.12	RW	Acknowledge 2 Transmit Code Word bit 12	0
08~19, 28~31	7.11	RO	Toggle Transmit Code Word bit 11	0
08~19, 28~31	7[10:0]	RW	Message/Unformatted Field Transmit Code Word bit 10:0	1

MII register 8 of PHY08~19,28~31 (Each PHY has its own MII register 8 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Link Partner Next Page Register				
08~19, 28~31	8.15	RO	Next Page Received Code Word bit 15	0
08~19, 28~31	8.14	RO	Acknowledge Received Code Word bit 14	0
08~19, 28~31	8.13	RO	Message Page Received Code Word bit 13	0
08~19, 28~31	8.12	RO	Acknowledge 2 Received Code Word bit 12	0
08~19, 28~31	8.11	RO	Toggle Received Code Word bit 11	0
08~19, 28~31	8[10:0]	RO	Message/Unformatted Field Received Code Word bit 10:0	0

MII register 16 of PHY08~19,28~31 (8 PHYs, 4PHYs and 4PHYs share the MII register)

PHY	MII	R/W	Description	Default
Special Control Register				
08~19, 28~31	16.7	RW	Advance power saving mode 1 = Enable APS mode (default) 0 = Disable APS mode Please refer to the Power Saving application note for more detail description.	1
08~19, 28~31	16.4	RW	Far end fault function 1 = Far end fault function disable 0 = Far end fault function enable (default) This bit is only used for fiber mode.	0

MII register 18 of PHY08~19,28~31 (Each PHY has its own MII register 18 with different PHY address)

PHY	MII	R/W	Description	Default
Special Status Register				
08~19, 28~31	18.14	RO	Linkup 1 = linkup 0 = unlink	0
08~19, 28~31	18.11	RO	Speed Mode 1 = 100 Mbps 0 = 10 Mbps	0
08~19, 28~31	18.10	RO	Duplex Mode 1 = Full Duplex 0 = Half Duplex	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

6.1.2 MMD Control Register

MII register 13 of PHY08~19,28~31 (Each PHY has its own MII register 13 with different PHY address)

PHY	MII	R/W	Description	Default
MMD Access Control Register				
08~19, 28~31	13[15:14]	R/W	Function 00 = address 01 = data, no post increment 10 = data, post increment on reads and writes 11 = data, post increment on writes only	0
08~19, 28~31	13[13:5]	R/W	Reserved Write as 0, ignore on read	0
08~19, 28~31	13[4:0]	R/W	DEVAD Device Address	0

MII register 14 of PHY8~19,28~31 (Each PHY has its own MII register 14 with different PHY address)

PHY	MII	R/W	Description	Default
MMD Access Address Data Register				
08~19, 28~31	14[15:0]	R/W	Address Data If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register	0

Example 1, Read 0.3.20 (Read Data from MMD register 3.20 of PHY address 0):

1. Write 0.13 = 0x0003 //MMD DEVAD 3
2. Write 0.14 = 0x0014 //MMD Address 20
3. Write 0.13 = 0x4003 //MMD Data command for MMD DEVAD 3
4. Read 0.14 //Read MMD Data from 0.3.20

Example 2, Write 1.7.60 = 0x3210 (Write 0x3210 Data to MMD register 7.60 of PHY address 1):

1. Write 1.13 = 0x0007 //MMD DEVAD 7
2. Write 1.14 = 0x003C //MMD Address 60
3. Write 1.13 = 0x4007 //MMD Data command for MMD DEVAD 7
4. Write 1.14 = 0x3210 //Write MMD Data 0x3210 to 1.7.60

6.1.3 MMD Data Register

MMD register 3.0 of PHY8~19,28~31 (Each PHY has its own MMD register 3.0 with different PHY address)

PHY	MII	R/W	Description	Default
PCS control 1 Register				
08~19, 28~31	3.0[15:11]	RO	Reserved Ignore when read	0
08~19, 28~31	3.0.10	R/W	Clock stop enable 1 = PHY may stop xMII Rx clock during LPI 0 = Clock not stoppable	0
08~19, 28~31	3.0[9:0]	RO	Reserved Ignore when read	0

MMD register 3.1 of PHY08~19,28~31 (Each PHY has its own MMD register 3.1 with different PHY address)

PHY	MII	R/W	Description	Default
PCS status 1 Register				
08~19, 28~31	3.1[15:12]	RO	Reserved Ignore when read	0
08~19, 28~31	3.1.11	RO/LH	Tx LPI received 1 = Tx PCS has received LPI 0 = LPI not received	0
08~19, 28~31	3.1.10	RO/LH	Rx LPI received 1 = Rx PCS has received LPI 0 = LPI not received	0
08~19, 28~31	3.1.9	RO	Tx LPI indication 1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	0
08~19, 28~31	3.1.8	RO	Rx LPI indication 1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	0
08~19, 28~31	3.1.7	RO	Reserved Ignore on read	0
08~19, 28~31	3.1.6	RO	Clock stop capable 1 = The MAC may stop the xMII Tx clock during LPI 0 = Clock not stoppable	0
08~19, 28~31	3.1[5:0]	RO	Reserved Ignore when read	0

MMD register 3.20 of PHY08~19,28~31 (Each PHY has its own MMD register 3.20 with different PHY address)

PHY	MII	R/W	Description	Default
EEE capability Register				
08~19, 28~31	3.20[15:7]	RO	Reserved Ignore when read	0
08~19, 28~31	3.20.6	RO	10GBASE-KR EEE 1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR	0
08~19, 28~31	3.20.5	RO	10GBASE-KX4 EEE 1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4	0
08~19, 28~31	3.20.4	RO	1000BASE-KX EEE 1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX	0
08~19, 28~31	3.20.3	RO	10GBASE-T EEE 1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T	0
08~19, 28~31	3.20.2	RO	1000BASE-T EEE 1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T	0
08~19, 28~31	3.20.1	RO	100BASE-TX EEE 1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX	1
08~19, 28~31	3.20.0	RO	Reserved Ignore when read	0

MMD register 3.22 of PHY08~19,28~31 (Each PHY has its own MMD register 3.22 with different PHY address)

PHY	MII	R/W	Description	Default
EEE wake error count				
08~19, 28~31	3.22[15:0]	RO	EEE wake error count Count wake time faults where IP1819I fails to complete its normal wake sequence within the time required for the specific PHY type. This register keeps the value before reading the contents of the register.	0x0000

MMD register 7.60 of PHY08~19,28~31 (Each PHY has its own MMD register 7.60 with different PHY address)

PHY	MII	R/W	Description	Default
EEE advertisement Register				
08~19, 28~31	7.60[15:7]	RO	Reserved Ignore when read	0
08~19, 28~31	7.60.6	RO	10GBASE-KR EEE 1 = Advertise that the 10GBASE-KR has EEE capability 0 = Do not advertise that the 10GBASE-KR has EEE capability	0
08~19, 28~31	7.60.5	RO	10GBASE-KX4 EEE 1 = Advertise that the 10GBASE-KX4 has EEE capability 0 = Do not advertise that the 10GBASE-KX4 has EEE capability	0
08~19, 28~31	7.60.4	RO	1000BASE-KX EEE 1 = Advertise that the 1000BASE-KX has EEE capability 0 = Do not advertise that the 1000BASE-KX has EEE capability	0
08~19, 28~31	7.60.3	RO	10GBASE-T EEE 1 = Advertise that the 10GBASE-T has EEE capability 0 = Do not advertise that the 10GBASE-T has EEE capability	0
08~19, 28~31	7.60.2	RO	1000BASE-T EEE 1 = Advertise that the 1000BASE-T has EEE capability 0 = Do not advertise that the 1000BASE-T has EEE capability	0
08~19, 28~31	7.60.1	R/W	100BASE-TX EEE 1 = Advertise that the 100BASE-TX has EEE capability 0 = Do not advertise that the 100BASE-TX has EEE capability	1
08~19, 28~31	7.60.0	RO	Reserved Ignore when read	0

MMD register 7.61 of PHY08~19,28~31 (Each PHY has its own MMD register 7.61 with different PHY address)

PHY	MII	R/W	Description	Default
EEE link partner ability				
08~19, 28~31	7.61[15:7]	RO	Reserved Ignore when read	0
08~19, 28~31	7.61.6	RO	10GBASE-KR EEE 1 = Link partner is advertising EEE capability for 10GBASE-KR 0 = Link partner is not advertising EEE capability for 10GBASE-KR	0
08~19, 28~31	7.61.5	RO	10GBASE-KX4 EEE 1 = Link partner is advertising EEE capability for 10GBASE-KX4 0 = Link partner is not advertising EEE capability for	0
08~19, 28~31	7.61.4	RO	1000BASE-KX EEE 1 = Link partner is advertising EEE capability for 1000BASE-KX 0 = Link partner is not advertising EEE capability for 1000BASE-KX	0
08~19, 28~31	7.61.3	RO	10GBASE-T EEE 1 = Link partner is advertising EEE capability for 10GBASE-T 0 = Link partner is not advertising EEE capability for 10GBASE-T	0
08~19, 28~31	7.61.2	RO	1000BASE-T EEE 1 = Link partner is advertising EEE capability for 1000BASE-T 0 = Link partner is not advertising EEE capability for 1000BASE-T	0
08~19, 28~31	7.61.1	RO	100BASE-TX EEE 1 = Link partner is advertising EEE capability for 100BASE-TX 0 = Link partner is not advertising EEE capability for 100BASE-TX	0
08~19, 28~31	7.61.0	RO	Reserved Ignore when read	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

6.1.4 Register Page mode Control Register

MII register 20 of PHY08~19,28~31 (8 PHYs, 4 PHYs and 4 PHYs share the MII register)

PHY	MII	R/W	Description	Default
Page Control Register				
08~19, 28~31	20[4:0]	RW	Reg16~31_Page_Sel[4:0]	00000

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce unexpected function to write these registers.

6.1.5 WOL+ Control Register

MII page4 register16 of PHY08~19,28~31 (8 PHYs, 4 PHYs and 4 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL+ Control Register				
4	16.[15]	RW	WOL+ Interrupt Enable Set high to enable WOL+ interrupt 1=Enable 0=Disable Each PHY address can access the register of the corresponding port.	0
	16.[14]	RW	WOL+ Level Trigger This bit is used to select the output mode of WOL+ interrupt. 1=Level trigger (Low goes high or high goes low when WOL+ interrupt) 0=Edge trigger (Positive pulse or negative pulse when WOL+ interrupt)	1
	16.[13]	RW	WOL+ Positive Trigger This bit is used to select the polarity of WOL+ interrupt. 1=Low goes high or positive pulse 0=High goes low or negative pulse	0
	16.[12]	RW	Sense Link Change Set high to enable WOL+ interrupt when link change is sensing. 1=Enable 0=Disable WOL function will be disabled when both IP1819I WOL and PHY WOL settings are disabled.	1
	16.[11]	RW	Sense Magic Packet Set high to enable WOL+ interrupt when magic packet is receiving. 1=Enable 0=Disable	1
	16.[10]	RW	Sense Any Packet Set high to enable WOL+ interrupt when any packet is receiving. 1=Enable 0=Disable	1
	16.[9]	RW	Sense DUT Set high to enable WOL+ interrupt when DUT is sensing WOL+ event. 1=Enable 0=Disable Each PHY address can access the register of the corresponding port.	1
	16.[8]	RW	WOL+ Down Speed Enable Set high to enable WOL+ down speed function 1=Enable 0=Disable	1
	16.[7:1]	RO	Reserved	0x00

MII page4 register16 of PHY08~19,28~31 (8 PHYs, 4 PHYs and 4 PHYs share the MII register)

page	MII	R/W	Description	Default
	16.[0]	RO	PHY WOL+ Interrupt Status The status of PHY WOL+ interrupt is based on the setting of Reg16 Page4 bit14 and bit13. Each PHY address can access the register of the corresponding port.	1

MII page5 register16 of PHY08~19,28~31 (8 PHYs, 4 PHYs and 4 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL+ MAC Address Register 0				
5	16[15:0]	R/W	WOL+ MAC Address 0 (the most significant word) WOL+ MAC Address = {WOL+_MAC_Address_0, WOL+_MAC_Address_1, WOL+_MAC_Address_2}	0x0000

MII page5 register16 of PHY08~19,28~31 (8 PHYs, 4 PHYs and 4 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL+ MAC Address Register 1				
5	16[15:0]	R/W	WOL+ MAC Address 1 WOL+ MAC Address = {WOL+_MAC_Address_0, WOL+_MAC_Address_1, WOL+_MAC_Address_2}	0x0000

MII page5 register16 of PHY08~19,28~31 (8 PHYs, 4 PHYs and 4 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL+ MAC Address Register 2				
5	16[15:0]	R/W	WOL+ MAC Address 2 (the least significant word) WOL+ MAC Address = {WOL+_MAC_Address_0, WOL+_MAC_Address_1, WOL+_MAC_Address_2}	0x0000

Above three definitions are in the same register. Continuously write/read this register 3 times to set/obtain WOL Magic packet MAC address.

The first write/read : WOL+ MAC Address 0.

The second write/read : WOL+ MAC Address 1.

The third write/read : WOL+ MAC Address 2.

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

Example 1, Read page3 register16 (Read Data from page3 register16 of PHY address 0):

1. Write 0.20 = 0x0003 //page3
2. Read 0.16 //Read Data from page3 register16
3. Write 0.20 = 0x0000 //restore to page0

Example 2, Write page3 register16 = 0x3400 (Write Data 0x3400 to page3 register16 of PHY address 0):

1. Write 0.20 = 0x0003 //page3
2. Write 0.16 = 0x3400 //Write Data 0x3400 to page3 register16
3. Write 0.20 = 0x0000 //restore to page0

6.1.6 MDI/MDIX Control Register

MII register 23 of PHY8~19,28~31 (Each PHY has its own MII register 23 with different PHY address)

Page	MII	R/W	Description	Default
MDI/MDIX Control Register				
0	23[15:2]	RW	Reserved	0x0056
	23[1]	RW	Auto_MDIX 1 : Enable auto crossover function 0 : Disable auto crossover function	
	23[0]	RW	MDI/MDIX channel selection 1 : Select MDIX channel 0 : Select MDI channel	

6.1.7 10BaseT Control Register

MII register 23 of PHY8~19,28~31 (Each PHY has its own MII register 23 with different PHY address)

Page	MII	R/W	Description	Default
10BaseT Control Register				
1	23[15:4]	RW	Reserved	0x8000
	23[3]	RW	10BaseT selection 1 : Select 10BaseT 0 : Select 10BaseTe	
	23[2:0]	RW	Reserved	

6.2 Switch Register

6.2.1 Switch Page Map

Page	Description
0x00	<u>MAC control registers</u>
0x01	<u>ARL registers 1</u>
0x02	<u>ARL registers 2</u>
0x03	<u>SMI registers</u>
0x04	<u>OAM control registers</u>
0x05	Reserved
0x06	<u>RxDMA registers</u>
0x07	<u>TxDMA registers</u>
0x08	<u>Otp Qee registers</u>
0x09	<u>PTP registers</u>
0x0A	<u>IRMP registers</u>
0x0B	<u>Advanced EEPROM code registers</u>
0x0C	<u>Misc/System registers</u>
0x0D	Reserved

6.2.2 Switch Register Map

Type	Description
R	Read
W	Write
R/W	Read/Write
SC	Self-Clearing
RO	Read Only
LL	Latching Low
LH	Latching High

6.3 MAC Control Register

Table 34 MAC Control Register

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0x00	Switch ID/version register bit[3:0] : IP1819I IC version bit[15:4] : IP1819I ID	RO	0x8290
0x01	General MAC operation behavior register 1 bit[1:0] : Enable IPG compensation 00 : Disable 01 : compensation 160 ppm 10 : compensation 80 ppm 11 : compensation 40 ppm (default) bit[2] : Back pressure method 0 : Carrier Sense base 1 : Collision base bit[3] : Collision 16 times drop enable bit[4] : Collision back off enable bit[5] : Auto turn off flow control function if priority queue enable bit[6] : In-band management (Destination MAC address = switch MAC address) 0: Drop 1: to CPU port (switch MAC address define in offset address x5C, 0x5D, 0x5E) bit[7] : Disable TX packets CRC recalculation bit[8] : Bypass RX packets CRC error bit[9] : Enable for MIBs counters bit[10] : Port 17 interface select 0 : Reserved 1 : RGMII (default) bit[11] : Port 18 interface select 0 : Reserved 1 : RGMII (default) bit[13:12] : Reserved bit[14] : Port 19 interface select 0 : MII 1 : RGMII (default)	R/W	0x7C17
0x02	Jumbo Packets enable for port 1 ~ port 12, 1 bit per port bit[11:0] : enable jumbo 0 : Disable 1 : Enable	R/W	0x0000
0x03	Jumbo Packets enable for port 13 ~ port 19, 1 bit per port bit[12][9:4] : enable jumbo 0 : Disable 1 : Enable	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0x04	MAC LoopBack enable (MDI TX to RX) for port 1 ~ port 12 bit[11:0] : LoopBack enable 0 : Disable 1 : Enable	R/W	0x0000
0x05	MAC LoopBack enable (RGMII/MII TX to RX) for port 13 ~ port 19 bit[12][9:4]: LoopBack enable 0 : Disable 1 : Enable	R/W	0x0000
0x06	Ethernet L2 protocol frames capture (if 0x33 bit[8] is 1'b1, the BPDU capture should follow the 0x30 ~ 0x33 setting) bit[1:0] : for BPDU (01-80-C2-00-00-00) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[3:2] : for Slow Protocol (01-80-C2-00-00-02) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[5:4] : for 802.1X (01-80-C2-00-00-03) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[7:6] : for LLDP (01-80-C2-00-00-0E) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[9:8] : for Group 0 (01-80-C2-00-00-05, 06, 09 ~ 0C, 0F) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[11:10] : for All Bridge address (01-80-C2-00-00-10) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[13:12] : for Group 1 (01-80-C2-00-00-11 ~ 1F) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[15:14] : for GARP (01-80-C2-00-00-20, 21) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop	R/W	0x030C
0x07	Ethernet L2 protocol frames capture bit[1:0] : for Group 2 (01-80-C2-00-00-22 ~ 2F) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[3:2] : for Group 3 (01-80-C2-00-00-30 ~ 3F) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[4] : CPU does not act for drop setting for reserved group address as defined above. 0 : enable drop setting 1 : Disable drop setting bit[6:5] : Reserved bit[7] : ARP 0: Forward depend on DA 1: To DA and CPU	R/W	0x0040

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
	bit[8] : PPPoE protocol check enable 0 : Don't check PPPoE type 1 : Check PPPoE type bit[9] : PPPoE header remove 0 : Don't remove 1 : Remove bit[10] : IPv6 0 : Forward depend on DA 1 : To CPU port bit[11] : Pass Pause frame with DA not belong to Switch Address and 01-80-C2-00-00-01 0 : Drop 1 : Pass bit[12] : set (BPDU, 802.1x, Slow protocol, LLDP, GxRP) packets to highest priority if the corresponding protocol enable. 0 : Disable 1 : Enable bit[13] : Capture CFM packet to CPU 0 : Disable 1 : Enable bit[14] : Capture User define Ether Type (define in 0x23) 0 : Disable 1 : to DA and CPU bit[15] : Check if OAM frame DA equals to 0x01_80_C2_00_00_02 0 : can be unicast 1 : DA must be 0x01_80_C2_00_00_02		
0x08	Ethernet L3 protocol packet capture bit[1:0] : ICMP bit[3:2] : TCP bit[5:4] : UDP bit[7:6] : OSPF bit[9:8] : USR1 (0x09 low byte) bit[11:10] : USR2 (0x09 high byte) bit[13:12] : Ipv4 Other protocol, 00 : Send to ports only 01 : Send to CPU and ports 10 : Send to CPU only 11 : Drop	R/W	0x0000
0x09	User define IP protocol field bit[7:0] : IP protocol USR1 bit[15:8] : IP protocol USR2	R/W	0x0000
0x0A	User define TCP/UDP port number A	R/W	0x0000
0x0B	User define TCP/UDP port number B	R/W	0x0000
0x0C	User define TCP/UDP port number C upper range setting	R/W	0x0000
0x0D	User define TCP/UDP port number C lower range setting IP1819I will check if the port number C is in the following range lower range <= port number C <= upper range	R/W	0x0000
0x0E	User define TCP/UDP port number D upper range setting	R/W	0x0000

MAC Control Registers : Page 0x00				
Reg Addr.	Register Description		R/W	Default value
0x0F	User define TCP/UDP port number D lower range setting IP1819I will check if the port number D is in the following range lower range <= port number D <= upper range		R/W	0x0000
0x10	User define TCP/UDP port number E upper range setting		R/W	0x0000
0x11	User define TCP/UDP port number E lower range setting IP1819I will check if the port number E is in the following range lower range <= port number E <= upper range		R/W	0x0000
0x12	TCP/UDP port number based priority setting: bit[3:0]: FTP (20,21) bit[7:4]: SSH (22) bit[11:8]: TELNET (23) bit[15:12]: SMTP (25)	0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x13	TCP/UDP port number based priority setting: bit[3:0]: DNS (53) bit[7:4]: BOOTP/DHCP (67, 68) bit[11:8]: TFTP (69) bit[15:12]: HTTP_0,1 (80)	0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x14	TCP/UDP port number based priority setting: bit[3:0]: POP3 (110) bit[7:4]: NEWS (119) bit[11:8]: SNTP (123) bit[15:12]: NETBIOS0,1,2 (137 ~ 139)	0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x15	TCP/UDP port number based priority setting: bit[3:0]: IMAP_0,1 (143,220) bit[7:4]: SNMP_0,1 (161,162) bit[11:8]: HTTPS (443) bit[15:12]: USR define A	0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x16	TCP/UDP port number based priority setting: bit[3:0]: USR define B bit[7:4]: USR define C bit[11:8]: USR define D bit[15:12]: USR define E	0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x17	TCP/UDP port number based filter to WAN port select: bit[0]: FTP 0: Don't care 1: select bit[1]: SSH 0: Don't care 1: select bit[2]: TELNET 0: Don't care 1: select bit[3]: SMTP 0: Don't care 1: select bit[4]: DNS 0: Don't care 1: select bit[5]: BOOP/DHCP 0: Don't care 1: select bit[6]: TFTP 0: Don't care 1: select bit[7]: HTTP_0,1 0: Don't care 1: select		R/W	0x0000

MAC Control Registers : Page 0x00				
Reg Addr.	Register Description		R/W	Default value
	bit[8]: POP3 bit[9]: NEWS bit[10]: SNTP bit[11]: NETBIOS0,1,2 bit[12]: IMAP_0,1 bit[13]: SNMP_0,1, bit[14]: HTTPS bit[15]: USR define A	0: Don't care 1: select 0: Don't care 1: select 0: Don't care 1: select 0: Don't care 1: select 0: Don't care 1: select 0: Don't care 1: select 0: Don't care 1: select		
	(corresponding to offset address 0x12 ~ 0x16)			
0x18	TCP/UDP port number based filter to WAN port select: bit[0]: USR define B bit[1]: USR define C bit[2]: USR define D bit[3]: USR define E bit[4]: filter_md (0: negative list 1: positive list) 0 : negative list, the setting "1"s above which routed to wan will be filtered 1 : positive list, the setting "1"s above which routed to wan port can be passed, otherwise be filtered (bit[4] : Detail ref to offset address 0x0D~0x10 (page6))	0: Don't care 1: select 0: Don't care 1: select 0: Don't care 1: select 0: Don't care 1: select	R/W	0x00
0x19	TCP/UDP Port Number function enable for port 1 ~ port 12, 1 bit per port	bit[11:0] : function enable for Port 1 ~ Port 12 0 : Disable 1 : Enable	R/W	0x0000
0x1A	TCP/UDP Port Number function enable for port 13 ~ port 19, 1 bit per port	bit[12][9:4] : function enable for Port 13 ~ Port 19 0 : Disable 1 : Enable	R/W	0x0000
0x1B	TCP/UDP Port Number priority enable for port 1 ~ port 12, 1 bit per port	bit[11:0] : priority enable for Port 1 ~ Port 12 0 : Disable 1 : Enable	R/W	0x0000
0x1C	TCP/UDP Port Number priority enable for port 13 ~ port 19, 1-bit /port	bit[12][9:4] : priority enable for Port 13 ~ Port 19 0 : Disable 1 : Enable	R/W	0x0000
0x1D	TCP/UDP Port Number check for "TCP protocol" enable	bit[15:0] : enable the TCP/UDP Port Number Function for "TCP protocol" 0 : Disable 1 : Enable The Port Number Mapping is the same as define in 0x17	R/W	0xFFFF
0x1E	TCP/UDP Port Number check for "TCP protocol" enable	bit[3:0] : enable the TCP/UDP Port Number Function for "TCP protocol" 0 : Disable 1 : Enable The Port Number Mapping is the same as define in 0x18	R/W	0xF

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0x1F	TCP/UDP Port Number check for "UDP protocol" enable bit[15:0] : enable the TCP/UDP Port Number Function for "UDP protocol" 0 : Disable 1 : Enable The Port Number Mapping is the same as define in 0x17	R/W	0xFFFF
0x20	TCP/UDP Port Number check for "UDP protocol" enable bit[3:0] : enable the TCP/UDP Port Number Function for "UDP protocol" 0 : Disable 1 : Enable The Port Number Mapping is the same as define in 0x18	R/W	0xF
0x21	In-band management restriction configuration 1 When the register 0x01 bit[6] and 0x22 bit[15] are both 1'b1, the in-band Management packets will forward as the register 0x21 and 0x22 settings. bit[0] : ARP bit[1] : IPv4 bit[2] : IPv6 bit[3] : PPPoE bit[4] : ICMP bit[5] : TCP bit[6] : UDP bit[7] : User define Ether Type bit[8] : User define IP Protocol 1 bit[9] : User define IP Protocol 2 bit[10] : ICMPv6 bit[11] : FTP bit[12] : SSH bit[13] : Telnet bit[14] : SMTP bit[15] : DNS 0 : drop 1 : forward to CPU	R/W	0x0000
0x22	In-band management restriction configuration 2 bit[0] : BOOTP/DHCP bit[1] : TFTP bit[2] : HTTP bit[3] : POP3 bit[4] : NEWS bit[5] : SNTP bit[6] : NETBIOS bit[7] : IMAP bit[8] : SNMP bit[9] : HTTPS bit[10] : user define TCP/UDP Port Number A bit[11] : user define TCP/UDP Port Number B bit[12] : user define TCP/UDP Port Number C bit[13] : user define TCP/UDP Port Number D bit[14] : user define TCP/UDP Port Number E 0 : drop 1 : forward to CPU bit[15] : in-band management restriction enable (0x01 bit[6] need to be 1'b1) 0 : Disable 1 : Enable	R/W	0x0000
0x23	User define Ether Type bit[15:0] : user define Ether Type Value	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0x24 ~ 0x2F	Reserved		
0x30	BPDU per Port Capture configuration for port 1 ~ port 8 bit[1:0] : Port 1 BPDU setting bit[3:2] : Port 2 BPDU setting bit[5:4] : Port 3 BPDU setting bit[7:6] : Port 4 BPDU setting bit[9:8] : Port 5 BPDU setting bit[11:10] : Port 6 BPDU setting bit[13:12] : Port 7 BPDU setting bit[15:14] : Port 8 BPDU setting 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop	R/W	0x0000
0x31	BPDU per Port Capture configuration for port 9 ~ port 12 bit[7:0] : BPDU setting for port 9 ~ port 12 bit[15:8] : Reserved	R/W	0x0000
0x32	BPDU per Port Capture configuration for port 13 ~ port 16 bit[7:0] : Reserved bit[15:8] : BPDU setting for port 13 ~ port 16	R/W	0x0000
0x33	BPDU per Port Capture configuration for port 17 ~ port 18 bit[3:0] : BPDU setting for port 17 ~ port 18 bit[7:4] : Reserved bit[8] : BPDU per Port setting enable	R/W	0x0000
0x34 ~ 0x39	Reserved		
0x3A	Port based priority enable for port 1 ~ port 5, 3 bit per port bit[2:0] : port based priority setting for port 1 000 – to queue 0 (lowest priority) 001 – to queue 1 ... 111 – to queue 7 (highest priority) bit[5:3] : port 2 bit[8:6] : port 3 bit[11:9] : port 4 bit[14:12] : port 5	R/W	0x0000
0x3B	Port based priority enable for port 6 ~ port 10, 3 bit per port	R/W	0x0000
0x3C	Port based priority enable for port 11 ~ port 12, 3 bit per port bit[5:0] : port based priority setting for port 11 ~ port 12 bit[15:6] : Reserved	R/W	0x0000
0x3D	Reserved	R/W	0x0000
0x3E	Port based priority enable for port 13 ~ port 17, 3 bit per port	R/W	0x0000
0x3F	Port based priority enable for port 18 ~ port 19, 3 bit per port bit[2:0] : port based priority setting for port 18 bit[8:3] : Reserved bit[11:9] : port based priority setting for port 19	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0x40	Tag based priority settings bit[11:0] : enable 802.1Q tag priority for port 1 ~ port 12, 1 bit per port	R/W	0x0000
0x41	Tag based priority settings bit[12][9:4] : enable 802.1Q tag priority for port 13 ~ port 19, 1 bit per port bit[13] : enable special tag priority for CPU Port (port 19) bit[14] : 802.1Q tag priority Edition select 0 : 2005 Edition 1 : earlier Edition bit[15] : exchange the priority of 3'b000 and 3'b001 for 2005 Edition	R/W	0x0000
0x42	IP CoS based priority enable bit[11:0]: IP CoS based priority enable for port 1 ~ port 12, 1 bit per port	R/W	0x0000
0x43	IP CoS based priority enable bit[12][9:4]: IP CoS based priority enable for port 13 ~ port 19. 1 bit per port	R/W	0x0000
0x44	Differentiated Services (DS) priority setting bit[2:0]: priority setting for DSCP 0 bit[5:3]: priority setting for DSCP 1 bit[8:6]: priority setting for DSCP 2 bit[11:9]: priority setting for DSCP 3 bit[14:12]: priority setting for DSCP 4	R/W	0x7FFF
0x45	Differentiated Services (DS) priority setting bit[2:0]: priority setting for DSCP 5 bit[5:3]: priority setting for DSCP 6 bit[8:6]: priority setting for DSCP 7 bit[9] : priority for DSCP not match 0 : regard as low priority (priority 0) 1 : ignore IP priority (priority will according to tag/port)	R/W	0x3FF
0x46	DSCP configuration for DSCP_0 and DSCP_1 bit[5:0]: DSCP 0 configuration bit[11:6]: DSCP 1 configuration	R/W	0x280
0x47	DSCP configuration for DSCP_2 and DSCP_3 bit[5:0]: DSCP 2 configuration bit[11:6]: DSCP 3 configuration	R/W	0x692
0x48	DSCP configuration for DSCP_4 and DSCP_5 bit[5:0]: DSCP 4 configuration bit[11:6]: DSCP 5 configuration	R/W	0xBA2
0x49	DSCP configuration for DSCP_6 and DSCP_7 bit[5:0]: DSCP 6 configuration bit[11:6]: DSCP 7 configuration	R/W	0xE30
0x4A	Source MAC address based priority setting bit[11:0] : SMAC priority enable for port 1~ port 12	R/W	0x0000
0x4B	Source MAC address based priority setting bit[12][9:4] : SMAC priority enable for port 13 ~ port 19	R/W	0x0000
0x4C	VID based priority enable setting bit[11:0] : VID priority enable for port 1 ~ port 12	R/W	0x0000
0x4D	VID based priority enable setting bit[12][9:4] : VID priority enable for port 13 ~ port 19	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0x4E	IP based priority setting bit[11:0] : IP priority enable for port 1 ~ port 12 (ref Page 0x02, reg 0x01, 0x02)	R/W	0x0000
0x4F	IP based priority setting bit[12][9:4] : IP priority enable for port 13 ~ port 19 (ref Page 0x02, reg 0x01, 0x02)	R/W	0x0000
0x50	IGMP Multicast Group based priority enable setting bit[11:0] : IGMP Multicast Group priority enable for port 1 ~ port 12	R/W	0x0000
0x51	IGMP Multicast Group based priority enable setting bit[12][9:4] : IGMP Multicast Group priority enable for port 13 ~ port 19	R/W	0x0000
0x52	ACL based priority enable setting bit[11:0] : ACL priority enable for port 1 ~ port 12	R/W	0x0000
0x53	ACL based priority enable setting bit[12][9:4] : ACL priority enable for port 13 ~ port 19	R/W	0x0000
0x54	802.1x Port Lock Enable (port 1 ~ port 12) bit[11:0]: 0 : normal operation 1 : drop all frames except ARP & 802.1x EAPOL packet	R/W	0x0000
0x55	802.1x Port Lock Enable (port 13 ~ port 19) bit[12][9:4]: 0 : normal operation 1 : drop all frames except ARP & 802.1x EAPOL packet	R/W	0x0000
0x56	PPPoE session ID A	R/W	0x0000
0x57	PPPoE session ID B	R/W	0x0000
0x58	PPPoE session ID C	R/W	0x0000
0x59	PPPoE session ID D	R/W	0x0000
0x5A	MAC reset for port 1 ~ port 12, 1 bit per port bit[11:0] : 0: reset 1: normal	R/W	0xFFFF
0x5B	MAC reset for port 13 ~ port 19, 1 bit per port bit[12][9:4] : 0: reset 1: normal	R/W	0x1FFF
0x5C	Switch's MAC address[15:0]	R/W	0x0003
0x5D	Switch's MAC address[31:16]	R/W	0xC300
0x5E	Switch's MAC address[47:32]	R/W	0x0090
0x5F	Configuration for Low Power Idle bit[4:0] : threshold of IDLE period for entering LPI bit[7:5] : the interval selection for IDLE counter 0 ~ 7 – 1us/10us/100us/ 1ms/ 10ms/ 100ms/ 1s/ 10s bit[8] : Switch enter PSS when IDLE period hit the threshold 0 : Disable 1 : Enable bit[9] : use default Tw as the resolved Tw 0 : Disable 1 : Enable bit[10] : use LinkPartner's Tw as the resolved Tw (note : bit[9] has higher priority than this bit) 0 : Disable 1 : Enable bit[11] : Reserved	R/W	0x820F

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
	bit[12] : select the large one between default Tw and LinkPartner's Tw as the resolved Tw 0 : Disable 1 : Enable bit[13] : force to enable PSS support 0 : Disable 1 : Enable bit[14] : Reserved. Should be 1'b0. bit[15] : Reserved. Should be 1'b1.		
0x60	Configuration of the LPI State for port 1 ~ port 12, per port 1 bit bit[11:0] : LPI state for each port 0 : normal state 1 : in LPI State	R/W	0x0000
0x61	Configuration of the LPI State for port 13 ~ port 19, per port 1 bit bit[12][9:4] : LPI state for each port 0 : normal state 1 : in LPI State	R/W	0x0000
0x62	Configuration for LPI default Tw for 10/100 Mbps bit[15:0] : default Tw setting in us	R/W	0x0023
0x63	Configuration LPI default Tw for giga speed bit[15:0] : default Tw setting in us	R/W	0x0011
0x64	CPU Read statistic counter command bit[4:0] : statistic counter read address (R : ~0x17, T : ~0x13) bit[9:5] : statistic counter Port select (port 1 ~ port 19 : 0~11,20~25,28) bit[10] : statistic counter RX/TX selection 0 : RX 1 : TX bit[11] : statistic counter sequential read enable 0 : Disable 1 : Enable bit[12] : Reserved bit[14] : statistic counter read clear enable 0 : Disable 1 : Enable bit[15] : statistic counter command trig/Ack	R/W	0x0000
0x65	CPU Read low 16 bits statistic counter data	R/W	0x0000
0x66	CPU Read high 16 bits statistic counter data	R/W	0x0000
0x67	MAC self test packets control setting bit[11:0] : send self test packet for port 1 ~ port 12, per port 1 bit 0 : do not send 1 : send	R/W	0x0000
0x68	MAC self test packets control setting bit[12][9:4] : send self test packet for port 13 ~ port 19, per port 1 bit 0 : do not send 1 : send bit[14:13] : setting for self test packets number 00 : 32768 01 : 4096 10 : 256 11 : 16	R/W	0x0000
0x69	MAC self test result bit[11:0] : self test result for port 1 ~ port 12, per port 1 bit 0 : fail 1 : pass	RO	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0x6A	MAC self test result bit[12][9:4] : self test result for port 13 ~ port 19, per port 1 bit 0 : fail 1 : pass	RO	0x0000
0x6B	LoopDetect config register bit[11:0] : loop detect enable for port 1 ~ port 12, per port 1 bit 0 : Disable 1 : Enable	R/W	0x0000
0x6C	LoopDetect config register bit[12][9:4] : loop detect enable for port 13 ~ port 19, per port 1 bit 0 : Disable 1 : Enable bit[13] : loop detect time unit select 0 : 500ms 1 : 10s bit[14] : setting LoopDetect SA[40] value bit[15] : setting for LoopDetect re-random 0 : Disable 1 : Enable PS. To block loop port, Page 0x01, register 0x24 bit[3] need to be 1'b1	R/W	0xC000
0x6D	LoopDetect timer bit[7:0] : LPD packet sending timer, the time interval is timer x time unit bit[15:8] : Block release timer, the time interval is timer x time unit	R/W	0x0903
0x6E	LoopDetect frame DA[15:0] setting bit[15:0] : setting for LPD frame DA[15:0]	R/W	0x0000
0x6F	LoopDetect frame DA[31:16] setting bit[15:0] : setting for LPD frame DA[31:16]	R/W	0xC300
0x70	LoopDetect frame DA[47:32] setting bit[15:0] : setting for LPD frame DA[47:32]	R/W	0x0190
0x71	LoopDetect frame EtherType setting bit[15:0] : setting for LPD frame EtherType	R/W	0x8931
0x72	LoopDetect frame sub type setting bit[15:0] : setting for LPD frame sub type	R/W	0xFFFF
0x73	LoopDetect frame Device ID setting bit[7:0] : setting for LPD frame device ID	R/W	0x05
0x74	TCP flag global configuration bit[0] : Drop null flag 0 : Disable 1 : Enable bit[1] : Drop ALL-Set flag 0 : Disable 1 : Enable bit[3:2] : Period selection for Flag storm control counter 00 : 1000 / 100 / 10 Mbps -> 200us / 2ms / 20ms 01 : 1000 / 100 / 10 Mbps -> 1ms / 10ms / 100ms 10 : 1000 / 100 / 10 Mbps -> 10ms / 10ms / 10ms 11 : 1000 / 100 / 10 Mbps -> 100ms / 100ms / 100ms	R/W	0x0
0x75	TCP flag 0 configuration bit[7:0] : The TCP flag 0 configuration bit[10:8] : Priority setting for TCP flag 0 bit[11] : Priority setting enable for TCP flag 0 0 : Disable 1 : Enable	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
	bit[13:12] : action for TCP flag 0 00 : none 01 : storm control 10 : to CPU only 11 : drop bit[14] : reserved, should be 1'b0		
0x76	TCP flag 1 configuration bit[7:0] : The TCP flag 1 configuration bit[10:8] : Priority setting for TCP flag 1 bit[11] : Priority setting enable for TCP flag 1 0 : Disable 1 Enable bit[13:12] : action for TCP flag 1 00 : none 01 : storm control 10 : to CPU only 11 : drop bit[14] : reserved, should be 1'b0	R/W	0x0000
0x77	TCP flag 2 configuration bit[7:0] : The TCP flag 2 configuration bit[10:8] : Priority setting for TCP flag 2 bit[11] : Priority setting enable for TCP flag 2 0 : Disable 1 Enable bit[13:12] : action for TCP flag 2 00 : none 01 : storm control 10 : to CPU only 11 : drop bit[14] : reserved, should be 1'b0	R/W	0x0000
0x78	TCP flag 3 configuration bit[7:0] : The TCP flag 3 configuration bit[10:8] : Priority setting for TCP flag 3 bit[11] : Priority setting enable for TCP flag 3 0 : Disable 1 Enable bit[13:12] : action for TCP flag 3 00 : none 01 : storm control 10 : to CPU only 11 : drop bit[14] : reserved, should be 1'b0	R/W	0x0000
0x79	TCP flag0 and flag1 storm control threshold setting bit[7:0] : threshold setting for TCP flag 0 bit[15:8] : threshold setting for TCP flag 1	R/W	0x0000
0x7A	TCP flag2 and flag3 storm control threshold setting bit[7:0] : threshold setting for TCP flag 2 bit[15:8] : threshold setting for TCP flag 3	R/W	0x0000
0x7B	TCP flag 0 related function enable for port 1 ~ port 12 bit[11:0] : enable for TCP flag 0 related function 0 : Disable 1 : Enable	R/W	0x0000
0x7C	TCP flag 0 related function enable for port 13 ~ port 19 bit[12][9:4] : enable for TCP flag 0 related function 0 : Disable 1 : Enable	R/W	0x0000
0x7D	TCP flag 1 related function enable for port 1 ~ port 12 bit[11:0] : enable for TCP flag 1 related function 0 : Disable 1 : Enable	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0x7E	TCP flag 1 related function enable for port 13 ~ port 19 bit[12][9:4] : enable for TCP flag 1 related function 0 : Disable 1 : Enable	R/W	0x0000
0x7F	TCP flag 2 related function enable for port 1 ~ port 12 bit[11:0] : enable for TCP flag 2 related function 0 : Disable 1 : Enable	R/W	0x0000
0x80	TCP flag 2 related function enable for port 13 ~ port 19 bit[12][9:4] : enable for TCP flag 2 related function 0 : Disable 1 : Enable	R/W	0x0000
0x81	TCP flag 3 related function enable for port 1 ~ port 12 bit[11:0] : enable for TCP flag 3 related function 0 : Disable 1 : Enable	R/W	0x0000
0x82	TCP flag 3 related function enable for port 13 ~ port 19 bit[12][9:4] : enable for TCP flag 3 related function 0 : Disable 1 : Enable	R/W	0x0000
0x83	EoC configuration 1 bit[11:0] : EoC function enable for port 1 ~ port 12	R/W	0x0000
0x84	EoC configuration 2 bit[12][9:4] : EoC function enable for port 13 ~ port 19 bit[13] : Clear EoC block when receive a good packet bit[14] : EoC release time selection 0 : 1 Minute 1 : 10 Minutes bit[15] : Force to clear all EoC block (this bit will be self clear) PS. To block loop port, Page 0x01, register 0x24 bit[3] need to be 1'b1	R/W	0x0000
0x85	EoC block status for port 1 ~ port 12 bit[11:0] : block status check for port 1 ~ port 12 0 : normal 1 : loop detected	RO	0x0000
0x86	EoC block status for port 13 ~ port 19 bit[12][9:4] : block status check for port 13 ~ port 19 0 : normal 1 : loop detected	RO	0x0000
0x87	Ingress Rate control for port 1 bit[13:0] : Input Rate control The bandwidth = Rate control configure value x 64k bps	R/W	0x0000
0x88 ~ 0x92	Ingress Rate control for port 2 ~ port 12 bit[13:0] : Input Rate control	R/W	0x0000
0x93 ~ 0x9A	Reserved		
0x9B ~ 0xA0	Ingress Rate control for port 13 ~ port 18 bit[13:0] : Input Rate control	R/W	0x0000
0xA1 0xA2	Reserved		

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0xA3	Ingress Rate control for port 19 bit[13:0] : Input Rate control	R/W	0x0000
0xA4	Configuration for PTP bit[0] : PTP protocol enable (packets will to CPU only) bit[1] : PTP config for DA = 01-1B-19-00-00-00 0 : Enable 1 : not regard as PTP bit[2] : PTP config for DA = 01-80-C2-00-00-0E 0 : Enable 1 : not regard as PTP bit[3] : PTP config for UDP Destination Port 0 : Enable 1 : not check for PTP bit[4] : PTP config for UDP Source Port 0 : Enable 1 : not check as PTP bit[5] : Disable PTP packet send to CPU only 0 : to CPU only 1 : forward as DA specific bit[6] : Also check NTP packet 0 : Disable 1 : Enable bit[7] : PTP packets regard as high priority 0 : Disable 1 : Enable bit[8] : Allow PTP packets with unicast DA 0 : Disable 1 : Enable bit[9] : Check if Destination IP equal to 224.0.1.129 or 224.0.0.107 (if enable, the UDP port number must also match) 0 : Disable 1 : Enable	R/W	0x0000
0xA5	LoopDetect port 1 ~ port 12 status bit[11:0] : port status for port 1 ~ port 12 0 : normal 1 : loop detected	R	0x0000
0xA6	LoopDetect port 13 ~ port 19 status bit[12][9:4] : port status for port 13 ~ port 19 0 : normal 1 : loop detected	R	0x0000
0xA7	IPv6 related functions configuration bit[0] : Enable TCP/UDP Port Number related functions for IPv6 0 : Disable 1 : Enable bit[1] : Enable TCP/UDP flag related functions for IPv6 (bit[0] need 1'b1) 0 : Disable 1 : Enable bit[2] : Reserved, should be 1'b0. bit[3] : stop finding next header at Auth header bit[4] : stop finding next header at Encapsulation header bit[5] : stop finding next header at Fragment header bit[6] : stop finding next header at user define next header 1 bit[7] : stop finding next header at user define next header 2 0 : Enable 1 : Disable bit[8] : forwarding action "Send to CPU and ports" has higher priority than "Drop" 0 : Disable 1 : Enable bit[9] : forwarding action "Send to CPU only" has higher priority than "Drop" 0 : Disable 1 : Enable	R/W	0x003

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
0xA8	IPv6 related header forwarding bit[1:0] : Fragment header bit[3:2] : Encapsulation header bit[5:4] : Authentication header bit[7:6] : ICMPv6 header bit[9:8] : ICMPv6 MLD bit[11:10] : ICMPv6 NDP bit[13:12] : user define next header 1 bit[15:14] : user define next header 2 00 : Send to ports only 01 : Send to CPU and ports 10 : Send to CPU only 11 : Drop	R/W	0x0000
0xA9	IPv6 related header forwarding bit[1:0] : ICMPv6 user define type 1 bit[3:2] : ICMPv6 user define type 2 00 : Send to ports only 01 : Send to CPU and ports 10 : Send to CPU only 11 : Drop	R/W	0x0
0xAA	IPv6 user define next header configuration bit[7:0] : user define next header 1 bit[15:8] : user define next header 2	R/W	0x0000
0xAB	ICMPv6 user define type 1 setting bit[7:0] : lower range setting bit[15:8] : upper range setting	R/W	0x0000
0xAC	ICMPv6 user define type 2 setting bit[7:0] : lower range setting bit[15:8] : upper range setting	R/W	0x0000
0xAD	WOL+ Enable for TX enter saving mode bit[11:0] : WOL+ Enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0xAE	WOL+ enable for TX enter saving mode bit[12][9:4] : WOL+ enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000
0xAF	WOL+ configuration bit[4:0] : threshold of idle period for entering WOL+ saving mode (if giga port is enable for this function, the threshold should be greater than 30s) bit[6:5] : the interval selection for WOL+ idle counter 00 : Disable 01 : 10 s 10 : 1min 11 : 10 min bit[7] : if TX any packet, leave WOL+ mode or not 0 : leave 1 : Don't care bit[8] : if RX any packet, leave WOL+ mode or not 0 : leave 1 : Don't care	R/W	0x000

MAC Control Registers : Page 0x00			
Reg Addr.	Register Description	R/W	Default value
	bit[9] : WOL+ mode select 0 : slave 1 : master bit[10] : leave WOL+ mode if match ACL action : also to CPU 0 : Disable 1 : Enable bit[11] : Enable Interrupt to CPU 0 : Disable 1 : Enable		
0xB0	WOL+ mode control for port 1 ~ port 12 bit[11:0] : WOL+ active for port 1 ~ port 12 0 : normal 1 : enter WOL+ mode	R/W	0x0000
0xB1	WOL+ mode control for port 13 ~ port 19 bit[12][9:4] : WOL+ active for port 13 ~ port 19 0 : normal 1 : enter WOL+ mode	R/W	0x0000
0xB2	WOL+ event for port 1 ~ port 12 bit[11:0] : Indicate the port had entered WOL+ mode, read clear 0 : normal 1 : had entered WOL+ mode	RO	0x0000
0xB3	WOL+ event for port 13 ~ port 19 bit[12][9:4] : Indicate the port had entered WOL+ mode, read clear 0 : normal 1 : had entered WOL+ mode	RO	0x0000
0xB4	Reserved		
0xB5	Ethernet L2 protocol frames capture bit[1:0] : for 01-80-C2-00-00-04 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[3:2] : for 01-80-C2-00-00-07 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[5:4] : for 01-80-C2-00-00-08 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[7:6] : for 01-80-C2-00-00-0D 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop	R/W	0xFF
0xB6	Reserved		
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.4 ARL Control Register Page 1

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
0x01	LUT Aging timer setting bit[14:0] : Aging timer, the aging time is about : (mg_aging_time + 1) x 55.3 sec. ±3.8% bit[15] : Aging timer disable 0 : Enable 1 : Disable	R/W	0x0005
0x02	Source MAC address learning configure bit[1:0] : LUT learning mode 00 : overwrite L1/L2 according to the aging time 01, 10 : never overwrite before aging out 11 : only L2 will overwrite before aging out bit[2] : learning for null SA. 0 : Don't learn 1: learn. bit[3] : Hashing algorithm selection 0 : Direct hashing 1 : CRC hashing bit[4] : Disable forward unknown SA frame to CPU port 0 : forward 1 : not forward bit[5] : forward unknown SA frame if source address learning function is disable 0 : drop the unknown SA frame 1 : forward the unknown SA frame bit[6] : indicates the SA of input frame should match the original learn port or not 0 : SA will not bind the port 1 : SA will bind to the original learned port bit[7] : Learning SA or not when Packet drop by VLAN ingress check 0 : Learning 1 : not Learning	R/W	0x2C
0x03	Source MAC address learning enable for port 1 ~ port 12 bit[11:0] : Learning enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0xFFFF
0x04	Source MAC address learning Enable for port 13 ~ port 19 bit[12][9:4] : Learning Enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x1FFF
0x05	Source MAC address learning count control enable for port 1 ~ port 12 bit[11:0] : learning count control enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0x06	Source MAC address learning count control enable for port 13 ~ port 19 bit[12][9:4] : learning count control enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000
0x07	Source MAC address learning count control threshold setting bit[8:0] : learning count control threshold	R/W	0x000

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
0x08 ~ 0x0C	Reserved		
0x0D	Broadcast storm control configuration bit[7:0] : Broadcast storm control threshold bit[9:8] : Broadcast storm counter clear period selection 00 : 200 us / 2ms / 20ms for (Giga/100/10) 01 : 1 ms / 10ms / 100ms for (Giga/100/10) 10 : 10 ms / 10ms / 10ms for (Giga/100/10) 11 : 100 ms / 100ms / 100ms for (Giga/100/10) bit[10] : Block Broadcast/Multicast to CPU Enable 0 : Disable 1 : Enable bit[11] : Don't block bcst/Mcst Ipv4/IPv6 packets when bit[10] is enable 0 : block 1 : Don't block bit[12] : ignore 01:00:5E:xx:xx:xx for Mcst storm 0 : Don't ignore 1 : Ignore	R/W	0x01FF
0x0E	Broadcast storm control enable for port 1 ~ port 12 bit[11:0] : Broadcast storm control enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0x0F	Broadcast storm control enable for port 13 ~ port 19 bit[12][9:4] : Broadcast storm control enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000
0x10	Multicast storm control enable for port 1 ~ port 12 (share the same threshold with broadcast storm control) bit[11:0] : Multicast storm control enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0x11	Multicast storm control enable for port 13 ~ port 19 (share the same threshold with broadcast storm control) bit[12][9:4] : Multicast storm control enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000
0x12	DLF storm control enable for port 1 ~ port 12 (share the same threshold with broadcast storm control) bit[11:0] : DLF storm control enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0x13	DLF storm control enable for port 13 ~ port 19 (share the same threshold with broadcast storm control) bit[12][9:4] : DLF storm control enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000
0x14	ARP storm control configuration bit[7:0] : ARP storm control threshold bit[9:8] : ARP storm counter clear period selection 00 : 200 us / 2ms / 20ms for (Giga/100/10) 01 : 1 ms / 10ms / 100ms for (Giga/100/10) 10 : 10 ms / 10ms / 10ms for (Giga/100/10) 11 : 100 ms / 100ms / 100ms for (Giga/100/10)	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
	bit[10] : Blocked ARP frame forward to CPU 0 : Disable 1 : Enable bit[11] : ARP storm drop interrupt enable		
0x15	ARP storm control enable for port 1 ~ port 12 bit[11:0] : ARP storm control enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0x16	ARP storm control enable for port 13 ~ port 19 bit[12][9:4] : ARP storm control enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000
0x17	ICMP storm control configuration bit[7:0] : ICMP storm control threshold bit[9:8] : ICMP storm counter clear period selection 00 : 200 us / 2ms / 20ms for (Giga/100/10) 01 : 1 ms / 10ms / 100ms for (Giga/100/10) 10 : 10 ms / 10ms / 10ms for (Giga/100/10) 11 : 100 ms / 100ms / 100ms for (Giga/100/10) bit[10] : ICMP storm drop interrupt enable	R/W	0x0000
0x18	ICMP storm control enable for port 1 ~ port 12 bit[11:0] : ICMP storm control enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0x19	ICMP storm control enable for port 13 ~ port 19 bit[12][9:4] : ICMP storm control enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000
0x1A	Port based address flush configuration bit[11:0] : indicates that these addresses learnt by selected port should be flushed for port 1 ~ port 12 0 : Don't flush 1 : flush	R/W	0x0000
0x1B	Port based address flush configuration bit[12][9:4] : indicates that these addresses learnt by selected port should be flushed for port 13 ~ port 19 0 : Don't flush 1 : flush bit[13] : flush command trig	R/W	0x0000
0x1C	Trunk operation / Group configuration bit[2:0] : Trunk load balance hashing method selection 000 : Port ID 100 : DIP 001 : SA 101 : SIP 010 : DA 110 : TCP/UDP DP 011 : DA/SA 111 : TCP/UDP SP bit[3] : Trunk hashing method sequence enable 0 : Disable 1 : Enable bit[4] : CPU route function Don't care Trunk and VLAN result bit[5] : combine Trunk Group A and Group B into one Trunk bit[7:6] : Reserved bit[11:8] : Trunk Group A configuration (port 1 ~ port 4) 0 : not in trunk 1 : in trunk	R/W	0x0000

ARL Registers : Page 0x01

Reg Addr.	Register Description	R/W	Default value
	bit[15:12] : Trunk Group B configuration (port 5 ~ port 8) 0 : not in trunk 1 : in trunk		
0x1D	Trunk group configuration bit[3:0] : Trunk Group C configuration (port 9 ~ port 12) 0 : not in trunk 1 : in trunk bit[7:4] : Reserved bit[9:8] : Trunk Group D configuration (port 17 ~ port 18) 0 : not in trunk 1 : in trunk	R/W	0x000
0x1E	First Sniffer destination port group configuration bit[11:0] : select destination configuration for port 1 ~ port 12 0 : none 1 : selected	R/W	0x0000
0x1F	First Sniffer destination port group configuration bit[12][9:4] : select destination configuration for port 13 ~ port 19 0 : none 1 : selected bit[14:13] : sniffer method 00: Disable 01 : egress 10: ingress 11 : ingress+egress bit[15] : Tag/Untag setting for sniffed packet 0 : according to other criteria 1 : keep the original packet	R/W	0x0000
0x20	Second Sniffer destination port group configuration (only work for LUT/ACL/IGMP) bit[11:0] : select destination configuration for port 1 ~ port 12 0 : none 1 : selected	R/W	0x0000
0x21	Second Sniffer destination port group configuration (only work for LUT/ACL/IGMP) bit[12][9:4]: select destination configuration for port 13 ~ port 19 0 : none 1 : selected bit[13] : LUT trigger target for sniffer destination port group 1 0 : DA 1 : SA bit[14] : LUT trigger target for sniffer destination port group 2 0 : DA 1 : SA bit[15] : check if the destination port linkup or not 0 : check 1 : don't check	R/W	0x0000
0x22	Sniffer source port configuration bit[11:0] : sniffer source config for port 1 ~ port 12 0 : no selected 1 : source	R/W	0x0000
0x23	Sniffer source port configuration bit[12][9:4] : sniffer source config for port 13 ~ port 19 0 : no selected 1 : source	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
0x24	MISC configuration bit[0] : ACL function enable 0 : Disable 1 : Enable bit[1] : ACL ether type location for tag frame 0 : the location is after SA 1 : the location is after tag (ctag and/or stag) bit[2] : ACL ether type location for RFC 1042 frame 0 : the location is after SA 1 : the location is after RFC 1042 header bit[3] : LoopDetect block enable 0 : Disable 1 : Enable bit[5] : Sniffer Add/Rem Tag option for CPU special tag routing (reg 0x1C, bit[4] must be 1'b1) 0 : keep the original data 1 : according to other criteria bit[6] : Sniffer Add/Rem Tag option for ACL redirect/to_cpu action 0 : keep the original data 1 : according to other criteria bit[7] : Sniffer Add/Rem Tag option for other packets (include CPU special tag counting with Reg 0x1C, bit[4] is 1'b0) 0 : keep the original data 1 : according to other criteria Note : bit[7:5] only work when 0x1F bit[15] is 1'b1	R/W	0x00
0x25	802.3 OAM LoopBack configuration bit[11:0] : LoopBack enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0x26	802.3 OAM LoopBack configuration bit[12][9:4] : LoopBack enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000
0x27	802.3 OAM LoopBack configuration bit[11:0] : LoopBack mode select for port 1 ~ port 12 0 : passive mode 1 : active mode	R/W	0x0000
0x28	802.3 OAM LoopBack configuration bit[12][9:4] : LoopBack mode select for port 13 ~ port 19 0 : passive mode 1 : active mode	R/W	0x0000
0x29	IGMP snooping function configuration bit[0] : enable IGMP snooping function bit[1] : multicast table make by CPU bit[2] : Disable IP address 224.0.0.X broadcast (except IGMP packet) bit[3] : Disable " <u>Leave</u> " function (work in hardware-based IGMP-snooping) bit[4] : Reserved bit[5] : enable IGMP group member aging 0 : Disable 1 : Enable bit[12:6] : group member aging time setting (mg_mcst_thr + 1) x 70.4 sec. ±9.1% bit[13] : router list make by CPU only 0 : Disable 1 : make by CPU	R/W	0x4000

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
	bit[15:14] : router port list aging setting for geometry change detect 00 : aging Disable 01 : about 320s 10 : about 500s 11 : about 640s		
0x2A	IGMP packets forwarding configuration bit[3:0] : Query setting bit[7:4] : Leave setting bit[11:8] : unregister mcst data setting bit[15:12] : undefined IGMP type the 4-bit setting for each kind of packet is {drop, router, CPU, bcst} 0 : Disable 1 : Enable	R/W	0x1141
0x2B	IGMP packets forwarding configuration bit[4:0] : Report setting bit[9:5] : Group Specific Query setting bit[14:10] : registered mcst data setting the 5-bit setting is {group member, drop, router, CPU, bcst} 0 : Disable 1 : Enable bit[15] : the Hashing method for IGMP 0 : CRC 1 : Direct	R/W	0x5294
0x2C	IGMP Router List configuration bit[11:0] : Router List setting for port 1 ~ port 12 0 : normal port 1 : router port	R/W	0x0000
0x2D	IGMP Router List configuration bit[12][9:4] : Router List setting for port 13 ~ port 19 0 : normal port 1 : router port bit[13] : use for Router List clear process 0 : no action 1 : clear internal router list setting bits	R/W	0x0000
0x2E	Memory access command for Mcst table and Source List table Source List command (bit[8] is 1'b0) bit[5:0] : memory address bit[7:6] : Reserved bit[9:8] : should be 2'b00 bit[13:10] : Reserved bit[14] : read/write control 0 : read 1 : write bit[15] : command trig/ack Mcst table command bit[7:0] : memory address bit[9:8] : should be 2'b01 bit[13:10] : Reserved bit[14] : read/write control 0 : read 1 : write bit[15] : command trig/ack IP table command bit[6:0] : memory address bit[7] : Reserved bit[9:8] : should be 2'b10 bit[13:10] : Reserved	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
	bit[14] : read/write control 0 : read 1 : write bit[15] : command trig/ack		
0x2F	Read/Write data bit[15:0] for Mcst table/Source List table/IP table	R/W	0x0000
0x30	Read/Write data bit[31:16] for Mcst table/Source List table/IP table	R/W	0x0000
0x31	Read/Write data bit[47:32] for Mcst table/Source List table/IP table	R/W	0x0000
0x32	Read/Write data bit[63:48] for Mcst table/Source List table/IP table	R/W	0x0000
0x33	Read/Write data bit[79:64] for Mcst table/Source List table/IP table	R/W	0x0000
0x34	Read/Write data bit[95:80] for Mcst table/Source List table/IP table	R/W	0x0000
0x35	Read/Write data bit[111:96] for Mcst table/Source List table/IP table	R/W	0x0000
0x36	Read/Write data bit[127:112] for Mcst table/Source List table/IP table	R/W	0x0000
0x37	Read/Write data bit[143:128] Mcst table/Source List table/IP table	R/W	0x0000
0x38	Read/Write data bit[159:144] for Mcst table/Source List table/IP table	R/W	0x0000
0x39	Read/Write data bit[4:0] : for Mcst table bit[164:160] bit[15:0] : for Source List table/IP table bit[175:160]	R/W	0x0000
0x3A	Read/Write data bit[11:0] : for IP table bit[187:176] bit[15:0] : for Source List table bit[191:176]	R/W	0x0000
0x3B ~ 0x56	Read/Write data bit[207:192] for Source List table ~ Read/Write data bit[627:624] for Source List table	R/W	0x0000
0x57	Spanning Tree Protocol port state register 1_0 bit[15:0] : port state setting for port 1 ~ port 8, two bit per port. 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state note : this register for both STP and MSTP	R/W	0xFFFF
0x58	Spanning Tree Protocol port state register 1_1 bit[7:0] : port state setting for port 9 ~ port 12, two bit per port. 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state note : this register for both STP and MSTP	R/W	0xFFFF
0x59	Spanning Tree Protocol port state register 1_2 Bit[7:0] : Reserved bit[15:8] : port state setting for port 13 ~ port 16, two bit per port. 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state note : this register for both STP and MSTP	R/W	0xFFFF

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
0x5A	Spanning Tree Protocol port state register 1_3 bit[9:8][3:0] : port state setting for port 17 ~ port 19, two bit per port. 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state note : this register for both STP and MSTP	R/W	0x3FF
0x5B ~ 0x5E	Multiple Spanning Tree Protocol port state register 2 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x5F ~ 0x62	Multiple Spanning Tree Protocol port state register 3 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x63 ~ 0x66	Multiple Spanning Tree Protocol port state register 4 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x67 ~ 0x6A	Multiple Spanning Tree Protocol port state register 5 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x6B ~ 0x6E	Multiple Spanning Tree Protocol port state register 6 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x6F ~ 0x72	Multiple Spanning Tree Protocol port state register 7 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x73 ~ 0x76	Multiple Spanning Tree Protocol port state register 8 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
0x77 ~ 0x7A	Multiple Spanning Tree Protocol port state register 9 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x7B ~ 0x7E	Multiple Spanning Tree Protocol port state register 10 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x7F ~ 0x82	Multiple Spanning Tree Protocol port state register 11 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x83 ~ 0x86	Multiple Spanning Tree Protocol port state register 12 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x87 ~ 0x8A	Multiple Spanning Tree Protocol port state register 13 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x8B ~ 0x8E	Multiple Spanning Tree Protocol port state register 14 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x8F ~ 0x92	Multiple Spanning Tree Protocol port state register 15 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x93 ~ 0x96	Multiple Spanning Tree Protocol port state register 16 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x97	sFlow enable configuration for port 1 ~ port 12 bit[11:0] : enable for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0x98	sFlow enable configuration for port 13 ~ port 19 bit[12][9:4] : enable for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
0x99	sFlow sample method, 3 bits per port bit[14:0] : sample method for port 1 ~ port 5 000 : inbound 001 : VID 010 : ACL 011 : outbound 100 : Reserved 101 : LUT_MAC	R/W	0x0000
0x9A	sFlow sample method, 3 bits per port bit[14:0] : sample method for port 6 ~ port 10	R/W	0x0000
0x9B	sFlow sample method, 3 bits per port bit[5:0] : sample method for port 11 ~ port 12	R/W	0x0000
0x9C	Reserved		
0x9D	sFlow sample method, 3 bits per port bit[14:0] : sample method for port 13 ~ port 17	R/W	0x0000
0x9E	sFlow sample method, 3 bits per port bit[11:9][2:0] : sample method for port 18~ port 19 bit[12] : each port use the same sample counter	R/W	0x0000
0x9F	sFlow sample rate configure for port 1 bit[15:0] : rate configure. (rate = total packets / sampled packet)	R/W	0x0064
0xA0 ~ 0xAA	sFlow sample rate configure for port 2 ~ port 12 bit[15:0] : rate configure. (rate = total packets / sampled packet)	R/W	0x0064
0xAB ~ 0xB2	Reserved		
0xB3 ~ 0xB8	sFlow sample rate configure for port 13 ~ port 18 bit[15:0] : rate configure. (rate = total packets / sampled packet)	R/W	0x0064
0xB9 0xBA	Reserved		
0xBB	sFlow sample rate configure for port 19 bit[15:0] : rate configure. (rate = total packets / sampled packet)	R/W	0x0064
0xBC	sFlow sample VID configure for port 1 bit[11:0] : VID that want to sampled for sFlow	R/W	0x000
0xBD ~ 0xC7	sFlow sample VID configure for port 2 ~ port 12 bit[11:0] : VID that want to sampled for sFlow	R/W	0x000
0xC8 ~ 0xCF	Reserved		
0xD0 ~ 0xD5	sFlow sample VID configure for port 13 ~ port 18 bit[11:0] : VID that want to sampled for sFlow	R/W	0x000
0xD6 0xD7	Reserved		

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
0xD8	sFlow sample VID configure for port 19 bit[11:0] : VID that want to sampled for sFlow	R/W	0x000
0xD9	VLAN mask function configuration bit[11:0] : 12 bits VID mask 0 : mask 1 : not mask	R/W	0xFFF
0xDA	VLAN mask function enable for port 1 ~ port 12 bit[11:0] : function enable setting, per port 1 bit 0 : Disable 1 : Enable	R/W	0x0000
0xDB	VLAN mask function enable for port 13 ~ port 19 bit[12][9:4]: function enable setting, per port 1 bit 0 : Disable 1 : Enable	R/W	0x0000
0xDC ~ 0xDF	Reserved		
0xE0	CPU read/write address table configuration bit[12:0] : LUT address bit[13] : LUT block select 0 : first block 1 : second block bit[14] : Read/Write configuration 0 : Read 1 : Write bit[15] : Command trig/ack	R/W	0x0000
0xE1	CPU read/write address table data bit[15:0] : LUT data[15:0] if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x0000
0xE2	CPU read/write address table data bit[15:0] : LUT data[31:16] if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x0000
0xE3	CPU read/write address table data bit[15:0] : LUT data[47:32] if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x0000
0xE4	CPU read/write address table data bit[15:0] : LUT data[63:48] if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x0000
0xE5	CPU read/write address table data bit[4:0] : LUT data[68:64] bit[5] : Table address access method 0 : address calculated by CPU 1 : address calculated by HW for normal MAC entry if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x00

ARL Registers : Page 0x01			
Reg Addr.	Register Description	R/W	Default value
0xE6	IGMP join / leave enable for each port bit[11:0] : enable join / leave for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0xFFFF
0xE7	IGMP join / leave enable for each port bit[12][9:4] : enable join / leave for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x1FFF
0xE8	ARP storm drop event for port 1 ~ port 12 bit[11:0] : indicate the ARP storm drop event for port 1 ~ port 12	R/C	0x0000
0xE9	ARP storm drop event for port 13 ~ port 19 bit[12][9:4] : indicate the ARP storm drop event for port 13 ~ port 19	R/C	0x0000
0xEA	ICMP storm drop event for port 1 ~ port 12 bit[11:0] : indicate the ICMP storm drop event for port 1 ~ port 12	R/C	0x0000
0xEB	ICMP storm drop event for port 13 ~ port 19 bit[12][9:4]: indicate the ICMP storm drop event for port 13 ~ port 19	R/C	0x0000
0xEC ~ 0xEF	Reserved		
0xF0	Multicast VLAN Group 1 setting bit[11:0] : VLAN member setting for port 1 ~ port 12	R/W	0x0000
0xF1	Multicast VLAN Group 1 setting bit[12][9:4]: VLAN member setting for port 13 ~ port 19	R/W	0x0000
0xF2 ~ 0xFD	Multicast VLAN Group 2 ~ 7 setting	R/W	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

6.5 ARL Control Register Page 2

ARL Registers : Page 0x02			
Reg Addr.	Register Description	R/W	Default value
0x01	Configuration for IP filter function bit[11:0] : IP filter function enable for port 1 ~ port 12	R/W	0x0000
0x02	Configuration for IP filter function bit[12][9:4] : IP filter function enable for port 13 ~ port 19 bit[13] : filter mode selection 0 : drop if IP mis-match 1 : drop if IP match bit[14] : enable pass for IP equal 0.0.0.0 0 : Disable 1 : Enable bit[15] : Hashing method selection 0 : CRC hashing 1 : direct hashing	R/W	0x0000
0x03 ~ 0x05	Reserved		
0x06	VLAN configuration bit[0] : protocol based VLAN enable 0 : Disable 1 : Enable bit[1] : tag based VLAN enable 0 : Disable 1 : Enable bit[2] : SVL/IVL select 0 : SVL 1 : IVL bit[3] : select the tag/untag method 0 : based on ports 1 : based on VIDs bit[4] : Modify tag in VID tag mode for CPU port 0 : Don't modify 1 : modify tag according to settings bit[5] : CTAG Remove/Modify enable 0 : Don't change CTAG 1 : remove/modify CTAG enable bit[6] : MSTP enable 0 : Disable 1 : Enable bit[7] : always use CTAG VID 0 : use CTAG / STAG (when STAG exist) 1 : use CTAG (even with STAG) bit[8] : Multicast Group specify VLAN Group 0 : Disable 1 : Enable bit[9] : VID priority works with the priority bits remark function 0 : Disable 1 : Enable bit[14:10] : inactive VID redirect 0~11,20~25,28 : redirect to port 1 ~ port 19 30 : broadcast others : drop bit[15] : inactive VID redirect enable 0 : Disable 1 : Enable	R/W	0x0000

ARL Registers : Page 0x02			
Reg Addr.	Register Description	R/W	Default value
0x07	Insert PVID to the output port bit[11:0] : insert PVID to the output frame for port 1 ~ port 12 0 : Disable 1 : insert PVID to the current port will replace the VID of tag frame to PVID	R/W	0x0000
0x08	Insert PVID to the output port bit[12][9:4] : insert PVID to the output frame for port 13 ~ port 19 0 : Disable 1 : insert PVID to the current port will replace the VID of tag frame to PVID	R/W	0x0000
0x09	VLAN ingress check configuration (802.1Q 8.6.2) bit[11:0] : check if the port is the VLAN member for port 1 ~ port 12 0 : Don't check if the ingress port is in the VLAN group 1 : check if the ingress port is in the VLAN group	R/W	0x0000
0x0A	VLAN ingress check configuration (802.1Q 8.6.2) bit[12][9:4] : check if the port is the VLAN member for port 13 ~ port 19 0 : Don't check if the ingress port is in the VLAN group 1 : check if the ingress port is in the VLAN group	R/W	0x0000
0x0B	VLAN ingress check for Frame Type bit[15:0] : the ingress frame type check for port 1 ~ port 8, 2-bit/port 00 : admit all 01 : admit tag frame only 10 : admit priority tag and non-tag frame 11 : admit priority tag and tag frame	R/W	0x0000
0x0C	VLAN ingress check for Frame Type bit[7:0] : the ingress frame type check for port 9 ~ port 12, 2-bit/port 00 : admit all 01 : admit tag frame only 10 : admit priority tag and non-tag frame 11 : admit priority tag and tag frame	R/W	0x0000
0x0D	VLAN ingress check for Frame Type bit[7:0] : Reserved bit[15:8] : the ingress frame type check for port 13 ~ port 16, 2-bit/port 00 : admit all 01 : admit tag frame only 10 : admit priority tag and non-tag frame 11 : admit priority tag and tag frame	R/W	0x0000
0x0E	VLAN ingress check for Frame Type bit[9:8][3:0] : the ingress frame type check for port 17 ~ port 19, 2-bit/port 00 : admit all 01 : admit tag frame only 10 : admit priority tag and non-tag frame 11 : admit priority tag and tag frame	R/W	0x000

ARL Registers : Page 0x02			
Reg Addr.	Register Description	R/W	Default value
0x0F	VLAN egress configuration. Set the criteria for the output to use default group setting. bit[11:0] : by port. One bit per port, for port 1 ~ port 12 0 : Don't use default group setting 1 : use default group setting	R/W	0x0000
0x10	VLAN egress configuration. Set the criteria for the output to use default group setting. bit[12][9:4] : by port. One bit per port, for port 13 ~ port 19 0 : Don't use default group setting 1 : use default group setting bit[13] : unicast frame 0 : Don't use default group setting 1 : use default group setting bit[14] : multicast frame (DA equal to 01:00:5E:xx:xx:xx and IGMP need to be enabled) 0 : Don't use default group setting 1 : use default group setting bit[15] : ARP frame 0 : Don't use default group setting 1 : use default group setting	R/W	0x0000
0x11	Allow for local traffic bit[11:0] : enable local traffic forwarding for port 1 ~ port 12 0 : Disable 1 : Enable	R/W	0x0000
0x12	Allow for local traffic bit[12][9:4] : enable local traffic forwarding for port 13 ~ port 19 0 : Disable 1 : Enable	R/W	0x0000
0x13	port 1 PVID configuration bit[11:0] : PVID setting bit[14:12] : PVID priority bits setting bit[15] : Force use PVID as VID for VLAN checking 0 : Disable 1 : Enable	R/W	0x0001
0x14 ~ 0x1E	port 2 ~ port 12 PVID configuration bit[11:0] : PVID setting bit[14:12] : PVID priority bits setting bit[15] : Force use PVID as VID for VLAN checking 0 : Disable 1 : Enable	R/W	0x0001
0x1F ~ 0x26	Reserved		
0x27 ~ 0x2C	port 13 ~ port 18 PVID configuration bit[11:0] : PVID setting bit[14:12] : PVID priority bits setting bit[15] : Force use PVID as VID for VLAN checking 0 : Disable 1 : Enable	R/W	0x0001
0x2D 0x2E	Reserved		

ARL Registers : Page 0x02

Reg Addr.	Register Description	R/W	Default value
0x2F	port 19 PVID configuration bit[11:0] : PVID setting bit[14:12] : PVID priority bits setting bit[15] : Force use PVID as VID for VLAN checking 0 : Disable 1 : Enable	R/W	0x0001
0x30	port 1 Port based VLAN configuration bit[11:0] : Port based VLAN group (port 1 ~ port 12) setting	R/W	0xFFFF
0x31	port 1 Port based VLAN configuration bit[12][9:4] : Port based VLAN group (port 13 ~ port 19) setting bit[13] : Force port 1 use Port based VLAN	R/W	0x1FFF
0x32 ~ 0x47	port 2 ~ port 12 Port based VLAN configuration	R/W	0xFFFF 0x1FFF
0x48 ~ 0x57	Reserved		
0x58 ~ 0x63	port 13 ~ port 18 Port based VLAN configuration	R/W	0xFFFF 0x1FFF
0x64 ~ 0x67	Reserved		
0x68	port 19 Port based VLAN configuration bit[11:0] : Port based VLAN group (port 1 ~ port 12) setting	R/W	0xFFFF
0x69	port 19 Port based VLAN configuration bit[12][9:4] : Port based VLAN group (port 13 ~ port 19) setting bit[13] : Force port 19 use Port based VLAN	R/W	0x1FFF
0x6A	Protocol based VLAN entry 1 configuration bit[15:0] : TYPE for protocol define in entry 1	R/W	0x0000
0x6B	Protocol based VLAN entry 1 configuration bit[11:0] : VID for protocol define in entry 1 bit[13:12] : Entry A protocol selection 00 : invalid 01 : EtherType 10 : LLC 11 : RFC 1042	R/W	0x0000
0x6C ~ 0x89	0x6C ~ 0x71 for Protocol based VLAN entry 2 ~ 4 configuration Note : 0x6A ~ 0x89 also used for ACL VID remarking.	R/W	0x0000 0x0000
0x8A	ACL Assigned VLAN Group 1 bit[11:0] : VLAN Group 01 member setting for port 1 ~ port 12 0 : not member 1 : member	R/W	0x0000

ARL Registers : Page 0x02			
Reg Addr.	Register Description	R/W	Default value
0x8B	ACL Assigned VLAN Group 1 bit[12][9:4] : VLAN Group 01 member setting for port 13 ~ port 19 0 : not member 1 : member	R/W	0x0000
0x8C ~ 0xC9	ACL Assigned VLAN Group 2 ~ 32 configuration	R/W	0x0000 0x0000
0xCA	VLAN exclusive setting for port 1 ~ port 12 bit[11:0] : 0: this port is normal port 1: this port is protected port	R/W	0x0000
0xCB	VLAN exclusive setting for port 13 ~ port 19 bit[12][9:4] : 0: this port is normal port 1: this port is protected port	R/W	0x0000
0xCC	VLAN output port add tag setting for port 1 ~ port 12 bit[11:0] : output port add tag setting 0 : Don't add 1 : add	R/W	0x0000
0xCD	VLAN output port add tag setting for port 13 ~ port 19 bit[12][9:4] : output port add tag setting 0 : Don't add 1 : add	R/W	0x0000
0xCE	VLAN output port remove tag setting for port 1 ~ port 12 bit[11:0] : output port remove tag setting 0 : Don't remove 1 : remove	R/W	0x0000
0xCF	VLAN output port remove tag setting for port 13 ~ port 19 bit[12][9:4] : output port remove tag setting 0 : Don't remove 1 : remove	R/W	0x0000
0xD0	VLAN uplink function configuration bit[11:0] : uplink port configuration for port 1 ~ port 12 0 : normal port 1 : uplink port	R/W	0x0000
0xD1	VLAN uplink function configuration bit[12][9:4] : uplink port configuration for port 13 ~ port 19 0 : normal port 1 : uplink port bit[13] : uplink port function enable 0 : Disable 1 : Enable	R/W	0x0000
0xD2	VLAN Table Access command register bit[11:0] : VID bit[12] : sequential Read bit[13] : Reserved bit[14] : Read/Write 0 : Read 1 : Write bit[15] : command trig/ack	R/W	0x0000
0xD3	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[15:0]	R/W	0x0000
0xD4	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[31:16]	R/W	0x0000
0xD5	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[47:32]	R/W	0x0000

ARL Registers : Page 0x02			
Reg Addr.	Register Description	R/W	Default value
0xD6	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[63:48]	R/W	0x0000
0xD7	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[79:64]	R/W	0x0000
0xD8	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[95:80]	R/W	0x0000
0xD9	ACL Bandwidth threshold setting 0 ~ 1 bit[6:0] : ACL bw0 threshold bit[7] : unit selection 0 : 128Kbps, 1 : 2Mbps bit[14:8] : ACL bw1 threshold bit[15] : unit selection 0 : 128Kbps, 1 : 2Mbps	R/W	0x0000
0xDA ~ 0xDF	ACL Bandwidth threshold setting 2 ~ 13	R/W	0x0000
0xE0	ACL Bandwidth threshold setting 14 bit[6:0] : ACL bw14 threshold bit[7] : unit selection 0 : 128Kbps, 1 : 2Mbps	RW	0x00
0xE1	ACL user define pattern location setting bit[4:0] : pattern 1 location setting bit[9:5] : pattern 2 location setting	R/W	0x000
0xE2	ACL user define pattern location setting bit[4:0] : pattern 3 location setting bit[9:5] : pattern 4 location setting	R/W	0x000
0xE3	ACL Table Access command register bit[6:0] : entries select bit[7] : sequential read bit[8] : table select 0 : rule 1 : action bit[14] : Read/ Write 0 : Read 1 : Write bit[15] : command trig	R/W	0x0000
0xE4	ACL entries access data register bit[15:0] : read/write ACL entry data[15:0]	R/W	0x0000
0xE5	ACL entries access data register bit[15:0] : read/write ACL entry data[31:16]	R/W	0x0000
0xE6	ACL entries access data register bit[15:0] : read/write ACL entry data[47:32]	R/W	0x0000
0xE7	ACL entries access data register bit[15:0] : read/write ACL entry data[63:48]	R/W	0x0000
0xE8	ACL entries access data register bit[15:0] : read/write ACL entry data[79:64]	R/W	0x0000
0xE9	ACL entries access data register bit[15:0] : read/write ACL entry data[95:80]	R/W	0x0000
0xEA	ACL entries access data register bit[15:0] : read/write ACL entry data[111:96]	R/W	0x0000

ARL Registers : Page 0x02

Reg Addr.	Register Description	R/W	Default value
0xEB	ACL entries access data register bit[15:0] : read/write ACL entry data[127:112]	R/W	0x0000
0xEC	ACL entries access data register bit[15:0] : read/write ACL entry data[143:128]	R/W	0x0000
0xED	ACL entries access data register bit[6:0] : read/write ACL entry data[150:144]	R/W	0x00
0xEE	Configuration for VID/PVID match behavior setting bit0 for port 1 ~ port 12 (not affect non_tag/priority_tag) bit[11:0] : bit 0 setting for port 1 ~ port 12	R/W	0x0000
0xEF	Configuration for VID/PVID match behavior setting bit0 for port 13 ~ port 19 (not affect non_tag/priority_tag) bit[12][9:4] : bit 0 setting for port 13 ~ port 19	R/W	0x0000
0xF0	Configuration for VID/PVID match behavior setting bit1 for port 1 ~ port 12 bit[11:0] : bit 1 setting for port 1 ~ port 12	R/W	0x0000
0xF1	Configuration for VID/PVID match behavior setting bit1 for port 13 ~ port 19 bit[12][9:4]: bit 1 setting for port 13 ~ port 19 The behavior for {bit1, bit0} is : 00 : Disable 01 : drop if VID equals to PVID 10 : drop if VID does not equal to PVID 11 : act with Multicast SRC function, to pass VID equal to PVID	R/W	0x0000
0xF2	Configuration Source Ports for Multicast SRC function bit[11:0] : source port setting for port 1 ~ port 12	R/W	0x0000
0xF3	Configuration Source Ports for Multicast SRC function bit[12][9:4] : source port setting for port 13 ~ port 19	R/W	0x0000
0xF4	LUT memory repair control bit[0] : disable the repair entry 0 0 : enable, 1 : disable bit[1] : disable the repair entry 1 bit[2] : disable the repair entry 2 bit[3] : disable the repair entry 3 bit[5:4] : repair entry read back selection	R/W	0x00
0xF5	LUT memory repair status bit[12][9:0] : the failed memory address bit[13] : the failed memory block 0 : low bits block, 1 : high bits block bit[14] : Valid bit 0 : invalid 1 : valid	RO	0x0000

ARL Registers : Page 0x02			
Reg Addr.	Register Description	R/W	Default value
0xF6	MAC based VLAN configuration bit[0] : MAC based vlan enable 0 : disable 1 : enable bit[1] : the related LUT entry need to be static 0 : disable 1 : enable bit[2] : CPU enable for MAC based vlan 0 : disable 1 : enable bit[3] : assign VLAN for the unknown SA packets 0 : disable 1 : enable	R/W	0x0
0xF7	CPU read/write MAC based VLAN Table configuration bit[12:0] : Table address bit[13] : block selection (the same as LUT) bit[14] : read/write select 0 : read 1 : write bit[15] : command trigger	R/W	0x0000
0xF8	CPU write MAC based VLAN Table data bit[12:0] : Table data	R/W	0x0000
0xF9	CPU read MAC based VLAN Table data (first block) bit[12:0] : Table data	R/W	0x0000
0xFA	CPU read MAC based VLAN Table data (second block) bit[12:0] : Table data	R/W	0x0000
0xFB	VID configuration for unknown SA bit[11:0] : VID bit[12] : enable	R/W	0x0000
0xFF	Register Page selection bit[5:0] : page selection	R/W	0x00

6.6 SMI Control Register

SMI Registers : Page 0x03			
Reg Addr.	Register Description	R/W	Default value
0x01	Auto negotiation configuration for port 1 ~ port 12 bit[11:0] : 0 : Disable auto negotiation 1 : Enable auto negotiation	R/W	0xFFFF
0x02	Auto negotiation configuration for port 13 ~ port 19 bit[12][9:4] : 0 : Disable auto negotiation 1 : Enable auto negotiation	R/W	0x1FFF
0x03	Speed setting for 1000 Mbps for port 17 ~ port 19 bit[4][1:0] : 0 : 1000 Mbps ability disable 1 : 1000 Mbps ability enable	R/W	0x1F
0x04	Speed setting for 10/100 Mbps for port 1 ~ port 12 bit[11:0] : 0 : 10 Mbps 1 : 100 Mbps	R/W	0xFFFF
0x05	Speed setting for 10/100 Mbps for port 13 ~ port 19 bit[12][9:4] : 0 : 10 Mbps 1 : 100 Mbps	R/W	0x1FFF
0x06	Duplex setting for port 1 ~ port 12 bit[11:0] : 0 : half duplex 1 : full duplex	R/W	0xFFFF
0x07	Duplex setting for port 13 ~ port 19 bit[12][9:4] : 0 : half duplex 1 : full duplex	R/W	0x1FFF
0x08	Pause setting for port 1 ~ port 12 bit[11:0] : 0 : Disable pause 1 : Enable pause	R/W	0xFFFF
0x09	Pause setting for port 13 ~ port 19 bit[12][9:4] : 0 : Disable pause 1 : Enable pause	R/W	0x1FFF
0x0A	Asymmetric pause setting for port 1 ~ port 12 bit[11:0] : 0 : Disable asymmetric pause 1 : Enable asymmetric pause	R/W	0xFFFF
0x0B	Asymmetric pause setting for port 13 ~ port 19 bit[12][9:4] : 0 : Disable asymmetric pause 1 : Enable asymmetric pause	R/W	0x1FFF
0x0C	Backpressure setting for port 1 ~ port 12 bit[11:0] : 0 : backpressure function disable 1 : backpressure function enable	R/W	0xFFFF
0x0D	Backpressure setting for port 13 ~ port 19 bit[12][9:4] : 0 : backpressure function disable 1 : backpressure function enable	R/W	0x1FFF
0x0E	Power down setting for port 1 ~ port 12 bit[11:0] : 0 : power down disable 1 : power down enable	R/W	0xF000
0x0F	Power down setting for port 13 ~ port 19 bit[12][9:4] : 0 : power down disable 1 : power down enable	R/W	0x0C0F

SMI Registers : Page 0x03			
Reg Addr.	Register Description	R/W	Default value
0x10	<p>WOL function enable for port 17 ~ port 18 bit[1:0] : 0 : WOL disable 1 : WOL enable WOL function will be disabled when both IP1819I WOL and PHY WOL settings are disabled. bit[3:2] : Reserved bit[4] : port 17 WOL sense ANY packet to wake up bit[5] : port 17 WOL sense MAGIC packet to wake up bit[6] : port 18 WOL sense ANY packet to wake up bit[7] : port 18 WOL sense MAGIC packet to wake up bit[15:8] : Reserved</p>	R/W	0x0FF0
0x11	<p>PHY address setting for port 17 ~ port 19 bit[2:0] : port 17 PHY address, default 3'd2 bit[5:3] : port 18 PHY address, default 3'd3 bit[11:6] : Reserved bit[14:12] : port 19 PHY address, default 3'd1</p>	R/W	0x1B1A
0x12	<p>SMI MISC setting bit[0] : port 19 force link set 0 : force link Disable 1 : force link Enable bit[1] : port 19 force duplex pin setting (RO) 0 : half duplex 1 : full duplex bit[3:2] : port 19 force speed pin setting (RO) 00 : 10 Mbps 01 : 100 Mbps 10 : 1000 Mbps 11 : Reserved bit[5:4] : Reserved bit[6] : port 17 LED off @TP mode 0 : Disable 1 : Enable bit[7] : port 18 LED off @TP mode 0 : Disable 1 : Enable bit[8] : port 19 force status (according to 0x03/0x05/0x07/0x09/0x0B) 0 : Disable 1 : Enable bit[9] : port 17 force PAUSE 0 : Disable 1 : Enable bit[10] : port 18 force PAUSE 0 : Disable 1 : Enable bit[15:11] : Reserved</p>	R/W	0x003E

SMI Registers : Page 0x03			
Reg Addr.	Register Description	R/W	Default value
0x13	CPU read/write PHY register command bit[4:0] : PHY address bit[9:5] : MII register address bit[10] : write all TP (port 1 ~ port 16) bit[13:11] : Reserved bit[14] : 0 : read operation 1 : write operation bit[15] : the read/write PHY register command trigger (RC) 0 : idle 1 : start command/ command complete	R/W RC	0x0000
0x14	CPU read/write PHY register command data bit[15:0] : in read command – the read back data in write command – data want to write	R/W	0x0000
0x15	SCA startup status for port 1 ~ port 12 (fiber port not support) bit[11:0] : 0 : cable test fail 1 : cable test good	RO	0x0000
0x16	SCA startup status for port 13 ~ port 19 (fiber port not support) bit[12][9:4] : 0 : cable test fail 1 : cable test good bit[13] : SCA period setting 0 : run 5 seconds show 3 seconds 1 : run 10 seconds show 5 seconds bit[14] : SCA enable 0 : Disable 1 : Enable bit[15] : SCA trig (only work when bit[14] is asserted) 0 : no action 1 : trig SCA and do it once	R/W	0x0000
0x17	LED Setting bit[2:0] : LED mode (B : bi-color; M : mono-color) 000 : 3-bit M (Giga-Spd, L/A, Dupx/Col) @ GE port (100-Spd, L/A, Dupx/Col) @ FE port 001 : 3-bit M (Giga-L/A, 10/100-L/A, Dupx/Col) @ GE port (100-L/A, 10-L/A, Dupx/Col) @ FE port 010 : 3-bit M (Giga-Spd, 10/100-Spd, /A) @ GE port (100-Spd, 10-Spd, /A) @ FE port 011 : 2-bit M (Giga-Spd, L/A) @ GE port (100-Spd, L/A) @ FE port 100 : 2-bit B, 1-bit M (Spd & L/A , PSE) @ GE port (Spd1 & L/A , PSE) @ FE port 101 : 2-bit M (L, /A) 110 : 2-bit B (Spd & L/A) @ GE port (Spd1 & L/A) @ FE port 111 : 2-bit B (Spd & L/A) @ GE port and 1-bit M (L/A) @ FE port (Reference 0x1E, 0x1F for PSE setting)	R/W RC	0x00C3

SMI Registers : Page 0x03

Reg Addr.	Register Description	R/W	Default value
	bit[3] : Reserved bit[5:4] : LED blink rate 00 : 40 ms 01 : 80 ms 10 : 120 ms 11 : 160 ms bit[7:6] : LED clock rate 00 : 781 KHz 01 : 2.5 MHz 10 : 5.2 MHz 11 : 10.4 MHz bit[8] : LED col blink disable 0 : blink when collision 1 : no blink when collision bit[9] : LED act (tx/rx) blink disable 0 : blink when act 1 : no blink when act bit[10] : LED loop-detect indication 0 : disable 1 : enable bit[11] : LED loop-detect indication time 0 : short pattern 1 : long pattern bit[12] : LED power-saving set. 0 : disable 1 : enable bit[13] : LED power-saving trig, and this bit will work when bit[12] is asserted. (RC) 0 : non action 1 : trig bit[14] : LED power-saving time 0 : LED trig show time is 10s 1 : LED trig show time is 30s bit[15] : CPU control serial-LED function 0 : disable 1 : enable		
0x18	LED port selection for port 1 ~ port 12 bit[11:0] : LED port selection	R/W	0x0FFF
0x19	LED port selection for port 13 ~ port 19 bit[12][9:4] : LED port selection bit[13] : Reserved bit[14] : port 19 LED CPU control enable 0 : Disable 1 : Enable (The corresponding signals for led_0/led_1/led_2, reference to register 0x1B[12]/0x1D[12]/0x1F[12]) bit[15] : Reserved	R/W	0x13F0

SMI Registers : Page 0x03			
Reg Addr.	Register Description	R/W	Default value
0x1A	CPU control serial-LED setting for port 1 ~ port 12 bit[11:0] : serial-LED(led_0) setting	R/W	0xFFFF
0x1B	CPU control serial-LED setting for port 13 ~ port 19 bit[12][9:4] : serial-LED(led_0) setting	R/W	0x1FFF
0x1C	CPU control serial-LED setting for port 1 ~ port 12 bit[11:0] : serial-LED(led_1) setting	R/W	0xFFFF
0x1D	CPU control serial-LED setting for port 13 ~ port 19 bit[12][9:4] : serial-LED(led_1) setting	R/W	0x1FFF
0x1E	CPU control serial-LED setting for port 1 ~ port 12 bit[11:0] : serial-LED(led_2) setting	R/W	0xFFFF
0x1F	CPU control serial-LED setting for port 13 ~ port 19 bit[12][9:4] : serial-LED(led_2) setting (reference to 0x17 LED mode = 3'b100, when enable PSE, the led_2 will be controlled via 0x1E & 0x1F)	R/W	0x1FFF
0x20	SMI port status for port 1 ~ port 2 (7bit / port) bit[6:0] : port 1 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit[7] : Reserved bit[14:8] : port 2 status flow_ctrl: include backpressure in half duplex speed definition: 1x: 1000 Mbps 01: 100 Mbps 00: 10 Mbps	RO	0x7A7A
0x21	SMI port status for port 3 ~ port 4 (7bit / port) bit[6:0] : port 3 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit[7] : Reserved bit[14:8] : port 4 status	RO	0x7A7A
0x22	SMI port status for port 5 ~ port 6 (7bit / port) bit[6:0] : port 5 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit[7] : Reserved bit[14:8] : port 6 status	RO	0x7A7A
0x23	SMI port status for port 7 ~ port 8 (7bit / port) bit[6:0] : port 7 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit[7] : Reserved bit[14:8] : port 8 status	RO	0x7A7A
0x24	SMI port status for port 9 ~ port 10 (7bit / port) bit[6:0] : port 9 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit[7] : reserved bit[14:8] : port 10 status	RO	0x7A7A

SMI Registers : Page 0x03			
Reg Addr.	Register Description	R/W	Default value
0x25	SMI port status for port 11 ~ port 12 (7bit / port) bit[6:0] : port 11 status { AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit[7] : reserved bit[14:8] : port 12 status	RO	0x7A7A
0x26 ~ 0x29	Reserved		
0x2A	SMI port status for port 13 ~ port 14 (7bit / port) bit[6:0] : port 13 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit[7] : reserved bit[14:8] : port 14 status	RO	0x7A7A
0x2B	SMI port status for port 15 ~ port 16 (7bit / port) bit[6:0] : port 15 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit[7] : reserved bit[14:8] : port 16 status	RO	0x7A7A
0x2C	SMI port status for port 17 ~ port 18 (7bit / port) bit[6:0] : port 17 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit[7] : reserved bit[14:8] : port 18 status	RO	0x3E3E
0x2D	Reserved		
0x2E	SMI port status for port 19 (7bit / port) bit[6:0] : port 19 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link}	RO	0x3E
0x2F	EEE polling enable for port 1 ~ port 12 bit[11:0] : EEE port enable	R/W	0xFFFF
0x30	EEE polling enable for port 13 ~ port 19 bit[12][9:4] : EEE port enable 0 : Disable 1 : Enable bit[13] : MMD register read/write enable 0 : Disable 1 : Enable bit[14] : Reserved bit[15] : EEE check duplex enable 0 : Disable 1 : Enable	R/W	0x1FFF

SMI Registers : Page 0x03			
Reg Addr.	Register Description	R/W	Default value
0x31	MMD read/write command bit[4:0] : PHY address bit[9:5] : DEVICE address bit[13:10] : Reserved bit[14] : 0 : read operation 1 : write operation bit[15] : the read/write PHY register command trigger (RC) 0 : idle 1 : start command/ command complete	R/W RC	0x0000
0x32	MMD read/write ADDRESS bit[15:0] : ADDRESS	R/W	0x0000
0x33	MMD write DATA bit[15:0] : write data	R/W	0x0000
0x34	MMD read DATA bit[15:0] : read data	R/W	0x0000
0x35	EEE auto-negotiation ability for port 1 ~ port 12 bit[11:0] : 0 : AN EEE disable 1 : AN EEE enable	RO	0x0000
0x36	EEE auto-negotiation ability for port 13 ~ port 19 bit[12][9:4] : 0 : AN EEE disable 1 : AN EEE enable	RO	0x0000
0x37	EEE Tw for port 1 bit[8:0] : port 1 EEE Tw	RO	0x014
0x38	EEE Tw for port 2 bit[8:0] : port 2 EEE Tw	RO	0x014
0x39	EEE Tw for port 3 bit[8:0] : port 3 EEE Tw	RO	0x014
0x3A	EEE Tw for port 4 bit[8:0] : port 4 EEE Tw	RO	0x014
0x3B	EEE Tw for port 5 bit[8:0] : port 5 EEE Tw	RO	0x014
0x3C	EEE Tw for port 6 bit[8:0] : port 6 EEE Tw	RO	0x014
0x3D	EEE Tw for port 7 bit[8:0] : port 7 EEE Tw	RO	0x014
0x3E	EEE Tw for port 8 bit[8:0] : port 8 EEE Tw	RO	0x014
0x3F	EEE Tw for port 9 bit[8:0] : port 9 EEE Tw	RO	0x014
0x40	EEE Tw for port 10 bit[8:0] : port 10 EEE Tw	RO	0x014
0x41	EEE Tw for port 11 bit[8:0] : port 11 EEE Tw	RO	0x014
0x42	EEE Tw for port 12 bit[8:0] : port 12 EEE Tw	RO	0x014

SMI Registers : Page 0x03			
Reg Addr.	Register Description	R/W	Default value
0x43 ~ 0x4A	Reserved		
0x4B	EEE Tw for port 13 bit[8:0] : port 13 EEE Tw	RO	0x014
0x4C	EEE Tw for port 14 bit[8:0] : port 14 EEE Tw	RO	0x014
0x4D	EEE Tw for port 15 bit[8:0] : port 15 EEE Tw	RO	0x014
0x4E	EEE Tw for port 16 bit[8:0] : port 16 EEE Tw	RO	0x014
0x4F	EEE Tw for port 17 bit[8:0] : port 17 EEE Tw	RO	0x014
0x50	EEE Tw for port 18 bit[8:0] : port 18 EEE Tw	RO	0x014
0x51 0x52	Reserved		
0x53	EEE Tw for port 19 bit[8:0] : port 19 EEE Tw	RO	0x014
0x54	For PHY status register, register address and page setting bit[4:0] : PHY status register address (default 5'd17) bit[9:5] : PHY status page selection (default 5'd15)	R/W	0x01F1
0x55	For PHY status register, bit selection (select 2 bits) bit[15:0] : bit selection for PHY status register (default 16'h14)	R/W	0x0014
0x56	For PHY status register, read enable for port 1 ~ port 12 bit[11:0] : PHY status register address	R/W	0x0000
0x57	For PHY status register, read enable for port 13 ~port 19 bit[12][9:4] : PHY status register address	R/W	0x0000
0x58	For PHY status register, 100 fiber status for port 1 ~port 12 bit[11:0] : running on 100 fiber	RO	0x0000
0x59	For PHY status register, 100 fiber status for port 13 ~ port 19 bit[12][9:4] : running on 100 fiber	RO	0x0000
0x5A	For PHY status register, 1000 fiber status for port 1 ~ port 12 bit[11:0] : running on 1000 fiber	RO	0x0000
0x5B	For PHY status register, 1000 fiber status for port 13 ~ port 19 bit[12][9:4] : running on 1000 fiber	RO	0x0000
0x5C	Force link setting for port 1 ~ port 12 bit[11:0] : force link enable	R/W	0x0000
0x5D	Force link setting for port 13 ~ port 18 bit[9:4] : force link enable bit[13:10] : Reserved bit[14] : Test mode polling PHY enable 0 : Disable (default) 1 : Enable	R/W	0x0000

SMI Registers : Page 0x03			
Reg Addr.	Register Description	R/W	Default value
	bit[15] : Bypass PHY enable 0 : Disable (default) 1 : Enable		
0x5E	Reserved		
0x5F	SCA setting bit[4][1:0] : SCA enable for port 17 ~ port 19 0 : Disable (default) 1 : Enable bit[9][6:5] : SCA mode for port 17 ~ port 19 0 : running as GE PHY (default) 1 : running as FE PHY bit[15:10] : Reserved	R/W	0x0000
0x60	EEE local Tw register address of MMD at 1000Mbps bit[15:0] : MMD register address (0x60, 0x61 and 0x62 a set)	R/W	0x0004
0x61	EEE local Tw device address of MMD at 1000Mbps bit[4:0] : MMD device address	R/W	0x1E
0x62	EEE local Tw bit number of MMD at 1000Mbps bit[15:0] : MMD bit number of the selected register (select 9-bit of 16-bit, ex 0x01FF select the lowest 9 bits)	R/W	0x01FF
0x63	EEE local Tw register address of MMD at 100Mbps bit[15:0] : MMD register address (0x63, 0x64 and 0x65 a set)	R/W	0x0003
0x64	EEE local Tw device address of MMD at 100Mbps bit[4:0] : MMD device address	R/W	0x1E
0x65	EEE local Tw bit number of MMD at 100Mbps bit[15:0] : MMD bit number of the selected register (select 9-bit of 16-bit, ex 0x01FF select the lowest 9 bits)	R/W	0x01FF
0x66	Uni-direction enable for port 1 ~ port 12 bit[11:0] : 0 : uni-direction disable 1 : uni-direction enable	R/W	0x0000
0x67	Uni-direction enable for port 13 ~ port 19 bit[12][9:4] : 0 : uni-direction disable 1 : uni-direction enable	R/W	0x0000
0x68 ~ 0xFE	Reserved		
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

6.7 OAM Control Register

OAM Registers 1 : Page 0x04			
Reg Addr.	Register Description	R/W	Default value
0x01	OAM Information OAMPDU OUI setting bit[15:0] : Information OUI[15:0]	R/W	0x90C3
0x02	OAM Information OAMPDU OUI setting bit[7:0] : Information OUI[23:16]	R/W	0x00
0x03	OAM Information OAMPDU VENDOR setting bit[15:0] : Information VENDOR[15:0]	R/W	0x0000
0x04	OAM Information OAMPDU VENDOR setting bit[15:0] : Information VENDOR[31:16]	R/W	0x0000
0x05	OAM indirect register command bit[4:0] : port selection bit[9:5] : register selection bit[13:10] : Reserved bit[14] : read/write 0 : read command 1 : write command bit[15] : the read/write OAM indirect register command trigger (RC) 0 : idle 1 : start command(for write)/ command complete(for read) (reference the OAM indirect registers)	R/W RC	0x0000
0x06	OAM indirect register data bit[15:0] : in read command – the read back data in write command – data want to write (reference the OAM indirect registers)	R/W	0x0000
0x07	OAM Dying Gasp Independent enable for port 1 ~ port 12 bit[11:0] : OAM Dying Gasp Independent enable (Using this function, do not enable OAM by asserting indirect register 0x00 bit[0] OAM enable)	R/W	0x0000
0x08	OAM Dying Gasp Independent enable for port 13 ~ port 19 bit[12][9:4] : OAM Dying Gasp Independent enable (Using this function, do not enable OAM by asserting indirect register 0x00 bit[0] OAM enable)	R/W	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

6.8 OAM Indirect Registers for Each Port

OAM Indirect Registers			
Reg Addr.	Register Description	R/W	Default value
0x00	<p>OAM configuration</p> <p>bit[0] : OAM enable 0 : Disable 1 : Enable</p> <p>bit[1] : OAM configuration trig</p> <p>bit[2] : OAM remote LoopBack trig</p> <p>bit[3] : OAM reset</p> <p>bit[4] : Information OAMPDU configuration Mode (When setting Mode, bit[1] should be set as "1.") 0 : passive mode 1 : active mode</p> <p>bit[5] : Information OAMPDU configuration Remote LoopBack support (When setting Remote LoopBack ability, bit[1] should be set as "1.") 0 : Disable 1 : Enable</p> <p>bit[6] : OAM remote read/write enable 0 : Disable 1 : Enable</p> <p>bit[7] : OAM remote read/write check OUI 0 : Disable 1 : Enable</p> <p>bit[8] : OAM LoopBack timeout enable (timeout time is 5 seconds) 0 : Disable 1 : Enable</p> <p>bit[9] : OAM LoopBack test result Read Clear enable, please refer to indirect register 0x08 bit[6] and bit[7]. 0 : Disable 1 : Enable</p> <p>bit[10] : OAM critical event register setting (Should check setting with bit[11]) 0 : no critical event 1 : critical event occur</p> <p>bit[11] : OAM internal critical event disable (OAM critical event according to register setting; reference to bit[10]) 0 : Enable 1 : Disable</p> <p>bit[12] : OAM external critical event disable (OAM critical event according to PIN) 0 : Enable 1 : Disable</p> <p>bit[13] : OAM critical event indication once per second enable 0 : Disable 1 : Enable</p>	R/W	0x0000

OAM Indirect Registers			
Reg Addr.	Register Description	R/W	Default value
	bit[14] : OAM Discovery check Unidirectional field 0 : Disable 1 : Enable bit[15] : OAM Discovery check Remote LoopBack field 0 : Disable 1 : Enable		
0x01	OAM remote read/write command	R/W	0x0000
0x02	OAM remote read/write data	R/W	0x0000
0x03 ~ 0x07	Reserved		
0x08	OAM Status bit[0] : link status 0 : unlink 1 : link bit[1] : OAM mode 0 : passive mode 1 : active mode bit[2] : local fault (refer to 0x17 for detail) 0 : local OAM no faults 1 : local OAM fault occurred bit[3] : remote fault (refer to 0x17 for detail) 0 : remote OAM no faults 1 : remote OAM fault occurred bit[5:4] : Reserved bit[6] : active LoopBack test packets send out 0 : test packets not send out 1 : test packets send out bit[7] : active LoopBack test result 0 : fail 1 : ok bit[9:8] : Reserved bit[10] : OAM remote read/write OUI check result (if 0x00 bit[6] and bit[7] are enable) 0 : mismatch 1 : match bit[13:11] : OAM Discovery state bit[15:14] : OAM Transmit state	RO	0x0000
0x09	OAM local flag bit[15:0] : OAM local flag	RO	0x0000
0x0A	OAM local Information OAMPDU revision bit[15:0] : OAM local Information OAMPDU revision	RO	0x0000
0x0B	OAM local Information OAMPDU state and configuration bit[7:0] : OAM local Information OAMPDU configuration bit[15:8] : OAM local Information OAMPDU state	RO	0x0000

OAM Indirect Registers			
Reg Addr.	Register Description	R/W	Default value
0x0C	OAM local Information OAMPDU OUI[15:0] bit[15:0] : OAM local Information OAMPDU OUI[15:0]	RO	0x0000
0x0D	OAM local Information OAMPDU OUI[23:16] bit[7:0] : OAM local Information OAMPDU OUI[23:16]	RO	0x00
0x0E	OAM local Information OAMPDU VENDOR bit[15:0] : OAM local Information OAMPDU VENDOR[15:0]	RO	0x0000
0x0F	OAM local Information OAMPDU VENDOR bit[15:0] : OAM local Information OAMPDU VENDOR[31:16]	RO	0x0000
0x10	OAM otifi flag bit[15:0] : OAM remote flag	RO	0x0000
0x11	OAM remote Information OAMPDU revision bit[15:0] : OAM remote Information OAMPDU revision	RO	0x0000
0x12	OAM remote Information OAMPDU state and configuration bit[7:0] : OAM remote Information OAMPDU configuration bit[15:8] : OAM remote Information OAMPDU state	RO	0x0000
0x13	OAM remote Information OAMPDU OUI[15:0] bit[15:0] : OAM remote Information OAMPDU OUI[15:0]	RO	0x0000
0x14	OAM remote Information OAMPDU OUI[23:16] bit[7:0] : OAM remote Information OAMPDU OUI[23:16]	RO	0x00
0x15	OAM remote Information OAMPDU VENDOR bit[15:0] : OAM remote Information OAMPDU VENDOR[15:0]	RO	0x0000
0x16	OAM remote Information OAMPDU VENDOR bit[15:0] : OAM remote Information OAMPDU VENDOR[31:16]	RO	0x0000
0x17	OAM local/remote fault record(clear by indirect register 0x00 bit[3] reset) bit[0] : OAM local link fault bit[1] : OAM local dying gasp bit[2] : OAM local critical event bit[7:3] : Reserved bit[8] : OAM remote link fault bit[9] : OAM remote dying gasp bit[10] : OAM remote critical event	RO	0x0000
0x18 ~ 0x1F	Reserved		

6.9 RxDMA Control Register

RxDMA Registers : Page 0x06			
Reg Addr.	Register Description	R/W	Default value
0x01 ~ 0x0C	Reserved		
0x0D	<p>TCP/UDP destination port filter method</p> <p>bit[1:0] : port 1 “Forwarding WAN/LAN / Packet drop” setting 00 : Disable Forwarding WAN/LAN& Packet drop 01 : Packet Drop enable (TX/RX ref 0x13 ~ 0x16) 10 : Forwarding to LAN port only (ref 0x11 ~ 0x12) 11 : Forwarding to WAN port only (ref 0x11 ~ 0x12)</p> <p>bit[3:2] : port 2 “Forwarding WAN/LAN / Packet drop” setting bit[5:4] : port 3 “Forwarding WAN/LAN / Packet drop” setting bit[7:6] : port 4 “Forwarding WAN/LAN / Packet drop” setting bit[9:8] : port 5 “Forwarding WAN/LAN / Packet drop” setting bit[11:10] : port 6 “Forwarding WAN/LAN / Packet drop” setting bit[13:12] : port 7 “Forwarding WAN/LAN / Packet drop” setting bit[15:14] : port 8 “Forwarding WAN/LAN / Packet drop” setting</p>	R/W	0x0000
0x0E	<p>TCP/UDP destination port filter method</p> <p>bit[1:0] : port 9 “Forwarding WAN/LAN / Packet drop” setting bit[3:2] : port 10 “Forwarding WAN/LAN / Packet drop” setting bit[5:4] : port 11 “Forwarding WAN/LAN / Packet drop” setting bit[7:6] : port 12 “Forwarding WAN/LAN / Packet drop” setting bit[15:8] : Reserved</p>	R/W	0x0000
0x0F	<p>TCP/UDP destination port filter method</p> <p>bit[7:0] : Reserved bit[9:8] : port 13 “Forwarding WAN/LAN / Packet drop” setting bit[11:10] : port 14 “Forwarding WAN/LAN / Packet drop” setting bit[13:12] : port 15 “Forwarding WAN/LAN / Packet drop” setting bit[15:14] : port 16 “Forwarding WAN/LAN / Packet drop” setting</p>	R/W	0x0000
0x10	<p>TCP/UDP destination port filter method</p> <p>bit[1:0] : port 17 “Forwarding WAN/LAN / Packet drop” setting bit[3:2] : port 18 “Forwarding WAN/LAN / Packet drop” setting bit[7:4] : Reserved bit[9:8] : port 19 “Forwarding WAN/LAN / Packet drop” setting</p> <p>Drop/ Filter rule: (ref below table)</p> <p>(1) “Forwarding WANLAN / Packet drop setting = 10 or 11 this port only reference forwarding to WAN/LAN port only setting.</p> <p>(2) “Forwarding WAN/LAN / Packet drop setting = 01 (i) this port is Drop enable and look at “drop act on” setting (a) if act on RX , then all packet RX at this port is dropped (b) if act on TX , then all packet from other port TX out this port will be dropped</p>	R/W	0x0000

RxDMA Registers : Page 0x06			
Reg Addr.	Register Description	R/W	Default value
	(3) "Forwarding WAN/LAN / Packet drop setting = 00 Filter & Drop function at this port is disabled		
0x11	WAN Port setting for TCP/UDP destination port bit[11:0] : WAN port setting (port 1 ~ port 12) 0: set as LAN 1: set as WAN	R/W	0x0000
0x12	WAN Port setting for TCP/UDP destination port bit[12][9:4] : WAN port setting (port 13 ~ port 19) 0: set as LAN 1: set as WAN	R/W	0x0000
0x13	TCP/UDP destination port filter – Drop act on TX/RX setting bit[1:0] : port 1 drop act 00: Rx (all matched port 1 Rx packet drop) 01: Tx (all matched packet Tx to port 1 drop) 1x: Rx+Tx (packet RX/TX to port 1 drop) bit[3:2] : port 2 drop act bit[5:4] : port 3 drop act bit[7:6] : port 4 drop act bit[9:8] : port 5 drop act bit[11:10] : port 6 drop act bit[13:12] : port 7 drop act bit[15:14] : port 8 drop act	R/W	0x0000
0x14	TCP/UDP destination port filter – Drop act on TX/RX setting bit[1:0] : port 9 drop act bit[3:2] : port 10 drop act bit[5:4] : port 11 drop act bit[7:6] : port 12 drop act bit[15:8] : Reserved	R/W	0x0000
0x15	TCP/UDP destination port filter – Drop act on TX/RX setting bit[7:0] : Reserved bit[9:8] : port 13 drop act bit[11:10] : port 14 drop act bit[13:12] : port 15 drop act bit[15:14] : port 16 drop act	R/W	0x0000
0x16	TCP/UDP destination port filter – Drop act on TX/RX setting bit[1:0] : port 17 drop act bit[3:2] : port 18 drop act bit[7:4] : Reserved bit[9:8] : port 19 drop act	R/W	0x000

Host / Client Forwarding WAN / LAN and Packet drop setting Condition															
Host / Client		Client Port setting													
		Client is LAN Port						Client is WAN Port							
		00 Disable	01 Drop			10 LAN	11 WAN	00 Disable	01 Drop			10 LAN	11 WAN		
Host port setting	00 Disable	V	V	X	X	V	V	V	V	X	X	V	V	(1) V : PASS (2) X : Drop (3) Host port Switch Port to receive packet (4) Client port Switch Port to transmit packet	
	01 Drop	Act on RX	X						X						
		Act on TX+RX	X						X						
	Act on TX	V	V	X	X	V	V	V	V	X	X	V	V		
	10 FWD LAN	V	V	X	X	V	V	X	X	X	X	X	X		
11 FWD WAN	X	X	X	X	X	X	V	V	X	X	V	V			

RxDMA Registers : Page 0x06

Reg Addr.	Register Description	R/W	Default value
0x17	RX Priority queuing decision setting (1 bit/ port) port 1 ~ port 12 bit[11:0] : priority to Q based on ACL DSCP selected remark QID 0: Disable 1: Enable Priority remapping : TX priority remapping (PG08.0xB2 ~ 0xB3 > PG08.0x14 ~ 0x4D) > RX priority remapping (PG06.0x24 ~ 0x5D) > ACL DSCP remark addr / VLAN Table Remark pri (PG06.0x17 ~ 0x1A)	R/W	0x0000
0x18	RX Priority queuing decision setting (1 bit/ port) port 13 ~ port 19 bit[12][9:4]: priority to Q based on ACL DSCP selected remark QID 0: Disable 1: Enable	R/W	0x0000
0x19	RX Priority queuing decision setting (1 bit/ port) port 1 ~ port 12 bit[11:0] : priority to Q based on VLAN-table remarked tag priority 0: Disable 1: Enable	R/W	0x0000
0x1A	RX Priority queuing decision setting (1 bit/ port) port 13 ~ port 19 bit[12][9:4]: priority to Q based on VLAN-table remarked tag priority 0: Disable 1: Enable bit[14] : 0: disable 1: enable (priority to Q based on ACL/VLAN) bit[15] : ACL DSCP pri / VLAN-table Tag pri criteria order 0: ACL DSCP pri > VLAN-table tag pri 1: VLAN-table tag pr > ACL DSCP pri (Note: IF DSCP pri / Tag pri remark are both enabled this reg only affect rx packet to which one queue)	R/W	0x0000
0x1B	(Mac priority/ VLAN-table remarked tag priority) to DSCP auto remarking (port 1 ~ port 12) bit[11:0] : mac_priority to DSCP auto remarking 0: Disable 1: Enable	R/W	0x0000
0x1C	(Mac priority/ VLAN-table remarked tag priority) to DSCP auto remarking (port 13 ~ port 19) bit[12][9:4]: mac_priority to DSCP auto remarking 0: Disable 1: Enable	R/W	0x0000

RxDMA Registers : Page 0x06			
Reg Addr.	Register Description	R/W	Default value
0x1D	(Mac priority/ VLAN-table remarked tag priority) to DSCP auto remarking (port 1 ~ port 12) bit[11:0] : VLAN-table remarked tag priority to DSCP auto remarking	R/W	0x0000
0x1E	(Mac priority/ VLAN-table remarked tag priority) to DSCP auto remarking (port 13 ~ port 19) bit[12][9:4]: VLAN-table remarked tag priority to DSCP auto remarking bit[15] : mac_pri / remarked tag pri criteria order 0 : mac pri > remarked tag pri 1 : remarked pri > tag pri (Criteria ACL DSCP pri > above description) (If QinQ VID Sel is enable , ACL DSCP remark will be disabled)	R/W	0x0000
0x1F	TCP Flag attribute priority: bit[0] : <= 256 Bytes TCP SYN highest priority enable bit[1] : <= 256 Bytes TCP SYN/ACK highest priority enable bit[2] : <= 256 Bytes TCP ACK highest priority enable	R/W	0x0
0x20	WRED Drop packet setting: bit[0] : WRED drop act on TCP packet only (1: tcp0: all) bit[1] : WRED drop act on TCP exclude TCP SYN <= 256 B bit[2] : WRED drop act on TCP exclude TCP SYN/ACK <= 256 B bit[3] : WRED drop act on TCP exclude TCP ACK <= 256 B bit[8] : sFlow packet force TX out (0: normal drop 1: force tx, regardless any drop) bit[9] : sFlow packet port map to cpu packet length cutoff (0: Disable 1: Enable)	R/W	0x009
0x21	Out Queue Pause / Drop to RX setting bit[11:0] :port 1 ~ port 12 out queue threshold to RX pause/drop disable 0: Enable 1: Disable (1bit/port)	R/W	0x0000
0x22	Out Queue Rx Pause / Drop to RX setting bit[12][9:4]:port 13 ~ port 19 out queue threshold to RX pause/drop disable	R/W	0x0000
0x23	Reserved		
0x24	port 1 RX Priority remap data bit[2:0] : Priority 0 remap bit[5:3] : Priority 1 remap bit[8:6] : Priority 2 remap bit[11:9] : Priority 3 remap bit[14:12] : Priority 4 remap	R/W	0x4688
0x25	port 1 RX Priority remap data bit[2:0] : Priority 5 remap bit[5:3] : Priority 6 remap bit[8:6] : Priority 7 remap Priority remapping : TX priority remapping (PG08.0xB2~0xB3 > PG08.0x14 ~ 0x4D) > RX priority remapping (PG06.0x24~0x5D) > ACL DSCP remark addr / VLAN Table Remark pri (PG06.0x17 ~ 0x1A)	R/W	0x1F5

RxDMA Registers : Page 0x06			
Reg Addr.	Register Description	R/W	Default value
0x26	port 2 RX Priority remap data bit[2:0] : Priority 0 remap bit[5:3] : Priority 1 remap bit[8:6] : Priority 2 remap bit[11:9] : Priority 3 remap bit[14:12] : Priority 4 remap	R/W	0x4688
0x27	port 2 RX Priority remap data bit[2:0] : Priority 5 remap bit[5:3] : Priority 6 remap bit[8:6] : Priority 7 remap	R/W	0x1F5
0x28 ~ 0x3B	port 3 ~ port 12 RX priority remap data	R/W	0x4688 0x1F5
0x3C ~ 0x4B	Reserved		
0x4C ~ 0x57	port 13 ~ port 18 RX priority remap data	R/W	0x4688 0x1F5
0x58 ~ 0x5B	Reserved		
0x5C 0x5D	port 19 RX priority remap data	R/W	0x4688 0x1F5
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

6.10 TxDMA Control Register

TxDMA Registers : Page 0x07										
Reg Addr.	Register Description								R/W	Default value
0x01	QinQ double tag remove service tag operation configuration bit[11:0] : output frame remove service tag (port 1 ~ port 12) 0 : Disable 1 : remove service tag to output frame								R/W	0x0000
0x02	QinQ double tag remove service tag operation configuration bit[12][9:4] : output frame remove service tag (port 13 ~ port 19) 0 : Disable 1 : remove service tag to output frame								R/W	0x0000
0x03	QinQ double tag add service tag operation configuration bit[11:0] : output frame add service tag (port 1 ~ port 12) 0 : Disable 1 : add service tag to output frame								R/W	0x0000
0x04	QinQ double tag add service tag operation configuration bit[12][9:4] : output frame add service tag (port 13 ~ port 19) 0 : Disable 1 : add service tag to output frame (QinQ detect enable set from 0x05 ~ 0x06)								R/W	0x0000
		0x05~0x06 detect enable				0x05~0x06 detect disable				
Qing (add,rmv)		00	01	10	11	00	01	10	11	
Service	0	x	x	add	x	x	x	add	x	
Tag rx	1	x	rmv	mdf	x	x	x	add	x	
0x05	Detect RX QinQ double tag enable for port 1 ~ port 12 bit[11:0] : 0 : Disable 1 : Enable								R/W	0x0000
0x06	Detect RX QinQ double tag enable for port 13 ~ port 19 bit[12][9:4] : 0 : Disable 1 : Enable								R/W	0x0000
0x07	802.1Q tagged PVID use TX port enable for port 1 ~ port 12 bit[11:0] : 0 : Disable 1 : Enable Criteria priority (0x75 ~ 0x78): 00: TX PVID (0x07~0x08) > ACL VID > QID register 0x70~0x74 > RX PVID 01: TX PVID (0x07~0x08) > ACL VID > RX PVID 10: TX PVID (0x07~0x08) > ACL VID > Vlan table pri remark > RX PVID 11: TX PVID (0x07~0x08) > ACL VID > Vlan table pri remark > QID register 0x70~0x74 > RX PVID (QID register 0x70~0x74 only relative to { pri, cfi }, VID index will use RXPVID)								R/W	0x0000
0x08	802.1Q tagged PVID use TX port enable for port 13 ~ port 19 bit[12][9:4] : 0 : Disable 1 : Enable								R/W	0x0000
0x09	QinQ double tag type-length definition								R/W	0x88A8
0x0A	QinQ double tag {PCP, DEI, VID} definition0 – Data (S-Tag VID) by ACL rule / register setting Used to insert into/modify frame which should add/modify a double tag								R/W	0x0000
0x0B ~ 0x49	QinQ double tag {PCP, DEI, VID} definition1~63 – Data (S-Tag VID) by ACL rule / register setting Used to insert into frame which should add a double tag								R/W	0x0000

TxDMA Registers : Page 0x07			
Reg Addr.	Register Description	R/W	Default value
0x4A	<p>QinQ double tag VID r/w address and select method port 1</p> <p>bit[5:0] : port 1 S-TAG VID r/w register select address</p> <p>bit[11:8] : port 1 S-TAG VID r/w address select method</p> <p>0000 : address = mg_stag_vid_adr_p1[5:0]</p> <p>0001 : address = acl_dvid_sel[5:0], 6'd0 means no ACL act (if ACL entry is not hit , mg_stag_vid_adr_p1[5:0] will be used)</p> <p>0010 : address = 802.1Q-VID[11:6] (C-TAG VID[11:6])</p> <p>0011 : address = 802.1Q-VID[5:0] (C-TAG VID[5:0])</p> <p>0100 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[11:8] } (C-TAG VID[11:8])</p> <p>0101 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[7:4] } (C-TAG VID[7:4])</p> <p>0110 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[3:0] } (C-TAG VID[3:0]) (use RX 1Q-VID before TX remove/modify 1Q-VID, If RX packet is non-1Q-VID , then DVID0 will be used)</p> <p>1010 : address = 802.1Q-VID[11:6] (C-TAG VID[11:6])</p> <p>1011 : address = 802.1Q-VID[5:0] (C-TAG VID[5:0])</p> <p>1100 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[11:8] } (C-TAG VID[11:8])</p> <p>1101 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[7:4] } (C-TAG VID[7:4])</p> <p>1110 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[3:0] } (C-TAG VID[3:0]) (Insert / modify : use TX 1Q-VID , come from ACL result) (Remove : use RX port's PVID)</p> <p>bit[12] : QinQ double tag {PCP, DEI} field keep original packet During qinq tag modification. (0: modified 1: keep org)</p>	R/W	0x0000
0x4B	<p>QinQ double tag VID r/w address and select method port 2</p> <p>bit[5:0] : port 2 S-TAG VID r/w Register select address</p> <p>bit[10:8] : port 2 S-TAG VID r/w address select method</p> <p>bit[12] : QinQ double tag {PCP, DEI} field keep original packet During qinq tag modification. (0: modified 1: keep org)</p>	R/W	0x0000
0x4C ~ 0x55	<p>QinQ double tag VID r/w address and select method port 3 ~ port 12</p> <p>bit[5:0] : port 3 ~ port 12 S-TAG VID r/w Register select address</p> <p>bit[10:8] : port 3 ~ port 12 S-TAG VID r/w address select method</p> <p>bit[12] : QinQ double tag {PCP, DEI} field keep original packet During qinq tag modification. (0: modified 1: keep org)</p>	R/W	0x0000
0x56 ~ 0x5D	Reserved		
0x5E ~ 0x63	<p>QinQ double tag VID r/w address and select method port 13 ~ port 18</p> <p>bit[5:0] : port 13 ~ port 18 S-TAG VID r/w Register select address</p> <p>bit[10:8] : port 13 ~ port 18 S-TAG VID r/w address select method</p> <p>bit[12] : QinQ double tag {PCP, DEI} field keep original packet During qinq tag modification. (0: modified 1: keep org)</p>	R/W	0x0000

TxDMA Registers : Page 0x07			
Reg Addr.	Register Description	R/W	Default value
0x64 0x65	Reserved		
0x66	QinQ double tag VID r/w address and select method port 19 bit[5:0] : port 19 S-TAG VID r/w Register select address bit[10:8] : port 19 S-TAG VID r/w address select method bit[12] : QinQ double tag {PCP, DEI} field keep original packet During qinq tag modification. (0: modified 1: keep org)	R/W	0x0000
0x67	IPv4/v6 DSCP/IPP TOS remarking (ACL Select 0, 1) / (QID = 0,1) bit[5:0] : ACL select 0 / Queue 0 , remarking Value bit[6] : ACL select 0 / Queue 0 DSCP[2:0]/ IPP remarking 0 : Enable 1: Disable bit[7] : ACL select 0 / Queue 0 DSCP[5:3]/ TOS remarking 0 : Enable 1: Disable bit[13:8] : ACL select 1 / Queue 1 , remarking Value bit[14] : ACL select 1 / Queue 1 DSCP[2:0]/ IPP remarking 0 : Enable 1: Disable bit[15] : ACL select 1 / Queue 1 DSCP[5:3]/ TOS remarking 0 : Enable 1: Disable	R/W	0x0000
0x68	IPv4/v6 DSCP/IPP TOS remarking (ACL Select 2, 3) / (QID = 2,3) bit[5:0] : ACL select 2 / Queue 2 , remarking Value bit[6] : ACL select 2 / Queue 2 DSCP[2:0]/ IPP remarking bit[7] : ACL select 2 / Queue 2 DSCP[5:3]/ TOS remarking bit[13:8] : ACL select 3 / Queue 3 , remarking Value bit[14] : ACL select 3 / Queue 3 DSCP[2:0]/ IPP remarking bit[15] : ACL select 3 / Queue 3 DSCP[5:3]/ TOS remarking	R/W	0x0000
0x69	IPv4/v6 DSCP/IPP TOS remarking (ACL Select 4, 5) / (QID = 4,5) bit[5:0] : ACL select 4 / Queue 4 , remarking Value bit[6] : ACL select 4 / Queue 4 DSCP[2:0]/ IPP remarking bit[7] : ACL select 4 / Queue 4 DSCP[5:3]/ TOS remarking bit[13:8] : ACL select 5 / Queue 5 , remarking Value bit[14] : ACL select 5 / Queue 5 DSCP[2:0]/ IPP remarking bit[15] : ACL select 5 / Queue 5 DSCP[5:3]/ TOS remarking	R/W	0x0000
0x6A	IPv4/v6 DSCP/IPP TOS remarking (ACL Select 6, 7) / (QID = 6,7) bit[5:0] : ACL select 6 / Queue 6 , remarking Value. bit[6] : ACL select 6 / Queue 6 DSCP[2:0]/ IPP remarking bit[7] : ACL select 6 / Queue 6 DSCP[5:3]/ TOS remarking bit[13:8] : ACL select 7 / Queue 7 , remarking Value bit[14] : ACL select 7 / Queue 7 DSCP[2:0]/ IPP remarking bit[15] : ACL select 7 / Queue 7 DSCP[5:3]/ TOS remarking	R/W	0x0000
0x6B	IPv4/v6 DSCP/IPP TOS Setup command (0x6E/0x6F QID rule per queue setting, per queue default is disabled) bit[7:0] : queue enable for Q7 ~ Q0 bit[13:8] : Read/ Write dscp enable data From/to Pxx bit[15] : 0: Read 1: Write	R/W	0x0000

TxDMA Registers : Page 0x07			
Reg Addr.	Register Description	R/W	Default value
0x6C	IPv4/v6 DSCP/IPP TOS remarking Method (from ACL table) bit[11:0] : ACL ruled Ipv4 DSCP/IPP TOS remarking (1 bit / port) (ACL has higher priority than queue ID)	R/W	0xFFFF
0x6D	IPv4/v6 DSCP/IPP TOS remarking Method (from ACL table) bit[12][9:4] : ACL ruled Ipv4 DSCP/IPP TOS remarking (1 bit / port) (ACL has higher priority than queue ID)	R/W	0x1FFF
0x6E	IPv4/v6 DSCP/IPP TOS remarking Method (from QID)(0x6B set per queue based) bit[11:0] : queue ID rules Ipv4 DSCP/IPP TOS remarking (1 bit / port) (0x6C, 0x6D ACL has higher priority than 0x6E 0x6F queue ID)	R/W	0xFFFF
0x6F	IPv4/v6 DSCP/IPP TOS remarking Method (from QID) (0x6B set per queue based) bit[12][9:4] : queue ID rules Ipv4 DSCP/IPP TOS remarking (1 bit / port) (0x6C, 0x6D ACL has higher priority than 0x6E 0x6F queue ID)	R/W	0x1FFF
0x70	802.1Q TAG {PCP} remarking (Q1 , Q0) bit[0] : Queue 0 original CFI value 0 remarking bit[1] : Queue 0 original CFI value 1 remarking bit[6:4] : Queue 0 , 802.1Q priority remarking value bit[8] : Queue 1 original CFI value 0 remarking bit[9] : Queue 1 original CFI value 1 remarking bit[14:12] : Queue 1 , 802.1Q priority remarking value CFI remarking will be regardless of 802.1Q TAG enable/disable	R/W	0x1202
0x71	802.1Q TAG {PCP} remarking (Q3 , Q2) bit[0] : Queue 2 original CFI value 0 remarking bit[1] : Queue 2 original CFI value 1 remarking bit[6:4] : Queue 2 , 802.1Q priority remarking value bit[8] : Queue 3 original CFI value 0 remarking bit[9] : Queue 3 original CFI value 1 remarking bit[14:12] : Queue 3 , 802.1Q priority remarking value CFI remarking will be regardless of 802.1Q TAG enable/disable	R/W	0x3222
0x72	802.1Q TAG {PCP} remarking (Q5 , Q4) bit[0] : Queue 4 original CFI value 0 remarking bit[1] : Queue 4 original CFI value 1 remarking bit[6:4] : Queue 4 , 802.1Q priority remarking value bit[8] : Queue 5 original CFI value 0 remarking bit[9] : Queue 5 original CFI value 1 remarking bit[14:12] : Queue 5 , 802.1Q priority remarking value CFI remarking will be regardless of 802.1Q TAG enable/disable	R/W	0x5242
0x73	802.1Q TAG {PCP} remarking (Q7 , Q6) bit[0] : Queue 6 original CFI value 0 remarking bit[1] : Queue 6 original CFI value 1 remarking bit[6:4] : Queue 6 , 802.1Q priority remarking value bit[8] : Queue 7 original CFI value 0 remarking bit[9] : Queue 7 original CFI value 1 remarking bit[14:12] : Queue 7 , 802.1Q priority remarking value CFI remarking will be regardless of 802.1Q TAG enable/disable	R/W	0x7262

TxDMA Registers : Page 0x07			
Reg Addr.	Register Description	R/W	Default value
0x74	802.1Q TAG {PCP} remarking Setup command (qid rule) bit[7:0] : queue enable for Q7 ~ Q0 bit[13:8] : Read/Write remarking enable data to From/to Pxx bit[15] : 0: Read 1: Write	R/W	0x0000
0x75	802.1Q TAG {PCP, CFI} remarking criteria (port 1 ~ port 8 , 2bit / port) bit[1:0] : port 1 remarking criteria 00: TX PVID (0x07~0x08) > ACL VID > QID register 0x70 ~0x74 > RX PVID 01: TX PVID (0x07~0x08) > ACL VID > RX PVID 10: TX PVID (0x07~0x08) > ACL VID > VLAN table pri remark > RX PVID 11: TX PVID (0x07~0x08) > ACL VID > VLAN table pri remark > QID register 0x70~0x74 > RX PVID (QID register 0x70~0x74 only relative to { pri, cfi } , VID index will use RXPVID) bit[15:2] : port 2 ~ port 8 remarking criteria	RW	0xAAAA
0x76	802.1Q TAG {PCP, CFI} remarking criteria (port 9 ~ port 12 , 2bit / port) bit[7:0] : port 9 ~ port 12 remarking criteria bit[15:8] : Reserved	RW	0xAAAA
0x77	802.1Q TAG {PCP, CFI} remarking criteria (port 13 ~ port 16 , 2bit / port) bit[7:0] : Reserved bit[15:8] : port 13 ~ port 16 remarking criteria	RW	0xAAAA
0x78	802.1Q TAG {PCP, CFI} remarking criteria (port 17 ~ port 19 , 2bit / port) bit[3:0] : port 17 ~ port 18 remarking criteria bit[7:4] : Reserved bit[9:8] : port 19 remarking criteria	R/W	0x2AA
0x79	TX (802.1Q TAG) type-length field definition bit[15:0] : CTAG T/L field (Add / MDF)	R/W	0x8100
0x7A	Port 19 Special Tag setting bit[3:0] : sFlow packet length cutoff setting 4'd0 : 64 Bytes 4'd1 : 256 Bytes 4'd2 : 512 Bytes 4'd3 : 768 Bytes 4'd4 : 1024 Bytes 4'd5 : 1280 Bytes 4'd6 : 1536 Bytes 4'd7 : 1792 Bytes 4'd8 : 2048 Bytes 4'd9 : 2304 Bytes 4'd10 : 2560 Bytes 4'd11 : 2816 Bytes 4'd12 : 3072 Bytes 4'd13 : 3328 Bytes 4'd14/15: Disable length cutoff Note: (1) If original packet length < length cutoff setting ,packet length will not modify bit[4] : sFlow information add to special tag (28 Bytes) 1: Enable 0 : Disable bit[5] : PTP stamp information add to special tag (8 Bytes) 1: Enable 0 : Disable	R/W	0x3F

TxDMA Registers : Page 0x07			
Reg Addr.	Register Description	R/W	Default value
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

6.11 Output Queue Control Register

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
0x01	<p>Port Group A Out queue schedule mode / weight selection</p> <p>bit[2:0] : Schedule mode 0 : FIFO schedule 1 : WRR/WFQ/BW/TWRR 2 : SPx1 + WRR/WFQ/BW/TWRR x7 3 : SPx2 + WRR/WFQ/BW/TWRR x6 4 : SPx4 + WRR/WFQ/BW/TWRR x4 5 : SPx8 6 : LLQx1 + WFQ/BW/TWRR x7 (LLQ in WRR will switch to SP) 7 : LLQx2 + WFQ/BW/TWRR x6 (LLQ in WRR will switch to SP)</p> <p>bit[4:3] : BW throttle period sel / TWRR tickle unit 00 : 64 Kbit/s / (800 us/8000 us/80000 us @ 1G/100M/10M) 01 : 1 Mbit/s / (49.92 us/499.2 us/4992 us @ 1G/100M/10M) 10 : 2 Mbit/s / (24.32 us/243.2 us/2432 us @ 1G/100M/10M) 11 : 4 Mbit/s / (12.8 us/128 us/1280 us @ 1G/100M/10M)</p> <p>bit[6:5] : Queue method(00: WRR 01: BW 10: WFQ 11: TWRR)</p> <p>bit[7] : Delay Bound mode (Q7/Q6/Q5/Q4/Q3/Q2/Q1) (Q0 queue out only when Q7~Q1 is empty) must set bit[6:5] = 10/01, at the same time</p> <p>bit[8] : Q0 BE(best effort) queue disable (only bit[7] = 1) (Q0 is also delay bound queue if disable BE)</p> <p>bit[9] : WRED Drop enable (must also set 0x53/0x54) bit[10] : Delay Bound/LLQ Pause-Backpressure enable (will enable automatically if 0x01[6:5]=01/10 & 0x01[7] =1)</p> <p>bit[11] : Priority remap enable (0: CPU 1: Std) bit[14:12] : Reserved bit[15] : Queue schedule ratio value "0" definition BW/WFQ/TWRR (0: eq value1 1: Stop & hold packet)</p>	R/W	0x0100
0x02	<p>Port Group A Out queue schedule ratio 0</p> <p>bit[7:0] : Q0 weight / bandwidth allocate / bit[15:8] : Q1 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit</p>	R/W	0x0000
0x03	<p>Port Group A Out queue schedule ratio 1</p> <p>bit[7:0] : Q2 weight / bandwidth allocate / bit[15:8] : Q3 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit</p>	R/W	0x0000
0x04	<p>Port Group A Out queue schedule ratio 2</p> <p>bit[7:0] : Q4 weight / bandwidth allocate / bit[15:8] : Q5 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit</p>	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
0x05	Port Group A Out queue schedule ratio 3 bit[7:0] : Q6 weight / bandwidth allocate / bit[15:8] : Q7 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit)	R/W	0x0000
	Note 1: if 0x0E ~ 0x13 SRP parameter is setup with value > 0 , Q7 BW = mg_oq_lan_ratio3[15:8]x 64 Bytes/ slot time Q6 BW = mg_oq_lan_ratio3[7:0] x 64 Bytes / slot time Note 2: The LAN port max BW (if port SRP parameter > 0) Q7 BW = mg_oq_lan_max_bw3[15:8]x 64 Bytes/ slot time Q6 BW = mg_oq_lan_max_bw3[7:0] x 64 Bytes / slot time Note 3: If Delay bound mode is enable , Per Queue latency limit = ratio x {16us, 64us, 256us, 1024us}(ref 0x69[10:9])		
0x06	Port Group A Out queue 0 latency threshold bit[7:0] : Q0 latency threshold bit[15:8] : Q1 latency threshold	R/W	0x80FF
0x07	Port Group A Out queue 1 latency threshold bit[7:0] : Q2 latency threshold bit[15:8] : Q3 latency threshold	R/W	0x2040
0x08	Port Group A Out queue 2 latency threshold bit[7:0] : Q4 latency threshold bit[15:8] : Q5 latency threshold	R/W	0x0810
0x09	Port Group A Out queue 3 latency threshold bit[7:0] : Q6 latency threshold bit[15:8] : Q7 latency threshold	R/W	0x0204
0x0A	Port Group A Out queue Max Bandwidth bit[7:0] : Q0 max bandwidth bit[15:8] : Q1 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x0B	Port Group A Out queue Max Bandwidth bit[7:0] : Q2 max bandwidth bit[15:8] : Q3 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x0C	Port Group A Out queue Max Bandwidth bit[7:0] : Q4 max bandwidth bit[15:8] : Q5 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x0D	Port Group A Out queue Max Bandwidth bit[7:0] : Q6 max bandwidth bit[15:8] : Q7 max bandwidth (value =0 : unlimited) Ethernet AV setup: The LAN port max BW (if port 0x0E ~0x13 SRP parameter > 0) Q7 BW = mg_oq_lan_max_bw3[15:8]x 64 Bytes/ slot time Q6 BW = mg_oq_lan_max_bw3[7:0] x 64 Bytes / slot time	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
0x0E	<p>Ethernet AV SRP BW Credit-shaper parameter setup</p> <p>bit[2:0] : port 01 bit[5:3] : port 02 bit[8:6] : port 03 bit[11:9] : port 04 bit[14:12] : port 05</p> <p>SRP parameter (sche mode must : WFQ / BW /TWRR) (250 us *n : reg0x66[13:11])</p> <p>000 : Disable 001 : Q7.125 us 010 : Q7.250 us * n 011 : Q7.125 us & Q6.125 us 100 : Q7.125 us & Q6.250 us * n 101 : Q7.250 us *n & Q6.250 us * n</p> <p>(Must set: Group A 0x0D Q7/Q6 max bandwidth → As MAX Threshold 0x09 Q7/Q6 latency threshold → As Idle Slope 0x05 Q7/Q6 bandwidth allocate → As min BW threshold</p> <p>Group B 0x84 Q7/Q6 max bandwidth → As MAX Threshold 0x80 Q7/Q6 latency threshold → As Idle Slope 0x7C Q7/Q6 bandwidth allocate → As min BW threshold</p> <p>For Credit Shaped BW control, MAX must > min BW Threshold,</p>	R/W	0x0000
0x0F	<p>Ethernet AV SRP BW Credit-shaper parameter setup</p> <p>bit[2:0] : port 6 bit[5:3] : port 7 bit[8:6] : port 8 bit[11:9] : port 9 bit[14:12] : port 10</p>	R/W	0x0000
0x10	<p>Ethernet AV SRP BW Credit-shaper parameter setup</p> <p>bit[2:0] : port 11 bit[5:3] : port 12 bit[15:6] : Reserved</p>	R/W	0x0000
0x11	Reserved		
0x12	<p>Ethernet AV SRP BW Credit-shaper parameter setup</p> <p>bit[2:0] : port 13 bit[5:3] : port 14 bit[8:6] : port 15 bit[11:9] : port 16 bit[14:12] : port 17</p>	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
0x13	Ethernet AV SRP BW Credit-shaper parameter setup bit[2:0] : port 18 bit[8:3] : Reserved bit[11:9] : port 19	R/W	0x000
0x14	port 1 TX Priority remap data bit[2:0] : Priority 0 remap bit[5:3] : Priority 1 remap bit[8:6] : Priority 2 remap bit[11:9] : Priority 3 remap bit[14:12] : Priority 4 remap	R/W	0x4688
0x15	port 1 TX Priority remap data bit[2:0] : Priority 5 remap bit[5:3] : Priority 6 remap bit[8:6] : Priority 7 remap Priority remapping : TX priority remapping (PG08.0xB2~0xB3 > PG08.0x14 ~ 0x4D) > RX priority remapping (PG06.0x24~0x5D) > ACL DSCP remark addr / VLAN Table Remark pri (PG06.0x17 ~ 0x1A)	R/W	0x1F5
0x16	port 2 TX Priority remap data bit[2:0] : Priority 0 remap bit[5:3] : Priority 1 remap bit[8:6] : Priority 2 remap bit[11:9] : Priority 3 remap bit[14:12] : Priority 4 remap	R/W	0x4688
0x17	port 2 TX Priority remap data bit[2:0] : Priority 5 remap bit[5:3] : Priority 6 remap bit[8:6] : Priority 7 remap	R/W	0x1F5
0x18 ~ 0x2B	port 3 ~ port 12 TX Priority remap data	R/W	0x4688 ~ 0x1F5
0x2C ~ 0x3B	Reserved		
0x3C ~ 0x47	port 13 ~ port 18 TX Priority remap data	R/W	0x4688 ~ 0x1F5
0x48 ~ 0x4B	Reserved		
0x4C 0x4D	port 19 TX Priority remap data	R/W	0x4688 0x1F5

Output Queue Register : Page 0x08							
Reg Addr.	Register Description	R/W	Default value				
0x4E	Out queue Random Early Detect threshold bit[3:0] : WRED threshold for ACT0 bit[7:4] : WRED threshold for ACT1 bit[11:8] : WRED threshold for ACT2 bit[15:12] : WRED threshold for ACT3	R/W	0x8421				
	WRED Drop probability			Q7/Q6	Q5/Q4	Q3/Q2	Q1/Q0
	oq_wred_cnt > ACT3			1/(0x52 thr)	1/(0x51 thr)	1/(0x50 thr)	1/(0x4F thr)
	ACT2 <oq_wred_cnt < ACT3			x	1/(0x52 thr)	1/(0x51 thr)	1/(0x50 thr)
	ACT1 <oq_wred_cnt < ACT2			x	x	1/(0x52 thr)	1/(0x51 thr)
	ACT0<oq_wred_cnt < ACT1			x	x	x	1/(0x52 thr)
	oq_wred_cnt < ACT0			x	x	x	x
0x4F	WRED markA weight threshold bit[8:0] : mark weight threshold drop rate(1/packet) = 1/(threshold)	R/W	0x001				
0x50	WRED markB weight threshold bit[8:0] : mark weight threshold drop rate(1/packet) = 1/(threshold)	R/W	0x002				
0x51	WRED markC weight threshold bit[8:0] : mark weight threshold drop rate(1/packet) = 1/(threshold)	R/W	0x003				
0x52	WRED markD weight threshold bit[8:0] : mark weight threshold drop rate(1/packet) = 1/(threshold)	R/W	0x004				
0x53	Out queue WRED enable bit[11:0] : port 1 ~ port 12 Out Queue WRED ability 1: Enable 0 : Disable	R/W	0x0000				
0x54	Out queue WRED enable bit[12][9:4]: port 13 ~ port 19 Out Queue WRED ability 1: Enable 0 : Disable	R/W	0x0000				
0x55	port 1 ~ port 2 queue based SBM (static bandwidth management / DBM (Dynamic bandwidth management) select bit[7:0] : port 1 Q7~Q0 SBM /DBM select (1: SBM 0: DBM) bit[15:8] : port 2 Q7~Q0 SBM /DBM select must set mg_oq_sche_mode[6:5] = 01 (Out queue BW-mode) <u>(DBM must work with 0x64~0x65 BW range set)</u> <u>(DBM will be disabled internally if 0x64 ~ 0x65 TX port BW range is not set.)</u> ex: throttle enable: 1: traffic stop when hit bandwidth limit threshold (SBM) 0: Traffic between Bandwidth MAX , min (DBM)		0xFFFF				

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
	<p>Note1: Per queue bandwidth range control must set PG08.0x01[6:5] = 2'b01 if belong to Port Group A PG08.0x76[6:5] = 2'b01 if belong to Port Group B PG08.0x55~0x63 (0: enable queue bw range control 1: only bandwidth limited) For Port Group A , PG08.0x02~0x05 used as Bandwidth-min PG08.0x0A~0x0D used as Bandwidth-MAX For Port Group B , PG08.0x79~0x7C used as Bandwidth-min PG08.0x81~0x84 used as Bandwidth-MAX</p> <p>Note2: If MAX < min , min BW will not be assured. It only show BW limited at MAX value</p>		
0x56 ~ 0x5A	<p>port 3 ~ port 12 queue based SBM (static bandwidth management / DBM (Dynamic bandwidth management) select bit[7:0] : Pn Q7~Q0 SBM /DBM select (1: SBM 0: DBM) bit[15:8] : Pn+1 Q7~Q0 SBM /DBM select</p>	R/W	0xFFFF
0x5B ~ 0x5E	Reserved		
0x5F ~ 0x61	<p>port 13 ~ port 18 queue based SBM (static bandwidth management / DBM (Dynamic bandwidth management) select bit[7:0] : Pn Q7~Q0 SBM /DBM select (1: SBM 0: DBM) bit[15:8] : Pn+1 Q7~Q0 SBM /DBM select</p>	R/W	0xFFFF
0x62	Reserved		
0x63	<p>port 19 queue based SBM (static bandwidth management / DBM (Dynamic bandwidth management) select bit[7:0] : port 19 Q7~Q0 SBM /DBM select (1: SBM 0: DBM) bit[15:8] : Reserved</p>	R/W	0xFF
0x64	<p>Queue DBM (Dynamic Bandwidth management) enable bit[11:0] : mg_oq_bw_range_en port 1 ~ port 12</p>	R/W	0x0000
0x65	<p>Queue DBM (Dynamic Bandwidth management) enable bit[12][9:4] : mg_oq_bw_range_en port 13 ~ port 19</p>	R/W	0x0000
0x66	<p>Out queue aging time bit[7:0]: Out queue aging time =(1~2)* value* 100 ms bit[8] : fast aging enable (unit = 1.638 ms) bit[10:9] : Out queue latency timing unit (Delay Bound mode) 0: 16 us/ 64us / 1024 us (Giga/100/10) 1 : 64 us 2: 256 us 3: 1024 us bit[13:11] : SRP macro slot period threshold (unit 250us) 000 : 250 us 001 : 500 us 010 : 1 ms 011 : 2 ms 100 : 4 ms 101/110/111 : 8 ms</p>	R/W	0x8000

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
	bit[8] : Q0 BE(best effort) queue disable (only bit[13] = 1) (Q0 is also delay bound queue if disable BE) bit[9] : Port Group B schedule mode setting enable 0: set as Group A 1: set as Group B (PG08.0x01[8:0]) (PG08.0x76[8:0])		
0x77	Out queue Port Group A/B selection bit[11:0] : port 1 ~ port 12 Group A/B select 1: Group B 0 : Group A	R/W	0x0000
0x78	Out queue Port Group A/B selection bit[12][9:4] : port 13 ~ port 19 Group A/B select 1: Group B 0 : Group A	R/W	0x0000
0x79	Port Group B Out queue schedule ratio 0 bit[7:0] : Q0 weight / bandwidth allocate / bit[15:8] : Q1 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit	R/W	0x0000
0x7A	Port Group B Out queue schedule ratio 1 bit[7:0] : Q2 weight / bandwidth allocate / bit[15:8] : Q3 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit	R/W	0x0000
0x7B	Port Group B Out queue schedule ratio 2 bit[7:0] : Q4 weight / bandwidth allocate / bit[15:8] : Q5 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit	R/W	0x0000
0x7C	Port Group B Out queue schedule ratio 3 bit[7:0] : Q6 weight / bandwidth allocate / bit[15:8] : Q7 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit Note 1: if 0x61 SRP parameter is setup with value > 0 , Q7 BW = mg_oq_wan_ratio3[15:8]x 64 Bytes/ slot time Q6 BW = mg_oq_wan_ratio3[7:0] x 64 Bytes / slot time Note 2: The WAN port max BW (if port SRP parameter > 0) Q7 BW = mg_oq_wan_max_bw3[15:8]x 64 Bytes/ slot time Q6 BW = mg_oq_wan_max_bw3[7:0] x 64 Bytes / slot time	R/W	0x0000
0x7D	Port Group B Out queue 0 latency threshold bit[7:0] : Q0 latency threshold bit[15:8] : Q1 latency threshold	R/W	0x80FF
0x7E	Port Group B Out queue 1 latency threshold bit[7:0] : Q2 latency threshold bit[15:8] : Q3 latency threshold	R/W	0x2040
0x7F	Port Group B Out queue 2 latency threshold bit[7:0] : Q4 latency threshold bit[15:8] : Q5 latency threshold	R/W	0x0810

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
0x80	Port Group B Out queue 3 latency threshold bit[7:0] : Q6 latency threshold bit[15:8] : Q7 latency threshold	R/W	0x0204
0x81	Port Group B Out queue Max Bandwidth bit[7:0] : Q0 max bandwidth bit[15:8] : Q1 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x82	Port Group B Out queue Max Bandwidth bit[7:0] : Q2 max bandwidth bit[15:8] : Q3 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x83	Port Group B Out queue Max Bandwidth bit[7:0] : Q4 max bandwidth bit[15:8] : Q5 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x84	Port Group B Out queue Max Bandwidth bit[7:0] : Q6 max bandwidth bit[15:8] : Q7 max bandwidth (value =0 : unlimited) Ethernet AV setup: The WAN port max BW (if port SRP parameter > 0) Q7 BW = mg_oq_wan_max_bw3[15:8]x 64 Bytes/ slot time Q6 BW = mg_oq_wan_max_bw3[7:0] x 64 Bytes / slot time	R/W	0x0000
0x85	Egress Rate control for port 1 bit[13:0] : Output Rate control bit[15:14] : 00 : write Both PIR/CIR 01 : write PIR 10 : read CIR 11 : read PIR (CIR : committed information rate : 2 nd bucket token rate) (PIR : peak information rate : 1 st bucket token rate)	R/W	0x0000
0x86 ~ 0x90	Egress Rate control for port 2 ~ port 12 bit[13:0] : Output Rate control bit[15:14] : 00 : write Both PIR/CIR 01 : write PIR 10 : read CIR 11 : read PIR (CIR : committed information rate : 2 nd bucket token rate) (PIR : peak information rate : 1 st bucket token rate)	R/W	0x0000
0x91 ~ 0x98	Reserved		

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
0x99 ~ 0x9E	Egress Rate control for port 13 ~ port 18 bit[13:0] : Output Rate control bit[15:14] : 00 : write Both PIR/CIR 01 : write PIR 10 : read CIR 11 : read PIR (CIR : committed information rate : 2 nd bucket token rate) (PIR : peak information rate : 1 st bucket token rate)	R/W	0x0000
0x9F 0xA0	Reserved		
0xA1	Egress Rate control for port 19 bit[13:0] : Output Rate control bit[15:14] : 00 : write Both PIR/CIR 01 : write PIR 10 : read CIR 11 : read PIR (CIR : committed information rate : 2 nd bucket token rate) (PIR : peak information rate : 1 st bucket token rate)	R/W	0x0000
0xA2	port 1 ~ port 2 Out queue rate control setting bit[7:0] : port 1 Q7~Q0, disable egress rate calculation. bit[15:8] : port 2 Q7~Q0, disable egress rate calculation. (ex: if WFQ mode, set Q6~Q0 has 75% bandwidth take into egress rate count , then Q7 take the (100% - 75%) Bandwidth.	R/W	0x0000
0xA3 ~ 0xA7	port 3 ~ port 12 queue rate control setting bit[7:0] : port xx Q7~Q0, disable egress rate calculation. bit[15:8] : port xy Q7~Q0, disable egress rate calculation. (ex: if WFQ mode, set Q6~Q0 has 75% bandwidth take into egress rate count , then Q7 take the (100% - 75%) Bandwidth.	R/W	0x0000
0xA8 ~ 0xAB	Reserved		
0xAC ~ 0xAE	port 13 ~ port 18 queue rate control setting bit[7:0] : port xx Q7~Q0, disable egress rate calculation. bit[15:8] : port xy Q7~Q0, disable egress rate calculation. (ex: if WFQ mode, set Q6~Q0 has 75% bandwidth take into egress rate count , then Q7 take the (100% - 75%) Bandwidth.	R/W	0x0000
0xAF	Reserved		

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
0xB0	<p>port 19 queue rate control setting bit[7:0] : port 19 Q7~Q0, disable egress rate calculation.</p> <p>(ex: if WFQ mode, set Q6~Q0 has 75% bandwidth take into egress rate count , then Q7 take the (100% - 75%) Bandwidth. (ex: if BW mode, set Q3~Q0 has total 25 % bandwidth take into egress rate Count , and Q7~Q4 total can use 75 % , and per Queue can setup SBM/DBM separately.</p>	R/W	0x00
0xB1	<p>Out queue parameter setup bit[3:0]: 2nd bucket size[3:0] (leaky bucket size)</p> <p>4'b0000: 4 KB 4'b0001: 8 KB 4'b0010: 16 KB 4'b0011: 32 KB 4'b0100: 64 KB 4'b0101: 128 KB 4'b0110: 256 KB 4'b0111: 512 KB 4'b1000: 1024 KB 4'b1001: 2 KB 4'b1010: 1 KB 4'b1011: 512 B 4'b1100: 256 B 4'b1101: 128 B 4'b1110: 64 B 4'b1111: 32 B</p> <p>The max. output bytes no. in one period time = Rate control configure value x 64k bps (4096 Bytes / 500 ms)(512 Bytes / 62.5 ms)</p> <p>bit[6:4]: Bandwidth period</p> <p>3'b000: (4096 Bytes / 500 ms) 3'b001: (2048 Bytes / 250 ms) 3'b010: (1024 Bytes / 125 ms) 3'b011: (512 Bytes / 62.5 ms) 3'b100: (256 Bytes / 31.25 ms) 3'b101: (128 Bytes / 15.625 ms) 3'b110: (64 Bytes / 7.8125 ms) 3'b111: (32 Bytes / 3.90625 ms)</p> <p>The max. output bytes no. in one period time = Rate control configure value x 64k bps (4096 Bytes / 500 ms)(512 Bytes / 62.5 ms)</p> <p>bit[7]: Out queue rate-jitter regulator enable for egress rate ctrl (Leaky Bucket Method 0: dis 1:en) 0 : Egress rate control using periodically Burst mode 1 : Egress rate control using leaky bucket mode</p>	R/W	0x82FF

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
	bit[8]: egress rate control trigger pause / drop enable (0 :shaping traffic 1: policing traffic) bit[9]: Out queue rate-jitter regulator enable burst mode for egress rate control (Token Bucket method 0: dis 1:en) bit[10]: enable per queue pause / drop for BW mode (if PG08.0xB1[11:10] =10, enable depend on PG08.0x55~0x63 if PG08.0xB1[11:10] =11, all queue is enable, regardless 0x55~0x63 bit[11]: enable out queue BW / WFQ pause / drop (BW / WFQ throttle) bit[13:12]: TWRR Tickle unit type 00 : fixed Giga (51.2ms /3.19ms /1.55ms /0.82ms) 01 : fixed 100M (512ms /31.9ms /15.5ms /8.2ms) 10 : fixed 10 M (5120ms /319ms /155ms /82ms) 11 : bit time (51.2 /3.19 /1.55 /0.82)x10 ⁶ bit time bit[14] : Out queue congest condition (1: port based 0: queue based) bit[15] : Queue bandwidth bytes cnt keep residue at Bw-assured mode (precise BW for jumbo packet)		
0xB2	TX queue mapping from TX "Port priority" bit[11:0] : mg_oq_wlan_pri_en port 1 ~ port 12	R/W	0x0000
0xB3	TX queue mapping from TX "Port priority" bit[12][9:4] : mg_oq_wlan_pri_en port 13 ~port 19 Priority remapping : TX priority remapping (PG08.0xB2~0xB3 > PG08.0x14~0x4D) > RX priority remapping (PG06.0x24~0x5D) > ACL DSCP remark addr / VLAN Table Remark pri (PG06.0x17~0x1A)	R/W	0x0000
0xB4	bit[2:0]: Out queue rate control rate jitter enable burst mode burst size (1st Token Bucket size). 0 : 4 KB 1 : 16 KB 2 : 32 KB 3 : 64 KB 4 : 128 KB 5 : 256 KB 6 : 512 KB 7 : 1024 KB bit[3] : WRED TAIL DROP (1:Enable 0:Disable) bit[4] : WRED IP ECN enable WRED notify explicit congestion notification in IP header. (Rule: ip packet , hit WRED drop , ECN bit = 01/10) bit[5] : WRED mode 1 enable (drop instantly without oq_rd_holb_cnt) bit[6] : WRED normal en (WRED enable ignore Delay bound weighted amount setting) bit[7] : WRED HEAD DROP (1:Enable 0:Disable)	R/W	0x068

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
	bit[8] : Out queue aging priority 0: Normal packet > Aging out packet (send normal first , aging packet still in queue , Use more Buffer) 1: Aging out packet > normal packet (stop TX and switch to aging, affect TX rate , less buffer used)		
0xB5	port 1 ~ port 16 Out queue pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x22F
0xB6	port 1 ~ port 16 Out queue pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x1E1
0xB7	port 17 ~ port 18 Out queue pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x22F
0xB8	port 17 ~ port 18 Out queue pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x1E1
0xB9	port 19 Out queue pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x22F
0xBA	port 19 Out queue pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x1E1
0xBB	Out queue Q0 pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x07F
0xBC	Out queue Q0 pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x01F
0xBD	Out queue Q1 pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x07F
0xBE	Out queue Q1 pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x01F
0xBF	Out queue Q2 pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x07F
0xC0	Out queue Q2 pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x01F
0xC1	Out queue Q3 pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x07F
0xC2	Out queue Q3 pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x01F
0xC3	Out queue Q4 pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x07F
0xC4	Out queue Q4 pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x01F
0xC5	Out queue Q5 pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x07F
0xC6	Out queue Q5 pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x01F

Output Queue Register : Page 0x08			
Reg Addr.	Register Description	R/W	Default value
0xC7	Out queue Q6 pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x07F
0xC8	Out queue Q6 pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x01F
0xC9	Out queue Q7 pause on threshold setting bit[10:0] : out queue pause on threshold	R/W	0x07F
0xCA	Out queue Q7 pause off threshold setting bit[10:0] : out queue pause off threshold	R/W	0x01F
0xCB 0xCD	Reserved		
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

6.12 PTP Control Register

PTP Register : Page 0x09			
Reg Addr.	Register Description	R/W	Default value
0x00	PTP clock reset bit bit[0] : 1: clear the PTP clock reference register configuration to default reg.0x10 reg.0x11 reg.0x12 reg.0x13 reg.0x14 reg.0x15 reg.0x16 reg.0x17 0: no action	SC	0x0
0x01	PTP time stamps read command bit[3:0] : time stamp address bit[4] : ingress/egress index 1 : egress time stamps 0 : ingress time stamps bit[9:5] : port index ,from 0x00~0x0B,0x14~0x19,0x1C (port 1 ~ port 19 and event) bit[11:10] : do not care bit[12] : data register (0x0B/0x0C/0x0D/0x0E) read indication 1 : read back data is the data you last written in 0 : the read back data is time stamp data or current PTP time bit[13] : Reserved bit[14] : Reserved bit[15] : command trigger 1 : issue a command 0 : idle	R/W	0x0000
0x02	PTP general configuration register bit[0] : Enable the PTP clock 1: Enable the PTP real time clock 0: Disable the PTP real time clock bit[1] : MAC PTP stamp buffer overwrite enable 1: write buffers from 0 to 15 in circles 0: no more write when buffers full bit[2] : Programmable output enable 1: Enable the output of programmable clock 0: Disable the output bit[3] :EVENT input trigger positive edge detection 1: Enable positive edge detection 0: Disable positive edge detection bit[4] :EVENT input trigger falling edge detection 1: Enable falling edge detection 0: Disable Falling edge detection bit[5] : EVENT PTP stamp buffer overwrite enable 1: write buffers from 0 to 7 in circles 0: no more write when buffers full	R/W	0x000

PTP Register : Page 0x09			
Reg Addr.	Register Description	R/W	Default value
	bit[6]: PTP Trigger Out Function Enable 1: Enable PTP trigger out function 0: Disable PTP trigger out function bit[7]: PTP Trigger Out "Type" Selection 1: Period 0: Pulse bit[8]: PTP Trigger Out "High Duration" Setting 1: Multiple Cycles (refers to 0x18 register, bit[15:8]) 0: One Cycle bit[10:9]: PTP Pulse Per Second Pin (ptp_pps) source selection 0: PTP Pulse Per Second (ptp_pps) 1: PTP programming output clock (reference: 0x02[2]) 2: PTP Trigger output clock 3: Reserve		
0x03	PTP port time stamp enable bit[0] : port 1 ingress time stamp enable bit[1] : port 1 egress time stamp enable bit[2] : port 2 ingress time stamp enable bit[3] : port 2 egress time stamp enable bit[4] : port 3 ingress time stamp enable bit[5] : port 3 egress time stamp enable bit[6] : port 4 ingress time stamp enable bit[7] : port 4 egress time stamp enable bit[8] : port 5 ingress time stamp enable bit[9] : port 5 egress time stamp enable bit[10] : port 6 ingress time stamp enable bit[11] : port 6 egress time stamp enable bit[12] : port 7 ingress time stamp enable bit[13] : port 7 egress time stamp enable bit[14] : port 8 ingress time stamp enable 1 : Enable, 0 : Disable bit[15] : port 8 egress time stamp enable 1 : Enable, 0 : Disable	R/W	0x0000
0x04	port 9 ~ port 12 PTP time stamp enable bit[7:0] : (same definition with register 0x03, except port 9 ~ port 12) bit[15:8] : Reserved	R/W	0x0000
0x05	port 13 ~ port 16 PTP time stamp enable bit[7:0] : Reserved bit[15:8] : (same definition with register 0x03, except port 13 ~ port 16)	R/W	0x0000
0x06	EVENT and port 17 ~ port 19 PTP time stamp enable bit[3:0] : (same definition with register 0x03, except port 17 ~ port 18) bit[7:4] : Reserved bit[9:8] : (same definition with register 0x03, except port 19) bit[10] : EVENT input time stamp enable	R/W	0x0000

PTP Register : Page 0x09			
Reg Addr.	Register Description	R/W	Default value
0x07	PTP time stamp clear register bit[0] : port 1 ingress stamp counter/full notification clear bit[1] : port 1 egress stamp counter/full notification clear bit[2] : port 2 ingress stamp counter/full notification clear bit[3] : port 2 egress stamp counter/full notification clear bit[4] : port 3 ingress stamp counter/full notification clear bit[5] : port 3 egress stamp counter/full notification clear bit[6] : port 4 ingress stamp counter/full notification clear bit[7] : port 4 egress stamp counter/full notification clear bit[8] : port 5 ingress stamp counter/full notification clear bit[9] : Pport 5 egress stamp counter/full notification clear bit[10] : port 6 ingress stamp counter/full notification clear bit[11] : port 6 egress stamp counter/full notification clear bit[12] : port 7 ingress stamp counter/full notification clear bit[13] : port 7 egress stamp counter/full notification clear bit[14] : port 8 ingress stamp counter/full notification clear 1 : clear to zero, 0 : no action bit[15] : port 8 egress stamp counter/full notification clear 1 : clear to zero, 0 : no action	SC	0x0000
0x08	port 9 ~ port 12 PTP time stamp clear register bit[7:0] : (same definition with register 0x07, except port 9 ~ port 12) bit[15:8] : Reserved	SC	0x0000
0x09	port 13 ~ port 16 PTP time stamp clear register bit[7:0] : Reserved bit[15:8] : (same definition with register 0x07, except port 13 ~ port 16)	SC	0x0000
0x0A	EVENT and port 17 ~ port 19 PTP time stamp clear register bit[3:0] : (same definition with register 0x07, except port 17 ~ port 18) bit[7:4] : Reserved bit[9:8] : (same definition with register 0x07, except port 19) bit[10] : EVENT input time stamp clear	SC	0x0000
0x0B	PTP time data for nano-second bit[15:0] : nano-second[15:0]	R/W	0x0000
0x0C	PTP time data for nano-second bit[13:0] : nano-second[29:16]	R/W	0x0000
0x0D	PTP time data for second bit[15:0] : second[15:0]	R/W	0x0000
0x0E	PTP time data for second bit[15:0] : second[31:16]	R/W	0x0000

PTP Register : Page 0x09			
Reg Addr.	Register Description	R/W	Default value
0x0F	PTP clock control register bit[0] : command trigger 1: issue a command 0: idle bit[2:1] : 00 : read back the current PTP clock into register 0x0B~0x0E 01 : Set the PTP time date 0x0B~0x0E to current PTP clock 10 : Add the PTP time date 0x0B~0x0E to current PTP clock 11 : Sub the PTP time date 0x0B~0x0E from current PTP clock Note! The register bit 0x01[12] should be "0" for reading back the current clock from 0x0B~0x0E	R/W SC	0x0000
0x10	PTP frequency addend value configuration Set the PTP real time clock divided from source (125MHz) bit[15:0] : addend value for the frequency compensation [15:0]	R/W	0x0000
0x11	PTP frequency addend value configuration Set the PTP real time clock divided from source (125MHz) bit[15:0] : addend value for the frequency compensation [31:16]	R/W	0x8000
0x12	PTP clock period register The period of PTP real time clock set bit[15:0] : 16bits clock period in nano-second Note : (a) The default clock period is 16ns,modification is not recommend (b) this register should be derived from register 0x10 and 0x11	R/W	0x0010
0x13	PTP frequency compensation configuration based on reg.0x10 and 0x11 bit[15:0] : the frequency compensation value [15:0]	R/W	0x0000
0x14	PTP frequency compensation configuration based on reg.0x10 and 0x11 bit[9:0] : the frequency compensation value [25:16]	R/W	0x000
0x15	PTP frequency compensation duration in numbers of PTP clock cycles bit[15:0] : duration in numbers of PTP clock cycles [15:0]	R/W	0x0000
0x16	PTP frequency compensation duration in numbers of PTP clock cycles bit[9:0] : duration in numbers of PTP clock cycles [25:16] Note : This register takes actively only when reg.0x17[1]=1, and the clock cycle is based PTP period defined in reg.0x10 and 0x11	R/W	0x000
0x17	PTP frequency compensation control register bit[0] : command trigger 1: frequency correction enable 0: Disable bit[1] : 1 : use the rate duration set in registers 0x15 and 0x16 0 : always correction bit[2] : 1 : frequency sub 0 : frequency add	R/W	0x0

PTP Register : Page 0x09			
Reg Addr.	Register Description	R/W	Default value
0x18	PTP programmable output configuration bit[7:0] : the “low” duration in numbers of PTP clock cycles bit[15:8] : the “high” duration in numbers of PTP clock cycles Note : This register takes actively only when reg.0x02[2]=1 and the clock cycle is based PTP period defined in reg.0x10 and 0x11	R/W	0x0000
0x19	PTP interrupt indication enable when a frame has been time stamped bit[0] : port 1 ingress time stamp interrupt enable bit[1] : port 1 egress time stamp interrupt enable bit[2] : port 2 ingress time stamp interrupt enable bit[3] : port 2 egress time stamp interrupt enable bit[4] : port 3 ingress time stamp interrupt enable bit[5] : port 3 egress time stamp interrupt enable bit[6] : port 4 ingress time stamp interrupt enable bit[7] : port 4 egress time stamp interrupt enable bit[8] : port 5 ingress time stamp interrupt enable bit[9] : port 5 egress time stamp interrupt enable bit[10] : port 6 ingress time stamp interrupt enable bit[11] : port 6 egress time stamp interrupt enable bit[12] : port 7 ingress time stamp interrupt enable bit[13] : port 7 egress time stamp interrupt enable bit[14] : port 8 ingress time stamp interrupt enable 1: Enable 0: Disable bit[15] : port 8 egress time stamp interrupt enable 1: Enable 0: Disable	R/W	0x0000
0x1A	port 9 ~ port 12 PTP time stamp interrupt enable bit[7:0] : (same definition with register 0x19, except port 9 ~ port 12) bit[15:8] : Reserved	R/W	0x0000
0x1B	port 13 ~ port 16 PTP time stamp interrupt enable bit[7:0] : Reserved bit[15:8] : (same definition with register 0x19, except port 13 ~ port 16)	R/W	0x0000
0x1C	EVENT and port 17 ~ port 19 PTP time stamp interrupt enable bit[3:0] : (same definition with register 0x19, except port 17 ~ port 18) bit[7:4] : Reserved bit[9:8] : (same definition with register 0x19, except port 19) bit[10] : EVENT input time stamp interrupt enable	R/W	0x0000
0x1D	PTP time stamp status register bit[0] : port 1 stamp status for ingress 1: notify a time stamp has been write into buffer 0: no time stamp wrote after last buffer read bit[1] : port 1 stamp status for egress 1: notify a time stamp has been write into buffer 0: no time stamp wrote after last buffer read bit[2] : port 2 stamp status for ingress bit[3] : port 2 stamp status for egress bit[4] : port 3 stamp status for ingress	RO	0x0000

PTP Register : Page 0x09			
Reg Addr.	Register Description	R/W	Default value
	bit[5] : port 3 stamp status for egress bit[6] : port 4 stamp status for ingress bit[7] : port 4 stamp status for egress bit[8] : port 5 stamp status for ingress bit[9] : port 5 stamp status for egress bit[10] : port 6 stamp status for ingress bit[11] : port 6 stamp status for egress bit[12] : port 7 stamp status for ingress bit[13] : port 7 stamp status for egress bit[14] : port 8 stamp status for ingress bit[15] : port 8 stamp status for egress Note : the status is cleared when any of the correspond buffers has been read		
0x1E	port 9 ~ port 12 PTP time stamp status register bit[7:0] : (same definition with register 0x1D, except port 9 ~ port 12) bit[15:8] : Reserved	RO	0x0000
0x1F	port 13 ~ port 16 PTP time stamp status register bit[7:0] : Reserved bit[15:8] : (same definition with register 0x1D, except port 13 ~ port 16)	RO	0x0000
0x20	EVENT and port 17 ~ port 19 PTP time stamp status register bit[3:0] : (same definition with register 0x1D, except port 17 ~ port 18) bit[7:4] : Reserved bit[9:8] : (same definition with register 0x1D, except port 19) bit[10] : EVENT input time stamp status register	RO	0x000
0x21	port 17 PTP ingress latency correction bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	R/W	0x0000
0x22	port 18 PTP ingress latency correction bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	R/W	0x0000
0x23 0x24	Reserved		
0x25	port 19 PTP ingress latency correction bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	R/W	0x0000
0x26	port 17 PTP egress latency correction bit[15:0] : correct the egress time by adding the latency correction (ns)	R/W	0x0000
0x27	port 18 PTP egress latency correction bit[15:0] : correct the egress time by adding the latency correction (ns)	R/W	0x0000
0x28 0x29	Reserved		
0x2A	port 19 PTP egress latency correction bit[15:0] : correct the egress time by adding the latency correction (ns)	R/W	0x0000

PTP Register : Page 0x09			
Reg Addr.	Register Description	R/W	Default value
0x2B	10M TP ingress latency correction (embedded PHY) bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	RO	0x0564
0x2C	100M TP ingress latency correction (embedded PHY) bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	RO	0x0140
0x2D	100M Fiber ingress latency correction (embedded PHY) bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	RO	0x0128
0x2E	10M TP egress latency correction (embedded PHY) bit[15:0] : correct the egress time by adding the latency correction (ns)	RO	0x0474
0x2F	100M TP egress latency correction (embedded PHY) bit[15:0] : correct the egress time by adding the latency correction (ns)	RO	0x0088
0x30	100M Fiber egress latency correction (embedded PHY) bit[15:0] : correct the egress time by adding the latency correction (ns)	RO	0x0088
0x31	PTP Specific Time Trigger Out data for nano-second bit[15:0]: nano-second [15:0]	R/W	0x0000
0x32	PTP Specific Time Trigger Out data for nano-second bit[15:0]: nano-second[29:16]	R/W	0x0000
0x33	PTP Specific Time Trigger Out data for second bit[15:0] : second[15:0]	R/W	0x0000
0x34	PTP Specific Time Trigger Out data for second bit[15:0] : second[31:16]	R/W	0x0000
0x35	PTP Specific Time Trigger Out Period Setting bit[15:0]: Period Value Setting[15:0]	R/W	0x0000
0x36	PTP Specific Time Trigger Out Period Setting. (Unit: RTC Rate) bit[15:0]: Period Value Setting[31:16] [Example] : The value is calculated as follows: If PTP real time clock is 62.5MHz (where Reg0x11: 0x8000), the 125us period should be setting as : 0x1e84 = 125us / 16ns Note : <ul style="list-style-type: none"> ● PTP Specific Time Trigger out Period Value == 0x0000h indicates disable the period function. ● PTP Specific Time Trigger out Period Value must large than “high duration cycles (0x18 register, bit[15:8])”; otherwise, it will be disable the period function. 	R/W	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

6.13 IRMP Control Register

IRMP Register : Page 0x0A			
Reg Addr.	Register Description	R/W	Default value
0x01	<p>IRMP operation</p> <p>bit[8:0] : The period of IRMP time out, the unit is “second” If no IRMP command is received in (bit[8:0]~bit[8:0]+1)sec., a granted port will be released and send out a goodbye frame (default value is 0x12C, 300sec)</p> <p>bit[11:9] : (Reserved)</p> <p>bit[12] : password is needed 1 : The IRMP should check password (default) 0 : no password needed</p> <p>bit[13] : The IRMP power abnormal indication enable 1 : when switch detects the power level is under threshold, a last gasp frame is send out by granted port (default) 0 : No power detection function</p> <p>bit[14] : IRMP topology function enable 1 : Enable (default) 0 : Disable</p> <p>bit[15] : Destination Address is limited to switch MAC address. 1 : IRMP check the DA of frame with the switch MAC address only 0 : IRMP check the DA of frame with switch MAC address and broadcast address (default)</p>	R/W	0x712C
0x02	<p>IRMP function enable for port 1 ~ port 12, 1 bit per port</p> <p>bit[0] : IRMP function enable for port 1 1 : IRMP enable (default) 0 : IRMP disable</p> <p>bit[11:1] : IRMP function enable for port 2 ~ port 12 The same definition with bit[0]</p>	R/W	0xFFFF
0x03	<p>IRMP function enable for port 13 ~ port 19, 1 bit per port</p> <p>bit[12][9:4] : IRMP function enable for port 13 ~ port 19 The same definition with register 0x02</p>	R/W	0x1FFF
0x04	<p>IRMP ether-type definition</p> <p>bit[15:0] : The ether-type definition of IRMP (default : 16’h0806)</p>	R/W	0x8931
0x05	<p>IRMP sub-type definition</p> <p>bit[15:0] : The sub-type definition of IRMP (default : 16’hFFFE)</p>	R/W	0xFFFE
0x06	<p>Vender ID [15:0]</p> <p>bit[15:0] : The vender identifier [15:0] (default : 0xC300)</p>	R/W	0xC300
0x07	<p>Vender ID [31:16]</p> <p>bit[15:0] : The vender identifier [31:16] (default : 0x0090)</p>	R/W	0x0090
0x08	<p>Device ID and Version</p> <p>bit[3:0] : The IRMP version control (default : 4’h0)</p> <p>bit[15:4] : The device identifier [11:0] (default : 12’h829)</p>	R/W	0x8290

IRMP Register : Page 0x0A			
Reg Addr.	Register Description	R/W	Default value
0x09	IRMP Password [15:0] bit[15:0] : The IRMP password [15:0] (default : 16'h0000)	R/W	0x0000
0x0A	IRMP password [31:16] bit[15:0] : The IRMP password [31:16] (default : 16'h0000)	R/W	0x0000
0x0B	IRMP connect ID bit[15:0] : The random ID generated for each connection	RO	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

Note : The IRMP operation flow, please refer to IRMP application note.

6.14 Advance EEPROM code Register

Advance EEPROM code Register : Page 0x0B			
Reg Addr.	Register Description	R/W	Default value
0x01	advance EEPROM operation bit[0] : The advance EEPROM function enable 1 : Enable 0 : Disable (default) bit[1] : The advance EEPROM code start point bit[16] (MSB) (refer to register 0x02) bit[2] : action code hold 1 : hold the command for debugging 0 : normal processing command code (default) bit[3] : action code trigger again 1 : re-start the action code from start address 0 : normal (default)	R/W	0x0
0x02	The advance EEPROM code start bit[15:0] bit[15:0] : start point Note : Four EEPROM bytes to form a command code, The code begin at EEPROM address is {start point [16:0], 2'b00} Note : MSB bit[16] is defined in 0x01[1]	R/W	0x0000
0x03	Data buffer 0 for advance EEPROM code bit[15:0] : buffer_0	RO	0x0000
0x04 ~ 0x0A	Data buffer 1 ~ data buffer 7 for advance EEPROM code bit[15:0] : buffer	RO	0x0000
0x0B	operation temporary 0 for advance EEPROM code bit[15:0] : temp_0	RO	0x0000
0x0C ~ 0x0E	operation temporary 1 ~ 3 for advance EEPROM code bit[15:0] : temp_1 ~ 3	RO	0x0000
0x0F	Logic result of advance EEPROM code bit[3:0] : logic temporary bit[3:0] 1 : true 0 : false bit[4] : The final result after command : result check 1 : true 0 : false	RO	0x00
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

Note : The advance EEPROM operation flow, please refer to Advance_EEPROM_code application note.

6.15 MISC Register

Misc/Syetem Register : Page 0x0C			
Reg Addr.	Register Description	R/W	Default value
0x00	Switch software reset bit[0] : 1: reset the switch of IP1819I, all parameters are maintained 0: no action bit[4] : 1: reset the switch of IP1819I, all parameters are reset to default 0: no action	SC	0x00
0x01	BIST Enable and reset mask set bit[0] : Software reset mask for BIST complete bit[1] : Software reset mask for buffer over-/under-flow bit[2] : Software reset mask for output queue critical event bit[3] : Software reset mask for share management bit[4] : Software reset mask for output queue overflow bit[5] : Frame buffer ECC enable bit[6] :MIB memory block BIST enable 1 : Enable BIST 0 : Disable BIST bit[7] :LUT memory block BIST enable bit[8] :Source List memory block BIST enable bit[9] :Multicast Table block BIST enable bit[10] :VLAN memory block BIST enable bit[11] :Buffer management memory block BIST enable bit[12] : (Reserved) bit[13] :Frame buffer memory block BIST enable bit[14] :Output queue memory block BIST enable bit[15] :PTP memory block BIST enable Note : some memory blocks share the same BIST enable bit	R/W	0xFFE0
0x02	Build in self test information bit[3:0] : MIBs 4 Blocks BIST result 1 : OK 0 : Fail bit[4] : LUT BIST result bit[5] : Source List BIST result bit[6] : Multicast table BIST result bit[7] : VLAN BIST result bit[8] : Buffer management BIST result bit[9] : Frame buffer BIST result bit[10] : Output queue BIST result bit[11] : PTP BIST result bit[12] : LUT memory is under BIST 1 : BIST is going 0 : BIST finish bit[13] : VLAN /Multicast memory is under BIST bit[14] : Output queue memory is under BIST bit[15] : Frame Buffer is under BIST	RO	0x0FFF

Misc/Sytem Register : Page 0x0C			
Reg Addr.	Register Description	R/W	Default value
0x03	Switch input/output pin configuration bit[0] : port 19 is connected to CPU indication 1: connect to CPU 0: normal port bit[1] : port 19 special tag function enable when port 19 is CPU port (bit[0]=1) 1 : Enable 0: Disable bit[2] : RGMII pads internal LDO power output disable 1: Power down the LDO output 0: LDO power output normally bit[3] : CPU I/F mode setting 1: serial mode (2 pin) 0: 4-wire mode (4 pin) bit[7:4] : Reserved bit[8] : port 19 MII PHY mode enable 1 : MII clocks is provided by IP1819I 0 : MII clocks is provided by external device bit[12:9] : Reserved bit[13] : port 19 turbo MII enable 1 : Enable turbo MII (MII TX/RX clock is set to 50MHz) 0 : Disable turbo MII (MII TX/RX clock is 25/2.5MHz) bit[14] : CPU I/F speed selection 1: normal speed (2 bits "ID" + 8 bits address) 0: high speed (8 bits address + 2 bits "00") bit[15] : (Reserved should be "0")	R/W	0x4008
0x04	Special TAG Type/Len setting bit[15:0]: special tag type/length item	R/W	0x9126
0x05	Interrupt output configuration bit[0] : interrupt enable for CPU read/write SMI done bit[1] : interrupt enable for link status change bit[2] : interrupt enable for link operation mode change bit[3] : interrupt enable for CPU read/write EEPROM done bit[4] : interrupt enable for last gasp bit[5] : interrupt enable for PTP bit[6] : interrupt enable for loop detection bit[7] : interrupt enable for critical event 1: interrupt enable 0: Disable bit[13:8] : interrupt pulse period when bit[14]=1, Pulse period = (bit[13:8]+1) x 8ns bit[14] : interrupt trigger type 1: pulse trigger 0: level trigger (read and clear) bit[15] : Interrupt is action high 1: high active 0: low active	R/W	0x8B02

Misc/Sytem Register : Page 0x0C			
Reg Addr.	Register Description	R/W	Default value
0x06	<p>Interrupt status</p> <p>bit[0] : interrupt notification for CPU read/write SMI done</p> <p>bit[1] : interrupt notification for link status change</p> <p>bit[2] : interrupt notification for link operation mode change</p> <p>bit[3] : interrupt notification for CPU read/write EEPROM done</p> <p>bit[4] : interrupt notification for last gasp</p> <p>bit[5] : interrupt notification for PTP</p> <p>bit[6] : interrupt notification for loop detection</p> <p>bit[7] : interrupt notification for critical event</p> <p>1: interrupt occurred 0: normal</p>	RO RC	0x00
0x07	<p>Last gasp configuration</p> <p>bit[0] : last gasp detect enable</p> <p>1: Enable 0:Disable</p> <p>bit[1] : last gasp detect method</p> <p>1: detect high 0: detect low</p> <p>bit[2] : critical event detect enable</p> <p>1: Enable 0:Disable</p> <p>bit[3] : critical event detect method</p> <p>1: detect high 0: detect low</p> <p>bit[4] : switch fast test mode enable (for test only)</p> <p>1: Enable 0: Disable</p> <p>bit[5] : Reserved</p> <p>bit[7:6] : Output pad driving current set [1:0] (EEPROM/LED/CPU)</p> <p>00 : 1mA</p> <p>01 : 3mA (default)</p> <p>10 : 6mA</p> <p>11 : 11mA</p> <p>(Based on 2.5V)</p> <p>bit[9:8] : output pad slew rate set [1:0] (EEPROM/LED/CPU)</p> <p>00 : default</p> <p>bit[12:10] : MDC/MDIO pad driving current set</p> <p>000 : 5mA</p> <p>001 : 9mA</p> <p>010 : 14mA</p> <p>011 : 19mA (default)</p> <p>100 : 24mA</p> <p>101 : 28mA</p> <p>110 : 31mA</p> <p>111 : 33mA</p> <p>(Based on 2.5V)</p> <p>bit[15:13] : MDC/MDIO pad slew rate set</p> <p>000 : default</p>	R/W	0x0C4A
0x08	<p>I/O configuration 0</p> <p>bit[2:0] : port 17 Rx clock input delay set (0~7ns), adjust the relative phase between Rx clock and Rx data path</p> <p>default : 000</p> <p>bit[5:3] : port 17 Tx clock output delay set (0~7ns), adjust the relative phase between Tx clock and Tx data path</p> <p>default : 000</p>	R/W	0x0539

Misc/Sytem Register : Page 0x0C			
Reg Addr.	Register Description	R/W	Default value
	bit[8:6] : port 17 RGMII output driving current set 000 : 5mA 001 : 9mA 010 : 14mA (default) 011 : 19mA 100 : 24mA 101 : 28mA 110 : 31mA 111 : 33mA (Based on 2.5V) bit[11:9] : Reserved bit[12] : CPU watch dog reset disable 0 : enable reset from CPU (default) 1 : disable bit[13] : CPU clock source selection bit 0 : internal PLL (default) 1 : clock source from AFE		
0x09	I/O configuration 1 bit[2:0] : port 18 Rx clock input delay set (0~7ns), adjust the relative phase between Rx clock and Rx data path default : 000 bit[5:3] : port 18 Tx clock output delay set (0~7ns), adjust the relative phase between Tx clock and Tx data path default : 000 bit[8:6] : port 18 RGMII output driving current set default: 010 bit[11:9] : Reserved	R/W	0x0539
0x0A	I/O configuration 2 bit[2:0] : port 19 Rx clock input delay set (0~7ns), adjust the relative phase between Rx clock and Rx data path default : 000 bit[5:3] : port 19 Tx clock output delay set (0~7ns), adjust the relative phase between Tx clock and Tx data path default : 000 bit[8:6] : port 19 RGMII/MII output driving current set 000 : 1mA 001 : 2mA 010 : 3mA (default) 011 : 4mA 100 : 5mA 101 : 6mA 110 : 7mA 111 : 15mA (Based on 2.5V) bit[11:9] : Reserved	R/W	0x05DC
0x0B	port 1 ~ port 12 Fiber mode set bit[10:0] : port 1 ~ port 11 fiber mode enable bit[11] : port 12 fiber mode enable 1: fiber mode 0: TP mode	R/W	0x0000

Misc/Sytem Register : Page 0x0C			
Reg Addr.	Register Description	R/W	Default value
0x0C	port 13 ~ port 16 Fiber mode set bit[7:4] : port 13 ~ port 16 fiber mode enable 1: fiber mode 0: TP mode	R/W	0x0000
0x0D	CPU read/write EEPROM command bit[7:0] : Byte Address bit[10:8] : Device Address bit[12:11] : (Reserved) bit[13] : do not care bit[14] : read/write operation 0 : read operation 1 : write operation bit[15] : the read/write command trigger 0 : idle 1 : start command	R/W	0x0000
0x0E	CPU read/write EEPROM command bit[7:0] : High Byte Address bit[11:10] : EEPROM force mode after initial read procedure 0: as initial Auto-detect 1: reserved 2: Force 24C01 ~ 24C16 3: unused bit[14:12] : EEPROM clock period 000: 3200 ns 001: 2400 ns 01x: 1600 ns 1xx: 800 ns bit[15] : restart EEPROM initial read procedure Note: use for 24C01 ~ 24C16 EEPROM address {00h, 01h} = 0x000B : command mode EEPROM address {00h, 01h} = 0x000A : data mode	R/W	0x0000
0x0F	CPU read/write EEPROM command data bit[7:0] : in read command – the read back data in write command – data want to write bit[9:8] : Unused bit[11:10]: size mode selection bit[14:12]: EEPROM initial Read command mode area size Size_mode = 0 1xx : 1Kbit (ROM addr : 0x00000 ~ 0x0007F) 011 : 2Kbit (ROM addr : 0x00000 ~ 0x000FF) 010 : 4Kbit (ROM addr : 0x00000 ~ 0x001FF) 001 : 8Kbit (ROM addr : 0x00000 ~ 0x003FF) 000 : 16Kbit (ROM addr : 0x00000 ~ 0x007FF) Size_mode = 1 1xx : 16Kbit (ROM addr : 0x00000 ~ 0x007FF) 011 : 32Kbit (ROM addr : 0x00000 ~ 0x00FFF) 010 : 64Kbit (ROM addr : 0x00000 ~ 0x01FFF) 001 : 128Kbit (ROM addr : 0x00000 ~ 0x03FFF) 000 : 256Kbit (ROM addr : 0x00000 ~ 0x07FFF) Size_mode = 2/3 1xx : 256Kbit (ROM addr : 0x00000 ~ 0x07FFF) 011 : 512Kbit (ROM addr : 0x00000 ~ 0x0FFFF)	R/W	0x0000

Misc/Sytem Register : Page 0x0C			
Reg Addr.	Register Description	R/W	Default value
	010 : 1024Kbit (ROM addr : 0x00000 ~ 0x1FFFF) 001 : 2048Kbit (ROM addr : 0x00000 ~ 0x3FFFF) 000 : 4096Kbit (ROM addr : 0x00000 ~ 0x7FFFF) bit[15] : unused (EEPROM read stop criteria : (a) STOP sign or (b) Read out configured Area size)		
0x10	Reserved		
0x11	IEEE802.3az TX clock silence enable bit[0] : port 17 RGMII GTXC clock silence enable 1 : enable clock off during LPI 0:disable bit[1] : port 17 MII TXC clock silence enable 1 : enable clock off during LPI 0:disable bit[2] : port 18 RGMII GTXC clock silence enable 1 : enable clock off during LPI 0:disable bit[3] : port 18 MII TXC clock silence enable 1 : enable clock off during LPI 0:disable bit[7:4] : Reserved bit[8] : port 19 GMII/RGMII GTXC clock silence enable 1 : enable clock off during LPI 0:disable bit[9] : port 19 MII TXC clock silence enable 1 : enable clock off during LPI 0:disable	R/W	0x000
0x12 ~ 0x21	Reserved		
0xFF	Register Page selection [5:0] : page selection	R/W	0x00

7 Electrical Characteristics

7.1 Absolute Maximum Rating

Permanent device damage may occur if Absolute Maximum Ratings are applied. Functional operation should be restricted to the conditions as specified in the following section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	I/O	V_{DDIO}	- 0.5	+3.63V	V
	Core	V_{DDCore}	- 0.5	+1.26V	V
Input Voltage		V_I	- 0.5	V_{DDIO}	V
Output Voltage		V_O	- 0.5	V_{DDIO}	V
Storage Temperature		T_{STG}	-65	+150	°C
Operation Temperature		T_{OPT}	-40	+85	°C
IC Junction Temperature		T_J		+125	°C

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

8 AC Characteristics

8.1 Power On Sequence and Reset Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{DIFF}	Time difference among power sources	0	-	-	ms
T_{PWR_LEAD}	All power source ready before reset released	10	-	-	ms
T_{CLK_LEAD}	X1 clock valid before reset released	10	-	-	ms
T_{SYS_INIT}	System initial completed, this time to keep silence.	10	-	-	ms

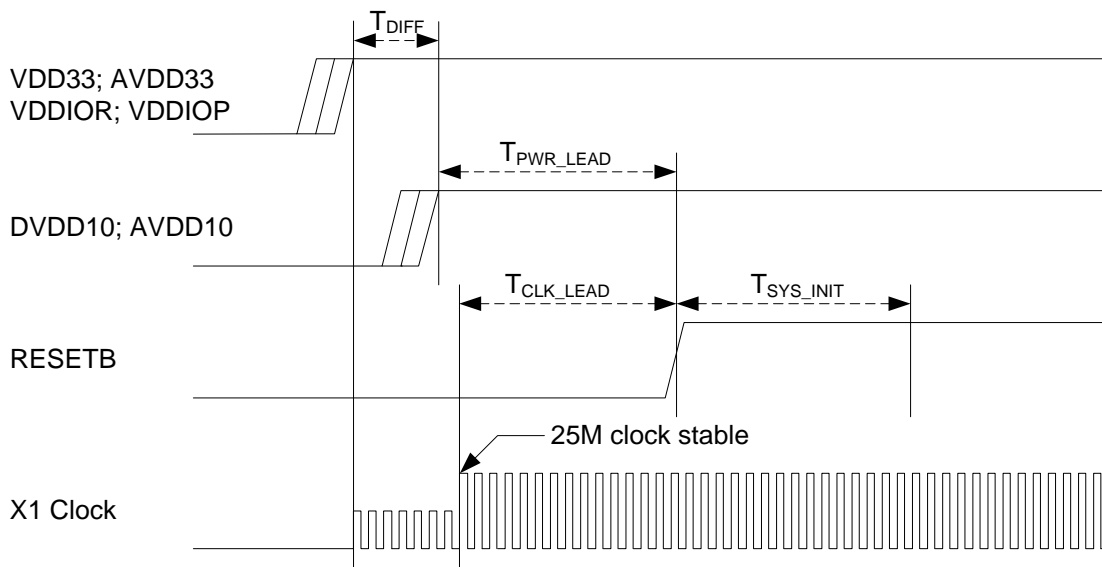


Figure 29 Power On Sequence and Reset timing Diagram

8.2 PHY Management (MDIO) Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{CH}	MDC High Time	-	200	-	ns
T_{CL}	MDC Low Time	-	200	-	ns
T_{CM}	MDCK cycle time	-	400	-	ns
T_{MD_SU}	MDIO set up time	10	-	-	ns
T_{MD_H}	MDIO hold time	0	-	-	ns
T_{MD_D}	MDIO output delay time	200	-	210	ns

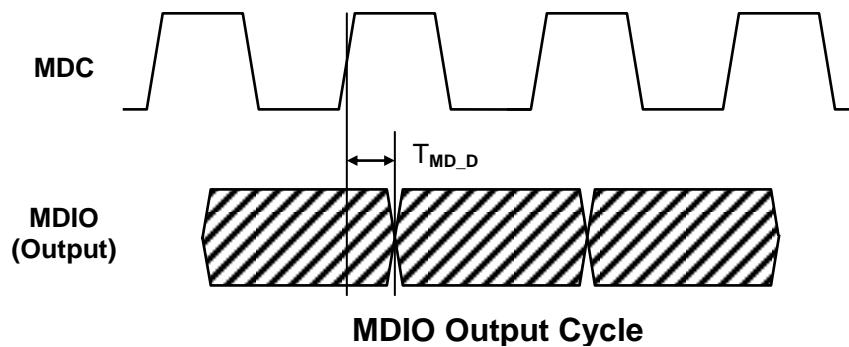
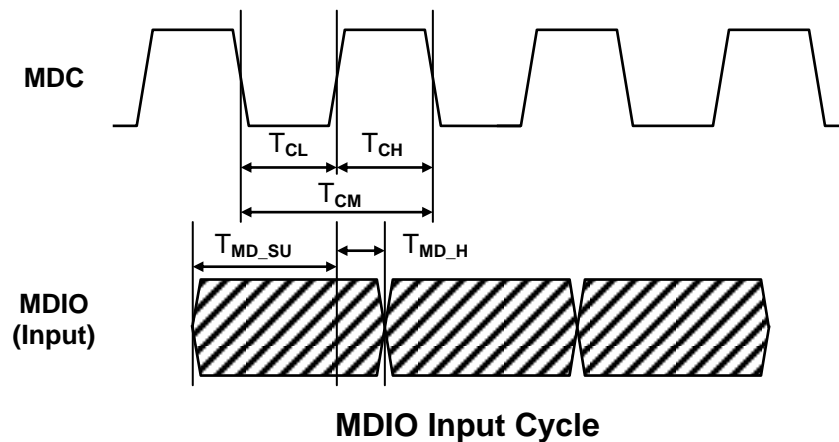


Figure 30 MDC/MDIO Read/Write cycle timing Diagram

8.3 CPU Serial Bus Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{s_c}	Serial CPU Clock cycle time	26	-	-	ns
T_{sio_su}	Serial I/O set up time	10	-	-	ns
T_{sio_H}	Serial I/O hold time	10	-	-	ns
T_{sio_D}	Serial I/O output delay time	-	-	20	ns

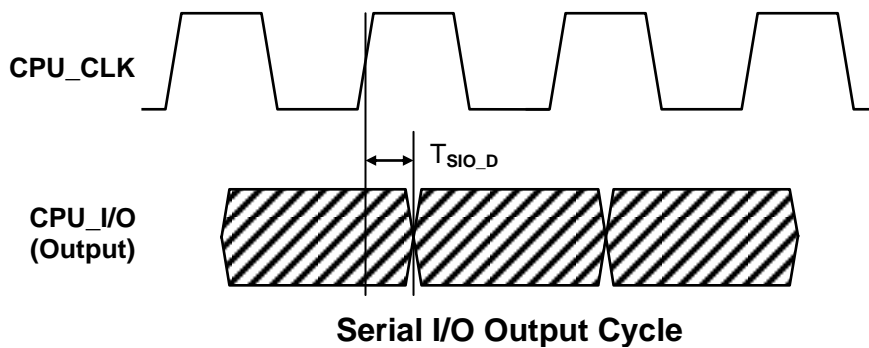
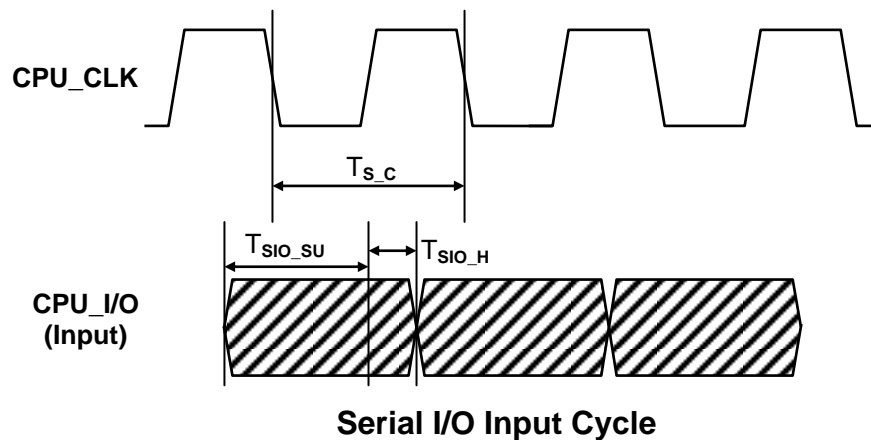


Figure 31 CPUIO Serial Bus timing Diagram

8.4 RGMII Timing

8.4.1 Rx Part Timing

Symbol	Description	Min.	Typ.	Max.	Unit
$T_{RGRxCLK}$	Period of receive clock in giga mode	-	8	-	ns
	Period of transmit clock in 100M mode	-	40	-	ns
	Period of transmit clock in 10M mode	-	400	-	ns
T_{RGS}	RXDV, RXD to RXCLK setup time	1	-	-	ns
T_{RGH}	RXCTL, RXD to RXCLK hold time	1	-	-	ns

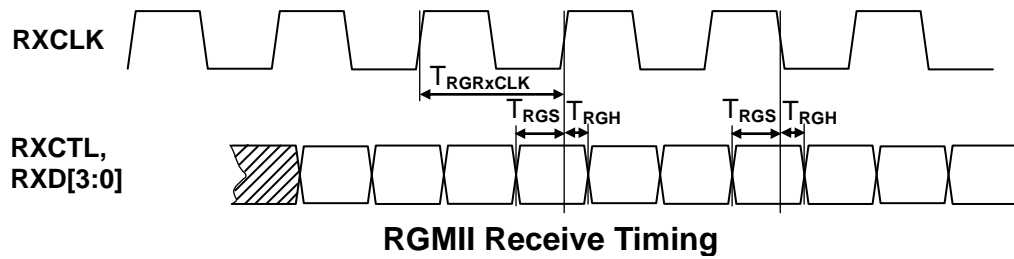


Figure 32 RGMII Receive Timing

8.4.2 Tx Part Timing

Symbol	Description	Min.	Typ.	Max.	Unit
$T_{RGTxCLK}$	Period of transmit clock in giga mode	-	8	-	ns
	Period of transmit clock in 100M mode	-	40	-	ns
	Period of transmit clock in 10M mode	-	400	-	ns
T_{RGTxD}	TXCTL, TXD output delay from GTXCLK edge (Note1)	1.1	-	2.7	ns

Note1: T_{RGTxD} allows implementation of delay on GTXCLK inside the transmitter. Refer to register 0x8, 0x9 and 0xA of page 0xC.

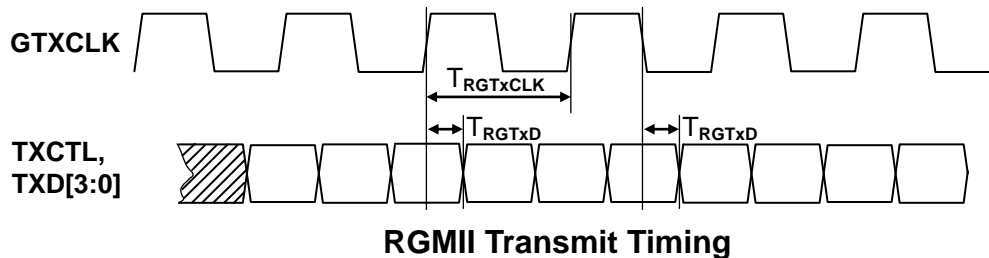
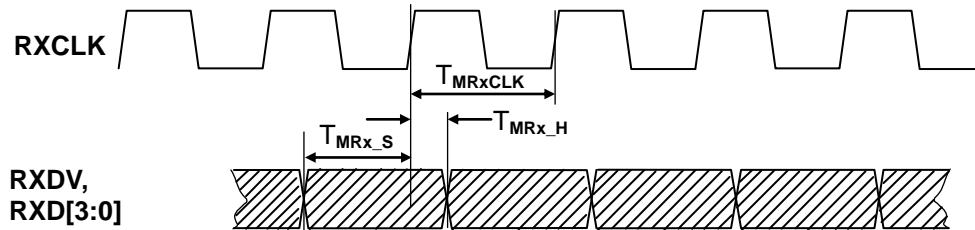


Figure 33 RGMII Transmit Timing

8.5 MII Timing

8.5.1 Receive Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{MRxCLK}	Receive clock period 100Mbps MII	-	40	-	ns
	Receive clock period 10Mbps MII	-	400	-	ns
T_{MRx_S}	RXDV, RXD to RXCLK setup time	2	-	-	ns
T_{MRx_H}	RXDV, RXD to RXCLK hold time	0.5	-	-	ns

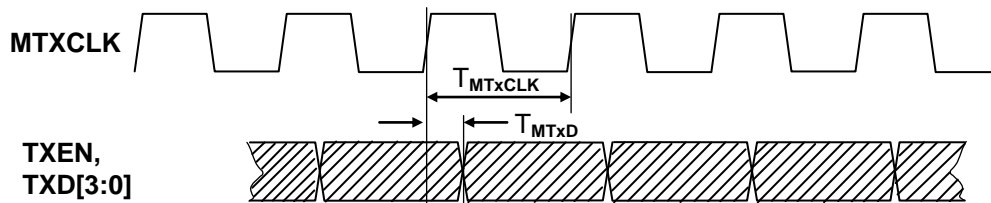


MII Receive Timing

Figure 34 MII Receive Timing

8.5.2 Transmit Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{MTxCLK}	Transmit clock period 100Mbps MII	-	40	-	ns
	Transmit clock period 10Mbps MII	-	400	-	ns
T_{MTxD}	MTXCLK rising edge to TXEN, TXD	5	-	25	ns



MII Transmit Timing

Figure 35 MII Transmit Timing

8.6 EEPROM Timing

8.6.1 Data read cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	12800	-	ns
T_{sSCL}	EE_DAT to EE_CLK setup time	20	-	-	ns
T_{hSCL}	EE_DAT to EE_CLK hold time	20	-	-	ns

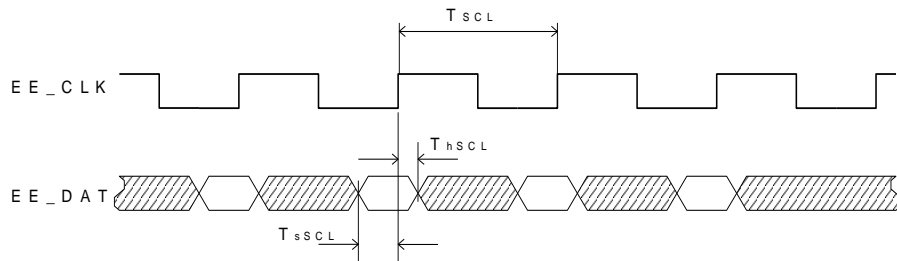


Figure 36 Data read cycle

8.6.2 Command cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	12800	-	ns
T_{dSCL}	EE_CLK falling edge to EE_DAT	-	-	3200	ns

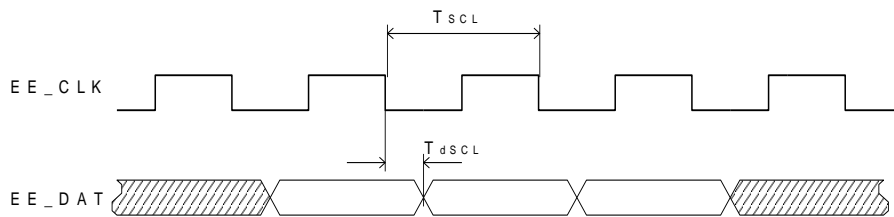


Figure 37 Command cycle

9 DC Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output low voltage	V_{OL}	---	---	$0.1 \times V_{DD33}$	V
Output high voltage	V_{OH}	$0.9 \times V_{DD33}$	---	---	V
VDD33 supply current I_{VDD33}	100M+2G	---	1	---	mA
	10M+2G	---	1	---	
	IDLE	---	1	---	
AVDD33 supply current I_{AVDD33}	100M+2G	---	335	---	mA
	10M+2G	---	412	---	
	IDLE	---	62	---	
DVDD10 supply current I_{DVDD10}	100M+2G	---	587	---	mA
	10M+2G	---	532	---	
	IDLE	---	443	---	
AVDD10 supply current I_{AVDD10}	100M+2G	---	56	---	mA
	10M+2G	---	24	---	
	IDLE	---	24	---	
VDDIOR supply current I_{VDDIOR}	VDDIOR=2.0V	---	3	---	mA
	VDDIOR=2.5V	---	10	---	
	VDDIOR=3.3V	---	47	---	
VDDIOP supply current I_{VDDIOP}	VDDIOP =2.5V	---	1	---	mA
	VDDIOP =3.3V	---	5	---	
VDD33 supply voltage	V_{VDD33}	2.97	3.3	3.63	V
AVDD33 supply voltage	V_{AVDD33}	2.97	3.3	3.63	V
DVDD10 supply voltage	V_{DVDD10}	1.05	1.08	1.15	V
AVDD10 supply voltage	V_{AVDD10}	1.05	1.08	1.15	V
VDDIOR supply voltage	VDDIOR=2.0V	1.9	2.0	2.1	V
	VDDIOR=2.5V	2.38	2.5	2.63	
	VDDIOR=3.3V	2.97	3.3	3.63	
VDDIOP supply voltage	VDDIOP=2.5V	2.38	2.5	2.63	V
	VDDIOP=3.3V	2.97	3.3	3.63	
RESET Threshold voltage		$0.4 \times V_{DDIOP}$	---	$0.6 \times V_{DDIOP}$	V
X1 Clock Input Low Voltage (3.3V operation)	V_{ILX1}	---	---	0.6	V
X1 Clock Input High Voltage (3.3V operation)	V_{IHX1}	1.5	---	---	V
Pull-up/down resistor	R_{PUD}	51	---	127	K Ω

RGMII						
Input Low to High	VDDIOR =2.0V	V _{IH}	1.2	---	---	V
Input High to Low		V _{IL}	---	---	0.8	
Input Low to High	VDDIOR =2.5V	V _{IH}	1.5	---	---	
Input High to Low		V _{IL}	---	---	1	
Input Low to High	VDDIOR =3.3V	V _{IH}	1.98	---	---	
Input High to Low		V _{IL}	---	---	1.32	
RGMII/MII						
Input Low to High	VDDIOP =2.5V	V _{IH}	1.5	---	---	V
Input High to Low		V _{IL}	---	---	1	
Input Low to High	VDDIOP =3.3V	V _{IH}	1.98	---	---	
Input High to Low		V _{IL}	---	---	1.32	

10 Serial Transmitter/Receiver DC characteristic

Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V _{OD}	Output Voltage Swing(single-ended)	200	300	400	mV _{p-p}
R _O	Output Impedance(single-ended)	42.5	50	57.5	Ωs

Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V _{RCOM}	Common mode voltage(Supplied by IC itself)	1.4	1.6	1.8	V
V _{IDTH}	Input Differential Threshold	200			mV _{p-p}
R _{IN}	Receiver 100Ω Differential Input Impedance	85	100	115	Ω

11 Power Consumption

Symbol	Parameter	Power Consumption (@25°C)	Units
P _{10MF}	16-Port 10M Full + 2G active	2.007	W
P _{100MF}	16-Port 100M Full + 2G active	1.796	W
P _{LPI}	IEEE802.3az low power idle mode	0.773	W
P _{LDPS}	Link down power saving mode	0.74	W

12 Crystal & X1 Clock Input Specifications

12.1 Crystal Specifications

Table 35 Crystal Specifications

Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Oscillation Mode	Fundamental Mode
3	Frequency Tolerance at 25°C	+/- 50 ppm
4	Temperature Characteristics	+/- 50 ppm
5	Operating Temperature Range	-40°C ~ +85°C
6	Equivalent Series Resistance	40 ohm Max.
7	Drive Level	100 μ W
8	Load Capacitance	20 pF
9	Shunt Capacitance	7 pF Max
10	Insulation Resistance	Mega ohm Min./DC 100V
11	Aging Rate A Year	+/- 5 ppm/year

12.2 X1 Clock Input Specifications

Table 36 X1 Clock Input Specifications

Item	Parameter	Range
1	Frequency	25.000 MHz
2	Duty cycle	40~60%
3	Rise time	Max: 4 ns
4	Fall time	Max: 4 ns
5	Max voltage	3.63V
6	Jitter	300 ps

13 Thermal Data

The junction temperature of chip (T_j) is a well-known key factor of IC characteristics and life time. There are three thermal resistance coefficients, J_A , ψ_{JT} , and J_c , which are defined in JEDEC 51-2 and 51-6, will be provided to estimate T_j . If the T_j is over maximum limit, it is necessary to disperse heat by extra dissipation device, such as heat sink and electrical fan.

Thermal resistance represents the capability of an IC package to carry out the heat inside an IC chip. It is a complex function of package structure, material property, input power, environment variables such as air flow speed and PCB layers. The major thermal dissipation paths can be illustrated as following.

Table 37 Operation Range

Parameter	Min	Typical	Max	unit
T_j	-40	-	+125	$^{\circ}\text{C}$
T_a	-40	+25	+85	$^{\circ}\text{C}$

Table 38 Thermal Resistance

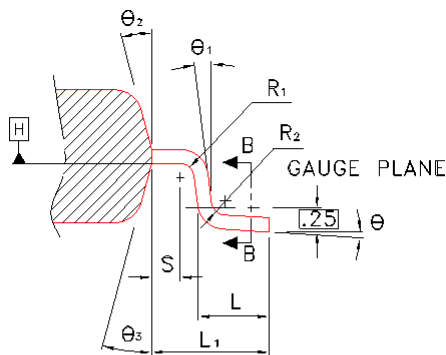
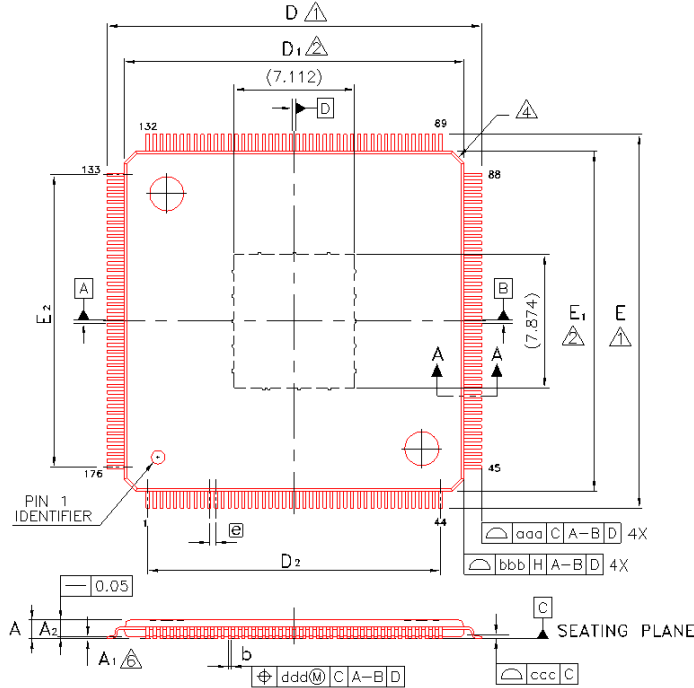
Parameter	Condition	Value	Unit
Θ_{JA}	0 ft/s Air flow 2 layers PCB	40.5	$^{\circ}\text{C}/\text{W}$
	0 ft/s Air flow 4 layers PCB	19.3	
	IC Plus 2 layers 224x120mm ² PCB	29.8	
Θ_{JC}	0 ft/s Air flow 2 layers PCB	8.0	$^{\circ}\text{C}/\text{W}$
	0 ft/s Air flow 4 layers PCB	7.5	
	IC Plus 2 layers 224x120mm ² PCB	8.0	
ψ_{JT}	0 ft/s Air flow 2 layers PCB	3.5	$^{\circ}\text{C}/\text{W}$
	0 ft/s Air flow 4 layers PCB	2.2	
	IC Plus 2 layers 224x120mm ² PCB	3.5	

14 Order Information

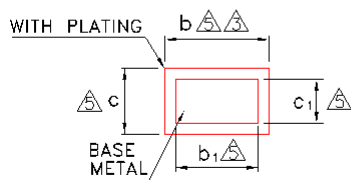
Part No.	Package	Notice
IP1819I	176 pin TQFP	-

15 Package Outline

176 pin TQFP Outline Dimensions



SECTION A-A



SECTION B-B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	1.00	1.10	1.20	0.039	0.043	0.047
A ₁	0.05	0.10	0.15	0.002	0.004	0.006
A ₂	0.95	1.00	1.05	0.037	0.039	0.041
b	0.13	0.18	0.23	0.005	0.007	0.009
b ₁	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c ₁	0.09	—	0.16	0.004	—	0.006
D	22.00 BSC			0.866 BSC		
D ₁	20.00 BSC			0.787 BSC		
D ₂	17.20 BSC			0.677 BSC		
E	22.00 BSC			0.866 BSC		
E ₁	20.00 BSC			0.787 BSC		
E ₂	17.20 BSC			0.677 BSC		
ⓐ	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L ₁	1.00 REF			0.039 REF		
R ₁	0.08	—	—	0.003	—	—
R ₂	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ ₁	0°	—	—	0°	—	—
θ ₂	11°	12°	13°	11°	12°	13°
θ ₃	11°	12°	13°	11°	12°	13°
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTE :

- △ TO BE DETERMINED AT SEATING PLANE [C].
- △ DIMENSIONS D₁ AND E₁ DO NOT INCLUDE MOLD PROTRUSION. D₁ AND E₁ ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- △ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
- △ EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
- △ A₁ IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 7. CONTROLLING DIMENSION : MILLIMETER.
- 8. REFERENCE DOCUMENT : JEDEC MS-026
- 9. SPECIAL CHARACTERISTICS C CLASS: ccc