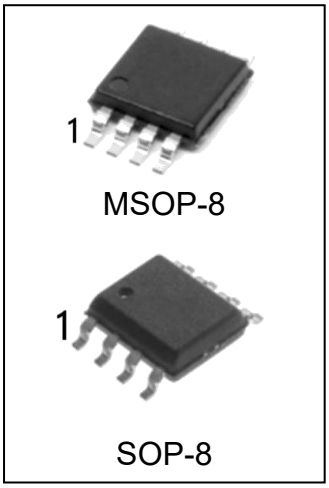
3.3V 64M-BIT SERIAL FLASH MEMORY WITH DUAL, QUAD SPI

1. FEATURES



New Family of SpiFlash Memories

– HG25Q64 : 64M-bit / 8M-byte
– Standard SPI: CLK, /CS, DI, DO,/WP,/Hold
– Dual SPI: CLK, /CS, IO0, IO1 ,/WP,/Hold
– Quad SPI: CLK, /CS, IO0, IO1, IO2, IO3
– Software & Hardware Reset

Highest Performance Serial Flash

– 104MHz Single, Dual/Quad SPI clocks
– 260/320MHz equivalent Dual/Quad SPI
– More than 10,000 erase/progran cycles
– More than 20-year data retention

Efficient “Continuous Read”

– Continuous Read with 8/16/32/64-Byte Wrap
– As few as 8 clocks to address memory

Low Power, Wide Temperature Range

– Single 2.7 to 3.6V supply
– 4mA active current,<3μA Power-down (typ.)
– -40°C to +85°C operating range

Flexible Architecture with 4KB sectors

– Uniform Sector/Block Erase (4K/32K/64K-Byte)
– Program 1 to 256 byte per programmable page
– Erase/Program Suspend & Resume

Advanced Security Features

– Software and Hardware Write-Protect
– Power Supply Lock-Down and OTP protection
– Top/Bottom, Complement array protection
– 64-Bit Unique ID for each device
– Discoverable Parameters (SFDP) Register
– 3X256-Bytes Security Registers
– Volatile & Non-volatile Status Register Bits

Space Efficient Packaging

– 8-pin SOP-150mil
– 8-pin SOP-208mil
– 8-pin MSOP

2. ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
HG25Q64MM/TR	MSOP-8	25Q64	REEL	3000pcs/Reel
HG25Q64M/TR	SOP-8-150mil	25Q64	REEL	2500pcs/Reel
HG25Q64MW/TR	SOP-8-208Mil	25Q64	REEL	2500pcs/Reel

3. GENERAL DESCRIPTIONS

The HG25Q64 (64M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25S series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on 3.0V to 3.6V power supply with current consumption as low as 3μA for power-down. All devices are offered in space-saving packages.

The HG25Q64 array is organized into 32,768 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The HG25Q64 has 2,048 erasable sectors and 128 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2.)

The HG25Q64 supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 and I/O3. SPI clock frequencies of HG25Q64 of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Dual I/O and 532MHz (80MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

Additionally, the device supports JEDEC standard manufacturer and device ID, and a 64-bit Unique Serial Number and three 256-bytes Security Registers.

4. PACKAGE TYPES AND PIN CONFIGURATIONS

4.1. Pin Configuration SOP 208mil/150mil

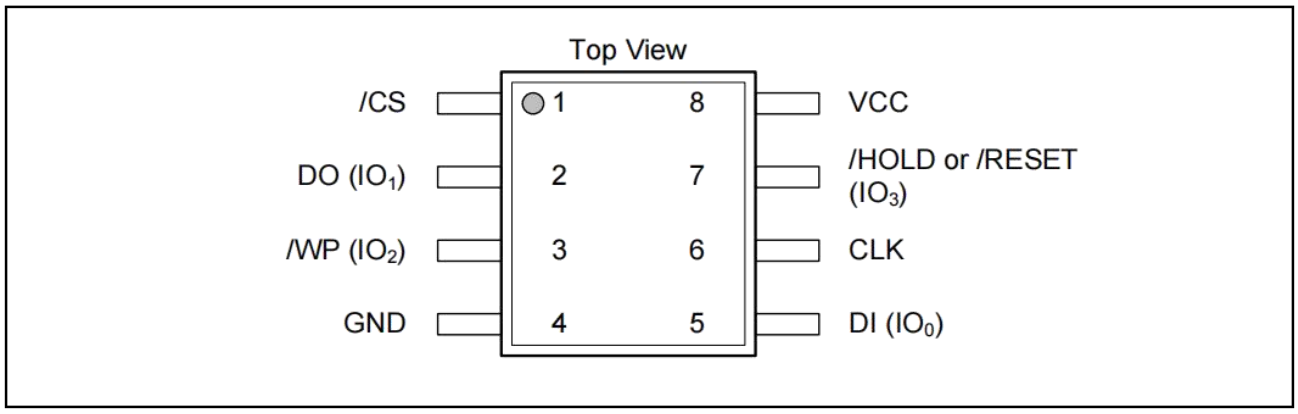


Figure 1a. HG25Q64 Pin Assignments, 8-pin SOP 208-mil/150mil

4.2. Pin Description SOP 208mil/150mil

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET(IO3)	I/O	Hold or Reset Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions

2. IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) function is only available for Standard/Dual SPI.

5. PIN DESCRIPTIONS

5.1. Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 38b). If needed a pull-up resister on the /CS pin can be used to accomplish this.

5.2. Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The HG25Q64 supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and the /HOLD pin becomes IO3.

5.3. Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low.

5.4. HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3.

See Figure 1a-c for the pin configuration of Quad I/O operation.

5.5. Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

6. BLOCK DIAGRAM

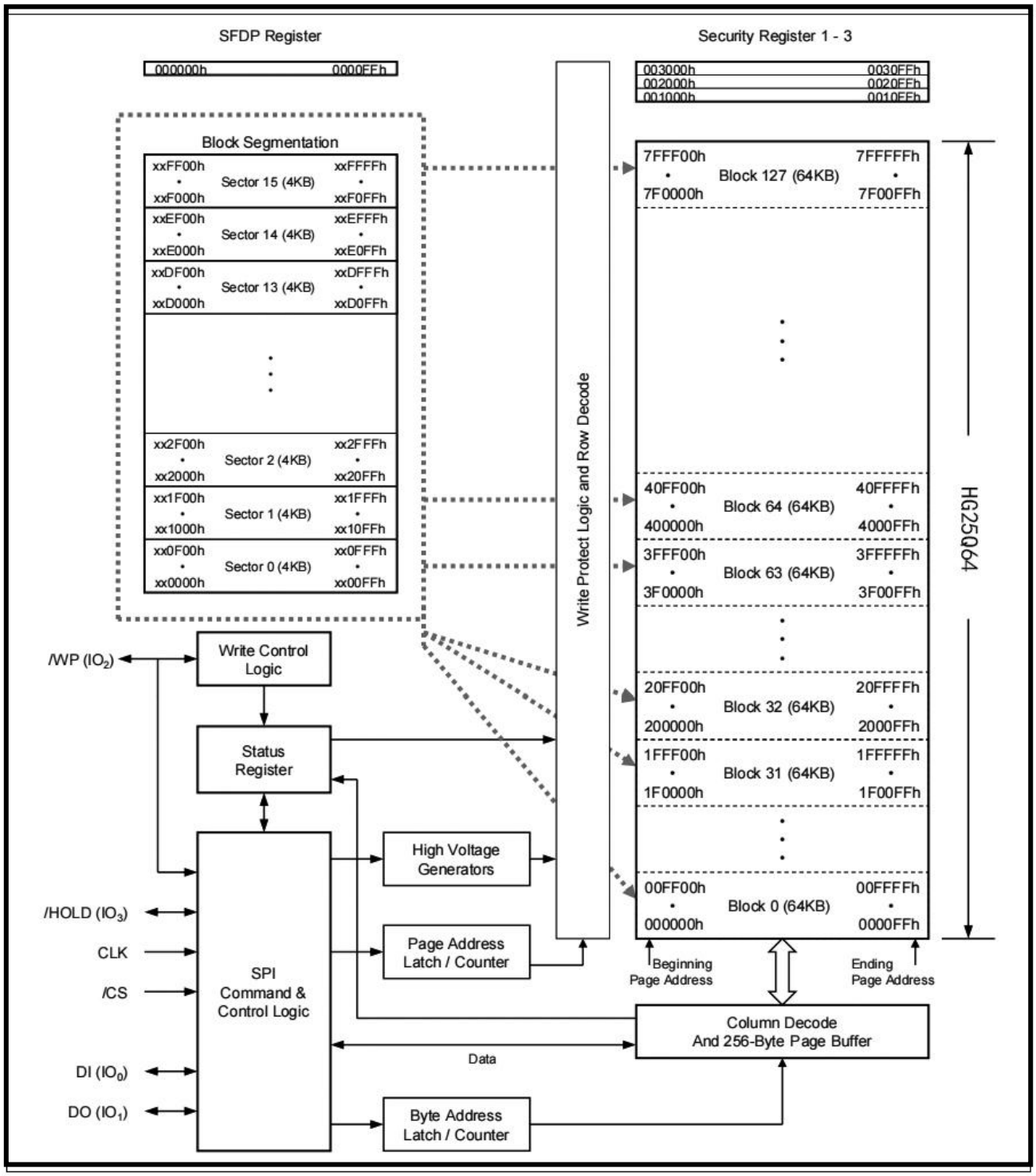


Figure 2. HG25Q64 Serial Flash Memory Block Diagram

7. FUNCTIONAL DESCRIPTIONS

7.1. Standard SPI Instructions

The HG25Q64 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

7.2. Dual SPI Instructions

The HG25Q64 supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

7.3. Software Reset

The HG25Q64 can be reset to the initial power-on state by a software Reset sequence. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately 30μS (t_{RST}) to reset.

6.4. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the HG25Q64 provides several means to protect the data from inadvertent writes.

6.5. Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (/WP pin) write protection using Status Registers
- Additional Individual Block/Sector Locks for array protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up

Upon power-up or at power-down, the HG25Q64 will maintain a reset condition while VCC is below the threshold value of VWI, (See Power-up Timing and Voltage Levels and Figure 34a). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of tPUW. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC min level and tVSL time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0. Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin,changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

8. STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for HG25Q64. The Read Status Register -1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, and output driver strength. Write access to the Status Register is controlled by the state of the non volatile Status Register Protect bits (SRL), the Write Enable instruction, and during Standard/Dual SPI operations

8.1. Status Registers

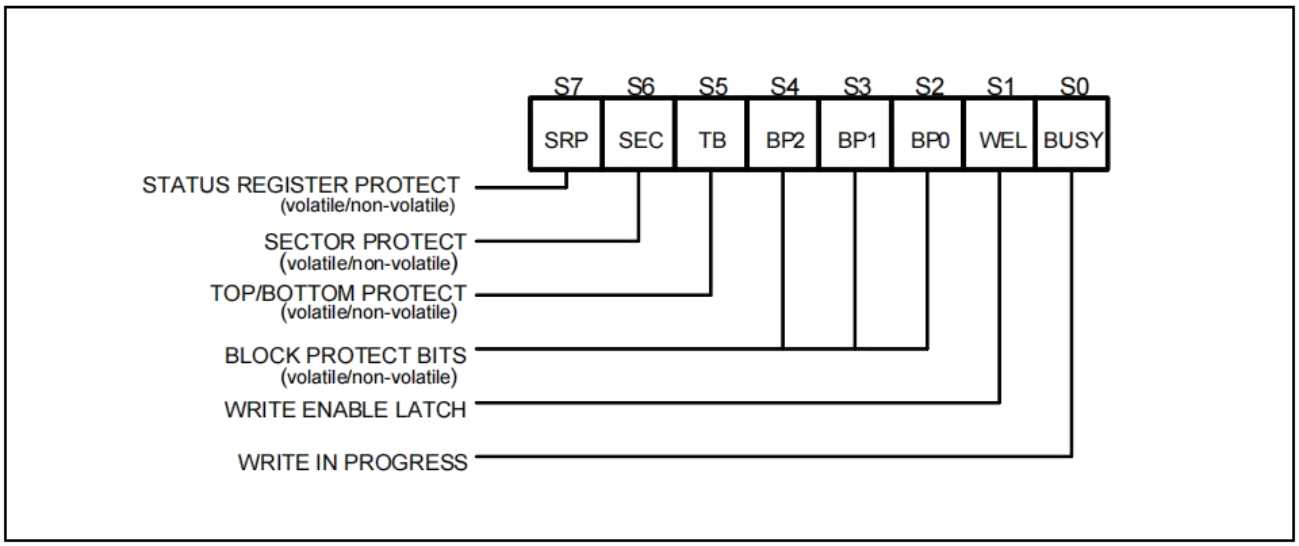


Figure3a. Status Register-1

8.1.1. Erase/Write In Progress (BUSY) – Status Only

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.1.2. Write Enable Latch (WEL) – Status Only

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

8.1.3. Block Protect Bits (BP2, BP1, BP0) – Volatile/Non-Volatile Writable

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

8.1.4. Top/Bottom Block Protect (TB) – Volatile/Non-Volatile Writable

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP/SRL and WEL bits.

8.1.5. Sector/Block Protect Bit (SEC) – Volatile/Non-Volatile Writable

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

8.1.6. Complement Protect (CMP) – Volatile/Non-Volatile Writable

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

8.1.7. Status Register Protect (SRP1, SRL0) – Volatile/Non-Volatile Writable

Three Status and Configuration Registers are provided for HG25Q64 . The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device iswrite enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, and output driver strength, The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, output driver. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

SRL	SRP	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written toafter a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot bewritten to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can bewritten to after a Write Enable instruction, WEL=1.
1	X	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again untilthe next power-down, power-up cycle.(1)
1	X	X	One Time Program	Status Register is permanently protected and cannot be writtento.

Notes:

1. When SRP1,SRP0=(1,0)，a power-down, power-up cycle will change SRP0 to (0,0) state.

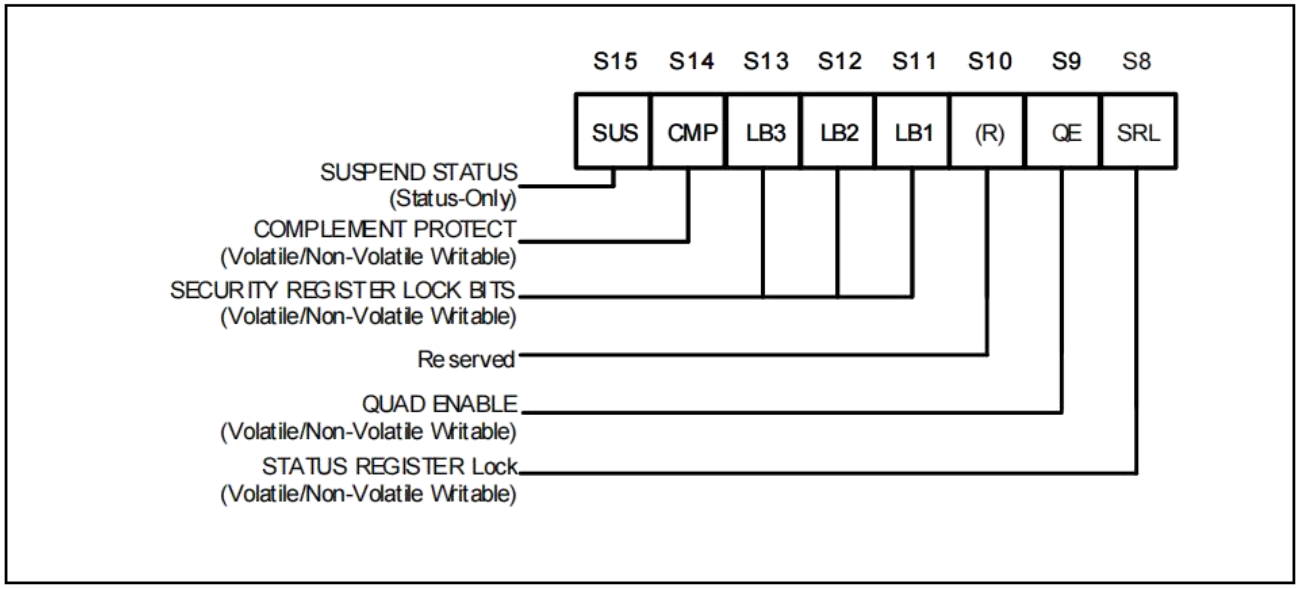


Figure 3b. Status Register-2

8.1.8. Erase/Program Suspend Status (SUS) – Status Only

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

8.1.9. Security Register Lock Bits (LB3, LB2, LB1) – Volatile/Non-Volatile OTP Writable

The Security Register Lock Bits (LB3, LB2, LB1,LB0) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11,S10) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently. LED value should be considered don`t care for erad.This bit is set to 1.Security register 0 contains the Serial Flash Discoverable Parameters and is always programmed and locked by CFX.

8.1.10. Quad Enable (QE) – Volatile/Non-Volatile Writable

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that enables Quad SPI operation. When the QE bit is set to a 0 state (factory default for part numbers with ordering options "IM" &"JM"), the /HOLD are enabled, the device operates in Standard/Dual SPI modes. When the QE bit is set to a 1 (factory fixed default for part numbers with ordering options "IQ" & "JQ"), the Quad IO2 and IO3 pins are enabled, and /HOLD function is disabled, the device operates in Standard/Dual/Quad SPI modes.

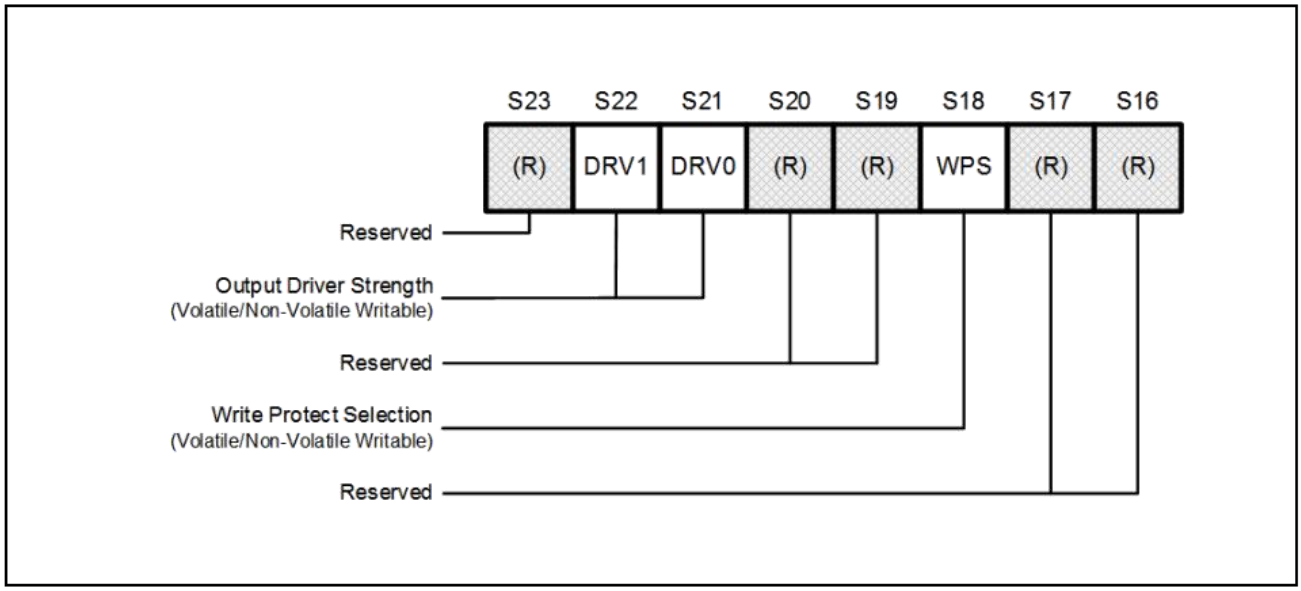


Figure 3c. Status Register-3

8.1.11. Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
0, 0	100%
0, 1	75%
1, 0	50%
1, 1	25% (default)

8.1.12. Reserved Bits – Non Functional

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

8.1.13.HG25Q64 Status Register Memory Protection(CMP=0)

STATUS REGISTER(1)					HG25Q64 (64M-BIT) MEMORY PROTECTION(3)			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTEDADDRESSES	PROTECTED DENSITY	PROTECTED PORTION(2)
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 and 127	7E0000h – 7FFFFFh	128KB	Upper 1/64
0	0	0	1	0	124 thru 127	7C0000h – 7FFFFFh	256KB	Upper 1/32
0	0	0	1	1	120 thru 127	780000h – 7FFFFFh	512KB	Upper 1/16
0	0	1	0	0	112 thru 127	700000h – 7FFFFFh	1MB	Upper 1/8
0	0	1	0	1	96 thru 127	600000h – 7FFFFFh	2MB	Upper 1/4
0	0	1	1	0	64 thru 127	400000h – 7FFFFFh	4MB	Upper 1/2
0	1	0	0	1	0 and 1	000000h – 01FFFFh	128KB	Lower 1/64
0	1	0	1	0	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/32
0	1	0	1	1	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/16
0	1	1	0	0	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/8
0	1	1	0	1	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/4
0	1	1	1	0	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/2
X	X	1	1	1	0 thru 127	000000h – 7FFFFFh	8MB	ALL
1	0	0	0	1	127	7FF000h – 7FFFFFh	4KB	U – 1/2048
1	0	0	1	0	127	7FE000h – 7FFFFFh	8KB	U – 1/1024
1	0	0	1	1	127	7FC000h – 7FFFFFh	16KB	U – 1/512
1	0	1	0	X	127	7F8000h – 7FFFFFh	32KB	U – 1/256
1	1	0	0	1	0	000000h – 000FFFh	4KB	L – 1/2048
1	1	0	1	0	0	000000h – 001FFFh	8KB	L – 1/1024
1	1	0	1	1	0	000000h – 003FFFh	16KB	L – 1/512
1	1	1	0	X	0	000000h – 007FFFh	32KB	L – 1/256

Notes:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

8.1.14. HG25Q64 Status Register Memory Protection (WPS = 0, CMP = 1)

STATUS REGISTER(1)					HG25Q64 (64M -BIT) MEMORY PROTECTION(3)			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION(2)
X	X	0	0	0	0 thru 127	000000h – 7FFFFFh	8MB	ALL
0	0	0	0	1	0 thru 125	000000h – 7DFFFFh	8,064KB	Lower 63/64
0	0	0	1	0	0 thru 123	000000h – 7BFFFFh	7,936KB	Lower 31/32
0	0	0	1	1	0 thru 119	000000h – 77FFFFh	7,680KB	Lower 15/16
0	0	1	0	0	0 thru 111	000000h – 6FFFFFh	7MB	Lower 7/8
0	0	1	0	1	0 thru 95	000000h – 5FFFFFh	5MB	Lower 3/4
0	0	1	1	0	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/2
0	1	0	0	1	2 thru 127	020000h – 7FFFFFh	8,064KB	Upper 63/64
0	1	0	1	0	4 thru 127	040000h – 7FFFFFh	7,936KB	Upper 31/32
0	1	0	1	1	8 thru 127	080000h – 7FFFFFh	7,680KB	Upper 15/16
0	1	1	0	0	16 thru 127	100000h – 7FFFFFh	7MB	Upper 7/8
0	1	1	0	1	32 thru 127	200000h – 7FFFFFh	5MB	Upper 3/4
0	1	1	1	0	64 thru 127	400000h – 7FFFFFh	4MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 127	000000h – 7FEFFFh	8,188KB	L – 2047/2048
1	0	0	1	0	0 thru 127	000000h – 7FDFFFh	8,184KB	L – 1023/1024
1	0	0	1	1	0 thru 127	000000h – 7FBFFFh	8,176KB	L – 511/512
1	0	1	0	X	0 thru 127	000000h – 7F7FFFh	8,160KB	L – 255/256
1	1	0	0	1	0 thru 127	001000h – 7FFFFFh	8,188KB	U – 2047/2048
1	1	0	1	0	0 thru 127	002000h – 7FFFFFh	8,184KB	U – 1023/1024
1	1	0	1	1	0 thru 127	004000h – 7FFFFFh	8,176KB	U – 511/512
1	1	1	0	X	0 thru 127	008000h – 7FFFFFh	8,160KB	U – 255/256

Notes:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

9. INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the HG25Q64 consists of 48 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table1-2). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figures 5 through 57. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

9.1. Device ID and Instruction Set Tables

9.1.1. Iden tification

	(MF7 - MF0)	
FSRK Serial Flash	83h	
Device ID	**(ID7 - ID0)**	**(ID15 - ID0)**
Instruction	**90h**	**9Fh**
HG25Q64	16h	4017h

9.1.2. Instruction Set Table 1(Standard SPI Instructions)(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-2)	8	8	8	8	8	8	8
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Release Power-down	ABh						
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	5Ah	00h	00h	A7-A0	Dummy	D7-D0...	
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)		
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Sector Erase(4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase(32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase(64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register-1(4)	01h	(S7-S0)(4)					
Read Staus Register-2	35h	(S15-S8)(2)					
Write Staus Register-2	31h	(S15-S8)					
Read Staus Register-3	15h	(S23-S16)(2)					
Write Staus Register-3	11h	(S23-S16)					
Read SFDP Register	5Ah	00	00	A7-A0	Dummy	(D7-D0)	
Erase Security Register(5)	44h	A23-A16	A15-A8	A7-A0			
Program Security Register(5)	42h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Read Security Register(5)	48h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase/Program Suspend	75h						
Erase/Program Resume	7Ah						
Power-down	B9h						
Enable reset	66h						
Reset Device	99h						

9.1.3. Instruction Set Table 2 (Dual/Quad SPI Instructions)(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Number of Clock(1-1-2)	**8**	**8**	**8**	**8**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(7)		
Number of Clock(1-2-2)	**8**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Fast Read Dual I/O	**BBh**	A23-A16(6)	A15-A8(6)	A7-A0(6)	Dummy(11)	(D7-D0)(7)			
Number of Clock(1-1-4)	**8**	**8**	**8**	**8**	**2**	**2**	**2**	**2**	**2**
Quad Input Page Program	**32h**	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	(D7-D0)(3)	…		
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)(10)
Number of Clock(1-4-4)	**8**	**2**(8)	**2**(8)	**2**(8)	**2**	**2**	**2**	**2**	**2**
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	Dummy(11)	Dummy	Dummy	(D7-D0)	
Word Read Quad I/O	**E7h**	A23-A16	A15-A8	A7-A0	Dummy(11)	Dummy	(D7-D0)		
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W8-W0				

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 IO pins.

2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.

3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

4. Write Status Register-1 (01h) can also be used to program Status Register-1&2, see section 9.2.5.

5. Security Register Address:

Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address

Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address

Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address

6. Dual SPI address input format:

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

7. Dual SPI data output format:

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

8. Quad SPI address input format:

IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

Set Burst with Wrap input format:

IO1 = x, x, x, x, x, W5, x

IO0 = x, x, x, x, x, W4, x

IO2 = x, x, x, x, x, W6, x

IO3 = x, x, x, x, x, x, x

9. Quad SPI data input/output format:

IO0 = (D4, D0, …..)

IO1 = (D5, D1, …..)

IO2 = (D6, D2, …..)

IO3 = (D7, D3, …..)

10. Fast Read Quad I/O data output format:

IO0 = (x, x, x, x, D4, D0, D4, D0)

IO1 = (x, x, x, x, D5, D1, D5, D1)

IO2 = (x, x, x, x, D6, D2, D6, D2)

IO3 = (x, x, x, x, D7, D3, D7, D3)

11. The first dummy is M7-M0 should be set to Fxh

9.2 Instruction Descriptions

9.2.1. Write Enable (06h)

The Write Enable instruction (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1.

The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

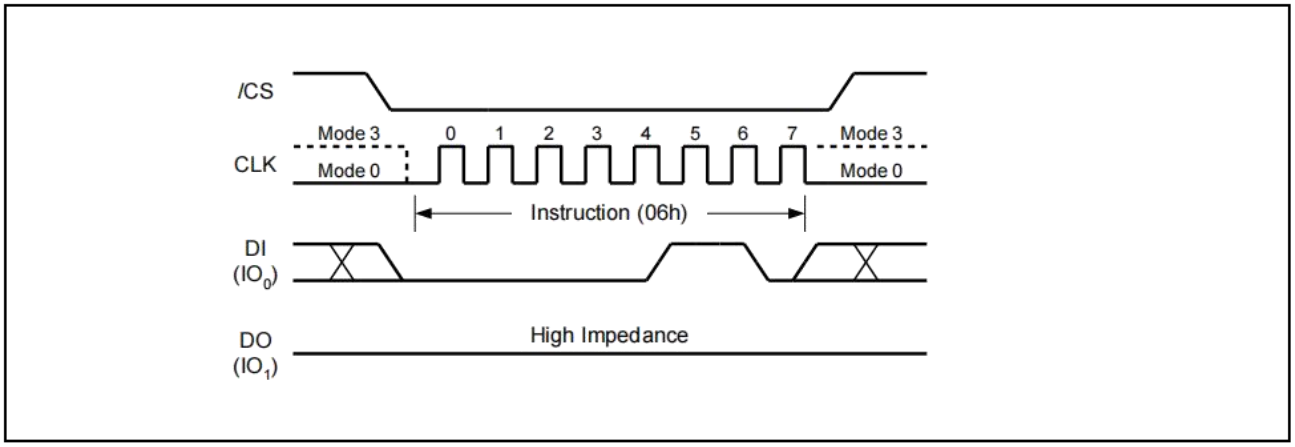


Figure 4. Write Enable Instruction for SPI Mode

9.2.2. Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 8.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 5) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

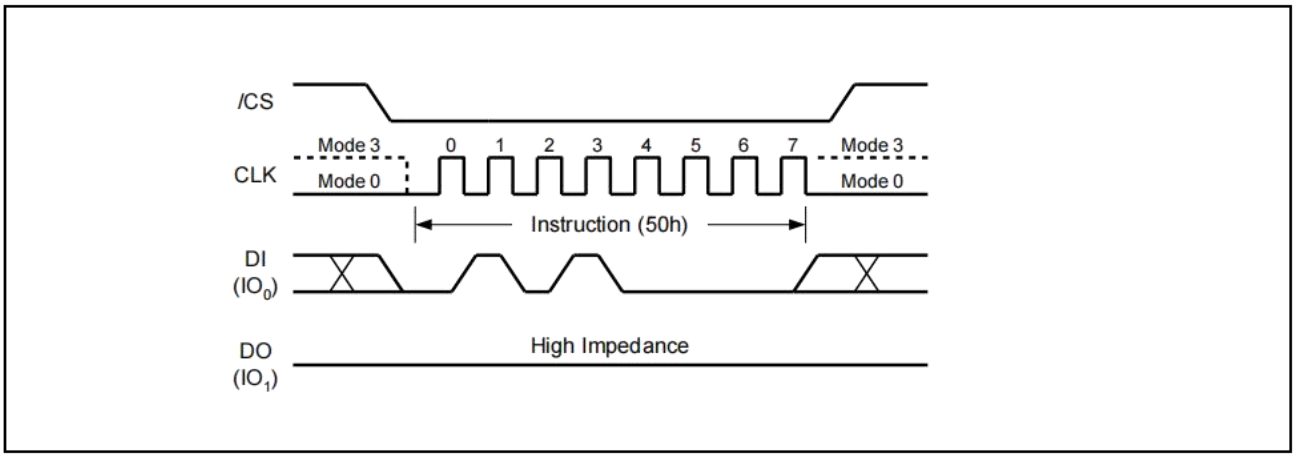


Figure 5. Write Enable for Volatile Status Register Instruction for SPI Mode

9.2.3. Write Disable (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

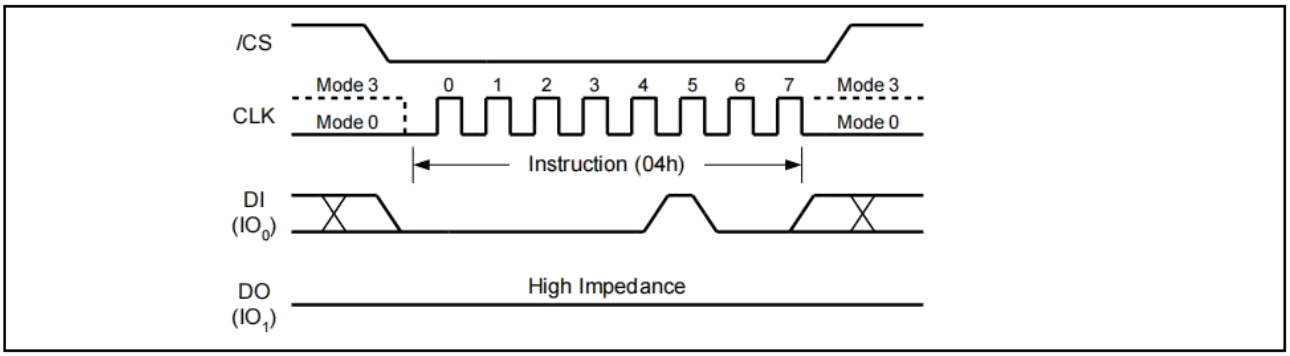


Figure 6. Write Disable Instruction for SPI Mode

9.2.4. Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7. Refer to section 8.1 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 8. The instruction is completed by driving /CS high.

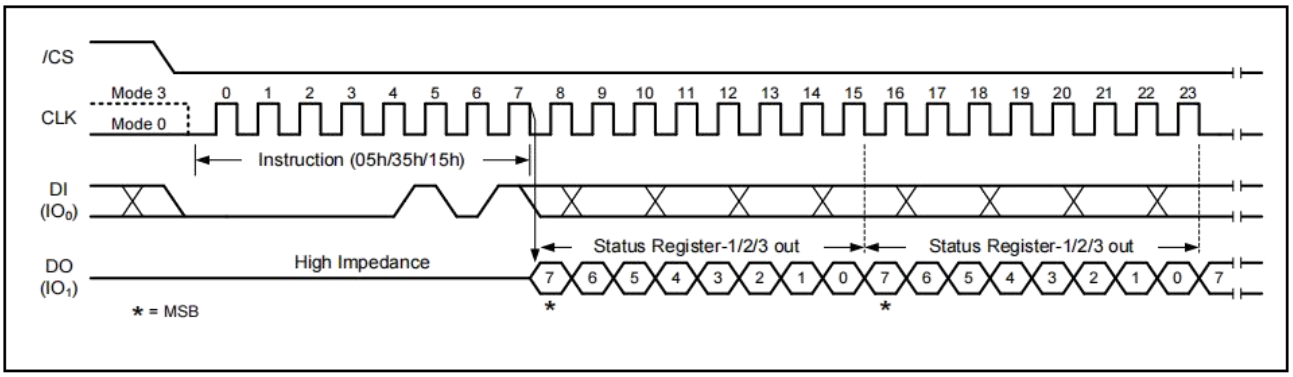


Figure 7. Read Status Register Instruction

9.2.5. Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include:SEC, TB, BP[2:0] in Status Register-1; CMP, LB[3:1], QE, SRL in Status Register-2; DRV1, DRV0, WPS in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 8.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRL and LB[3:1] cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of tSHSL2 (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

Refer to section 8.1 for Status Register descriptions.

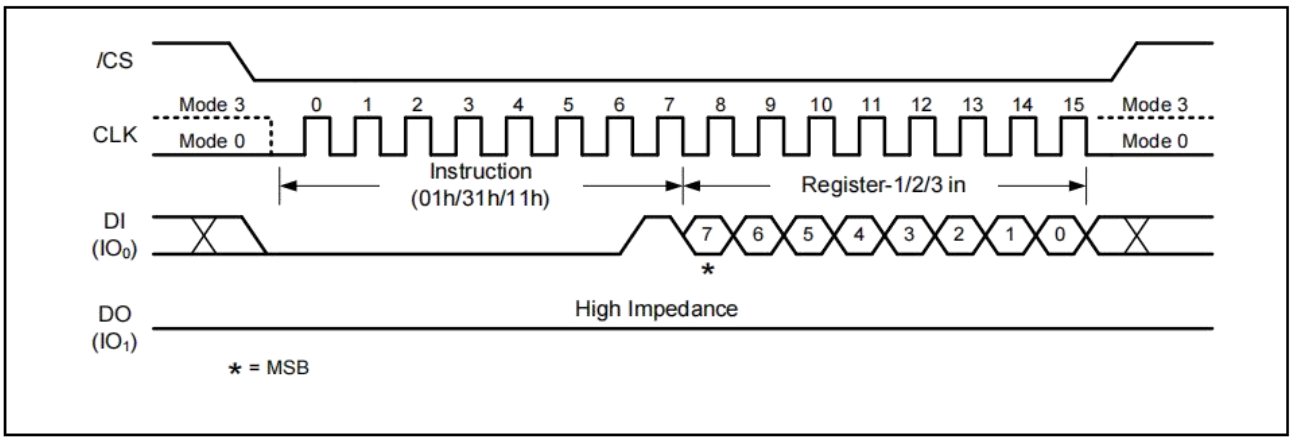


Figure 8. Write Status Register-1/2/3 Instruction

Notes:

After any one of the three Status Registers has been written, software reset instruction (66h and 99h) or power down is needed to reload the non-volatile bits of three Status Register.

9.2.6. Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 9. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

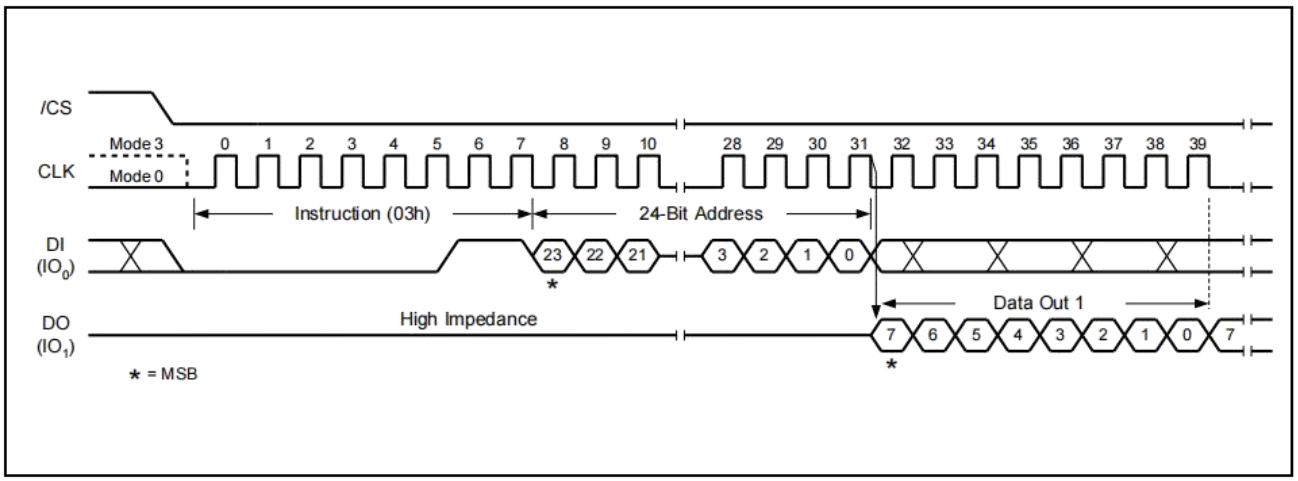


Figure 9. Read Data Instruction

9.2.7. Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 10. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DO pin is a “don’t care”.

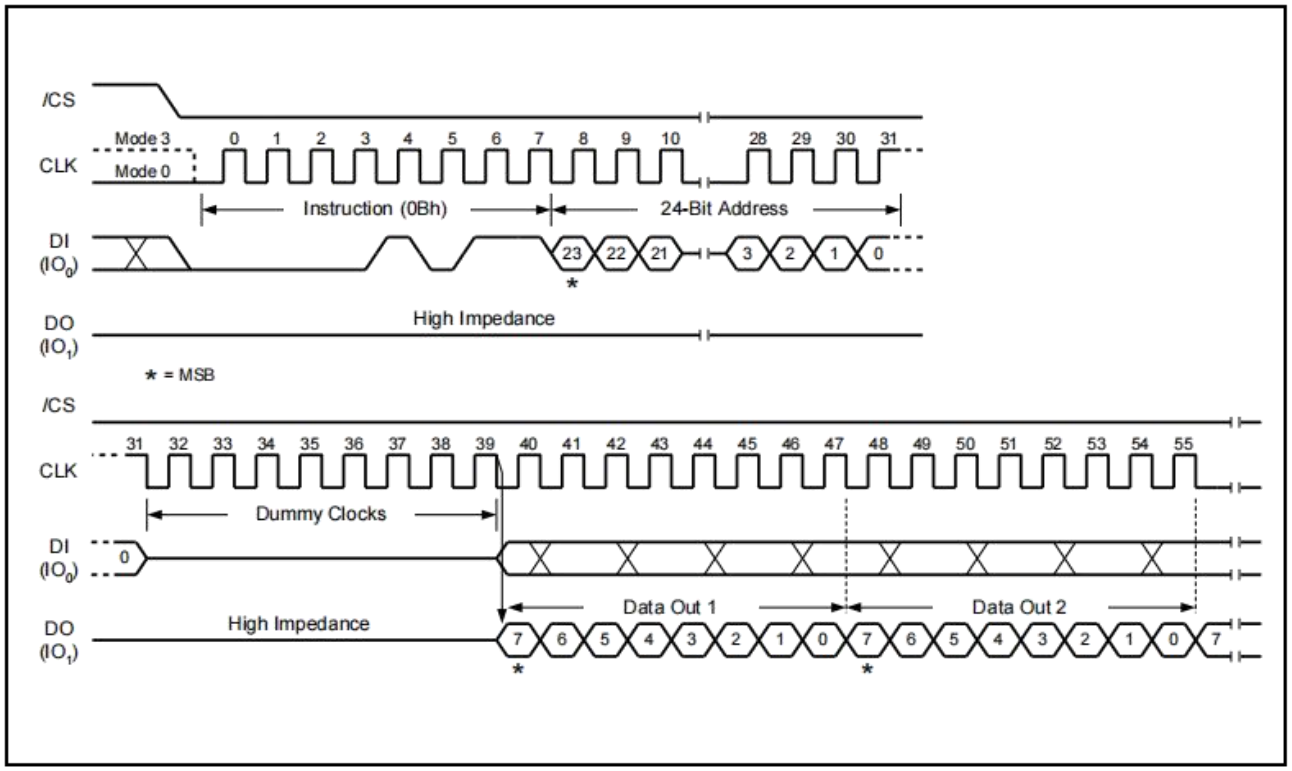


Figure 10. Fast Read Instruction

9.2.8. Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO0 and IO1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 11. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO0 pin should be high-impedance prior to the falling edge of the first data out clock.

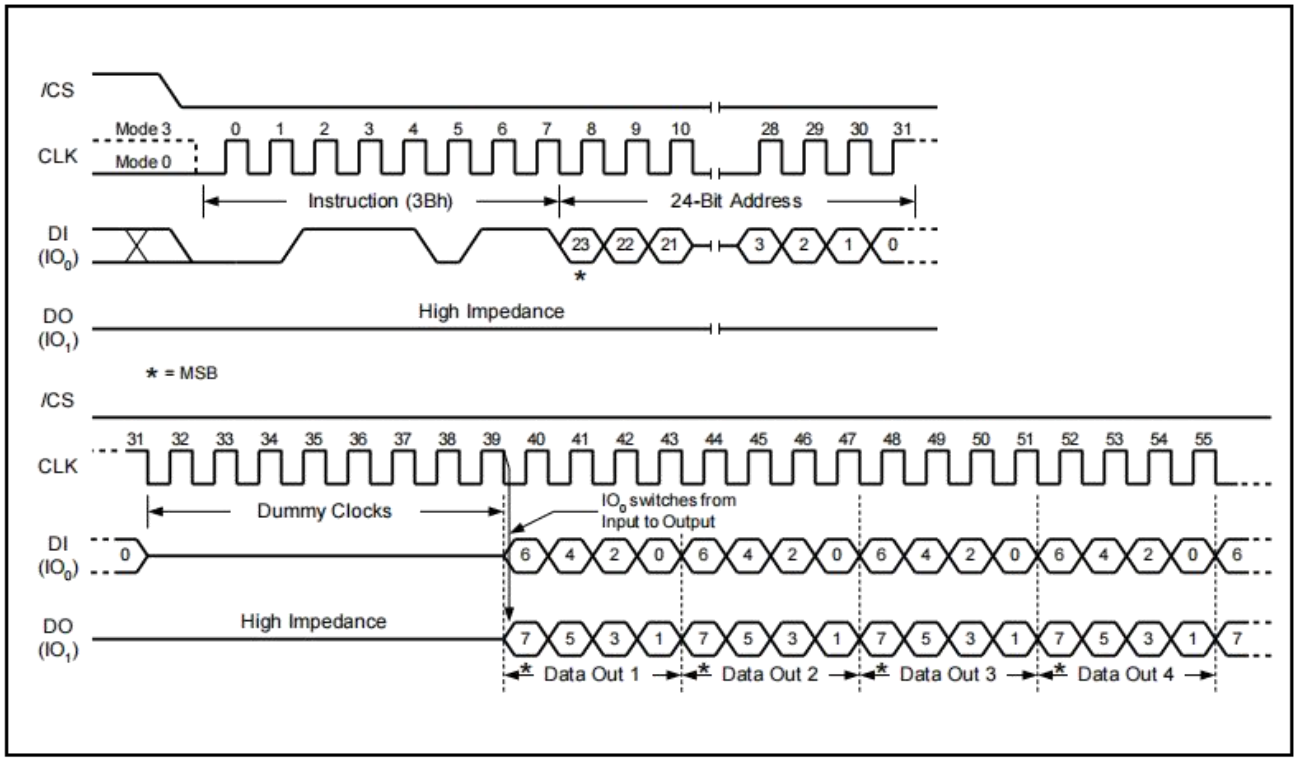


Figure 11. Fast Read Dual Output Instruction

9.2.9. Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO0, IO1, IO2, and IO3. The Quad Enable (QE) bit in Status Register- 2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 12. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high impedance prior to the falling edge of the first data out clock.

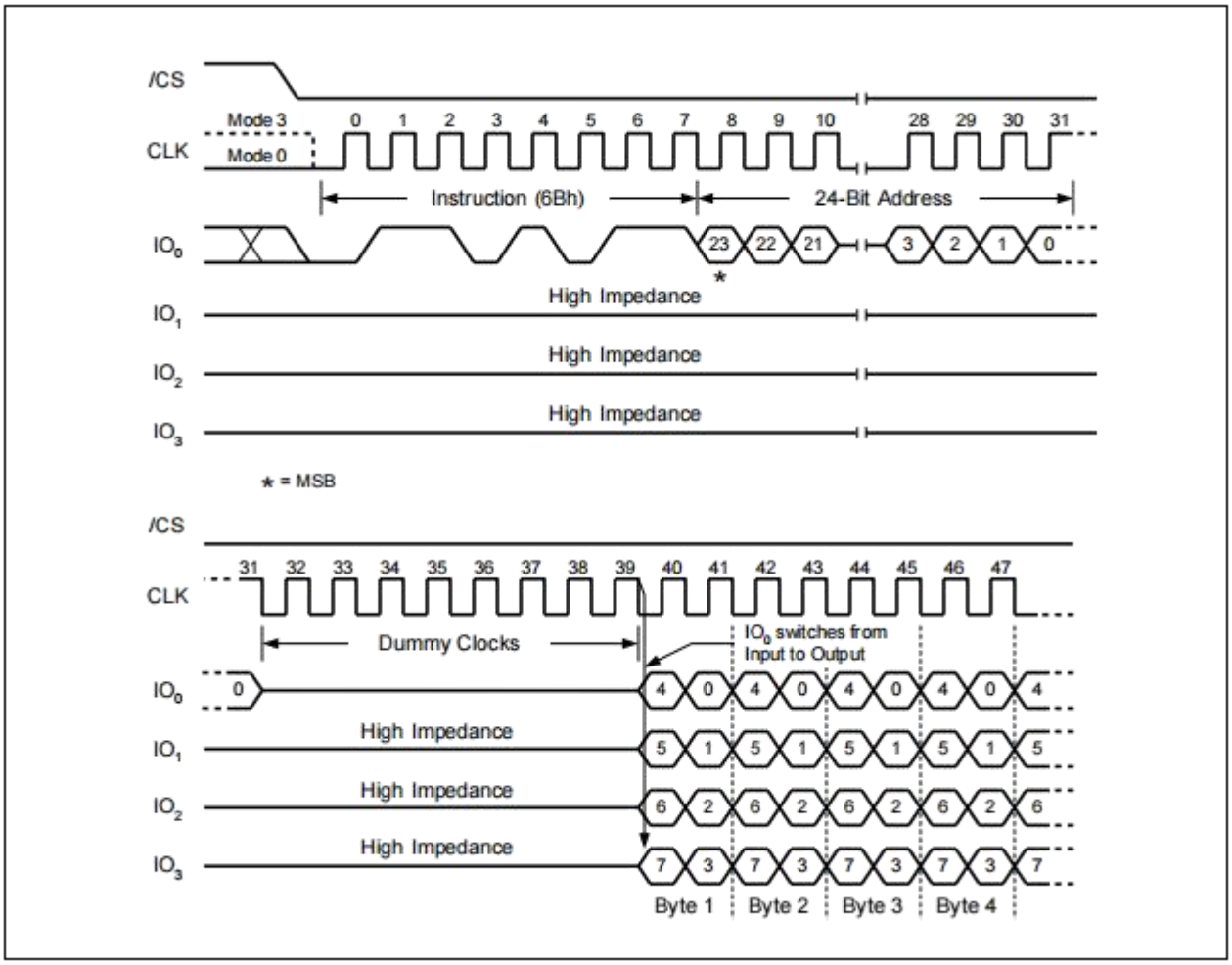


Figure 12. Fast Read Quad Output Instruction (SPI Mode only)

9.2.10. Fast Read Dual I/O (BBh) (1)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 13a. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 13b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

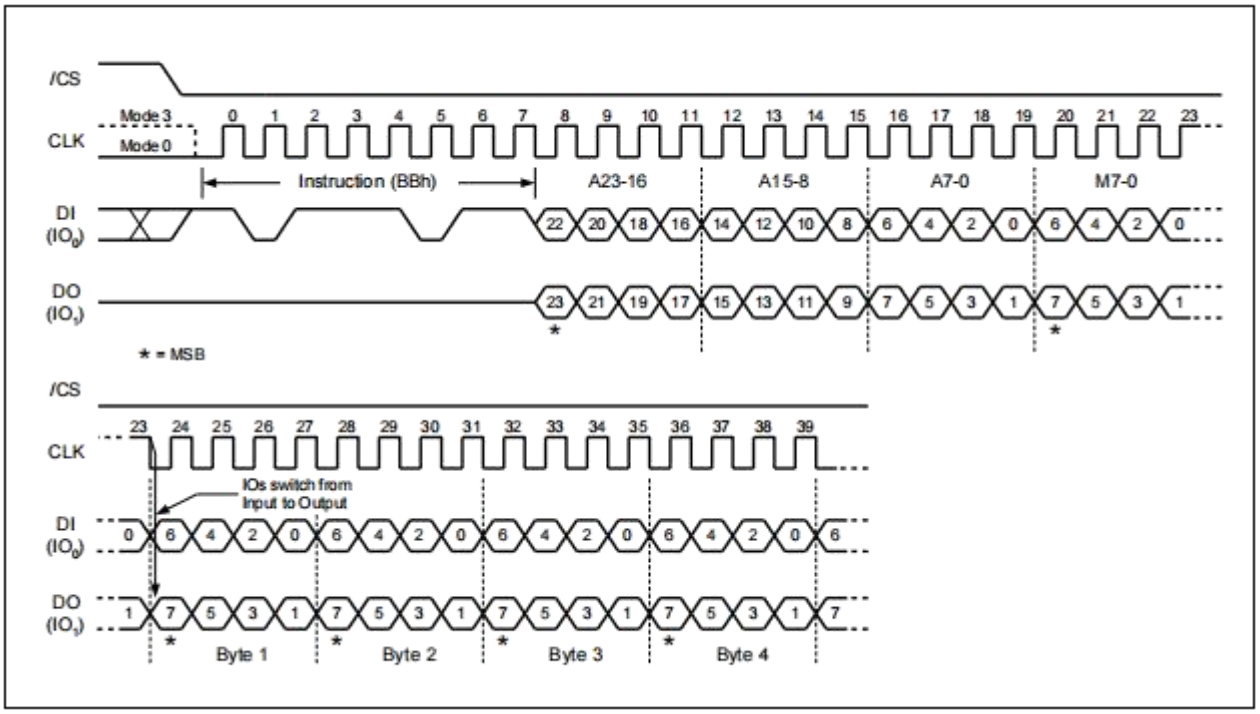


Figure 13a. Fast Read Dual I/O Instruction (Initial instruction or previoous M5-4 ≠10, SPI Mode only)

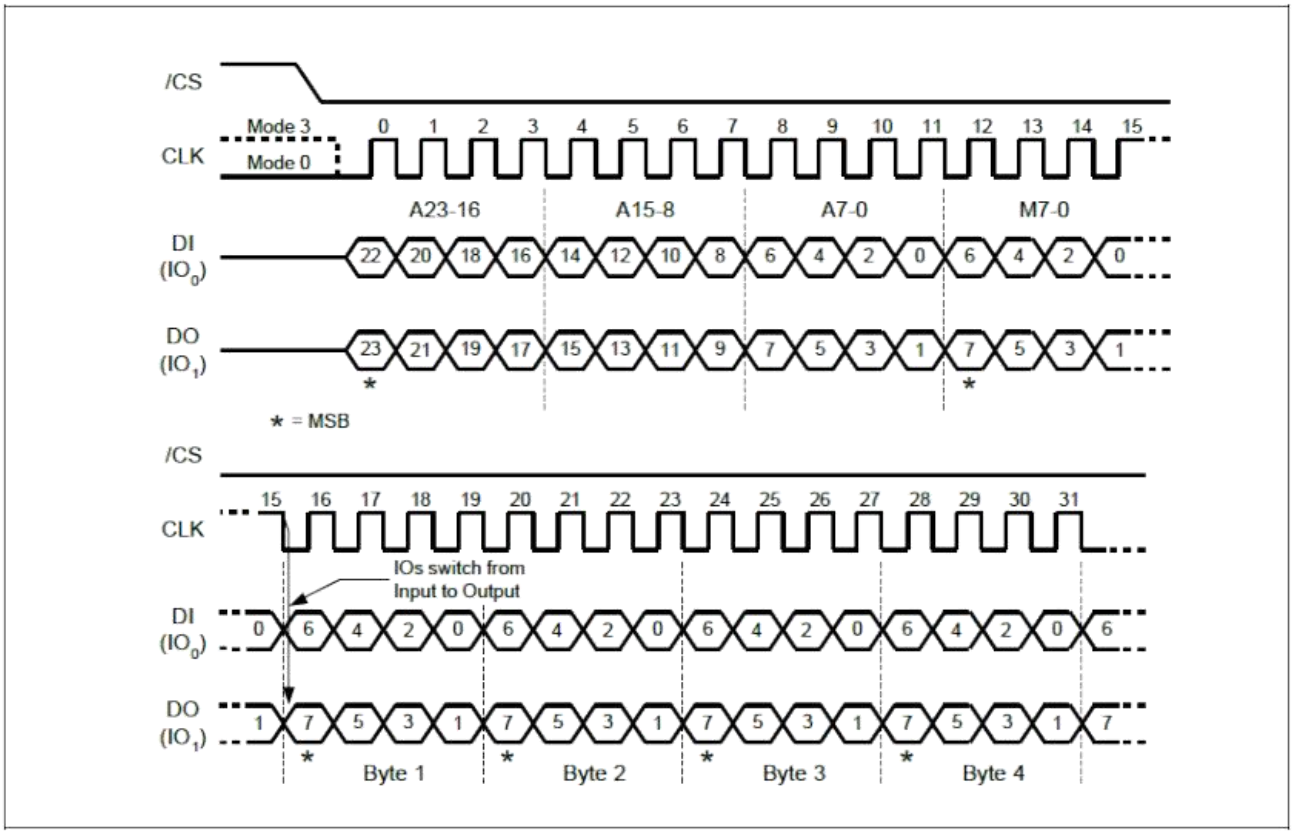


Figure 13b. Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

Notes:

1. During Fast Read Dual I/O instruction (BB), the A1 and A0 of input address (A23-A0) cannot be set to '1' simultaneously

9.2.11. Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with "Continuous Read Mode

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 14a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 14b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

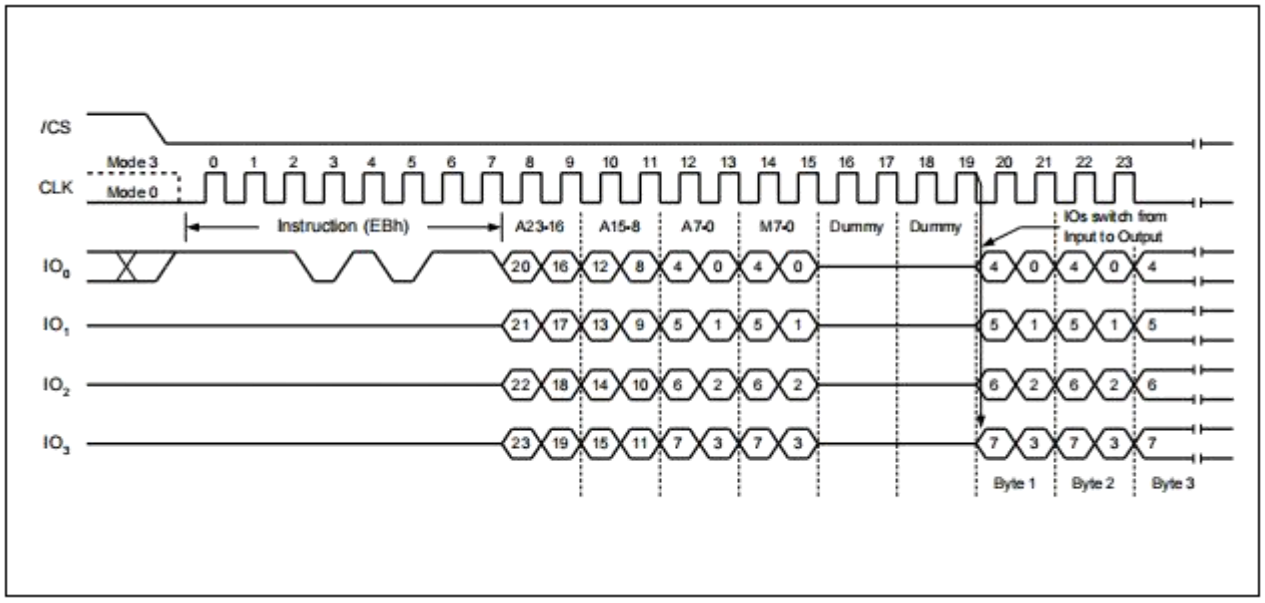


Figure 14a. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

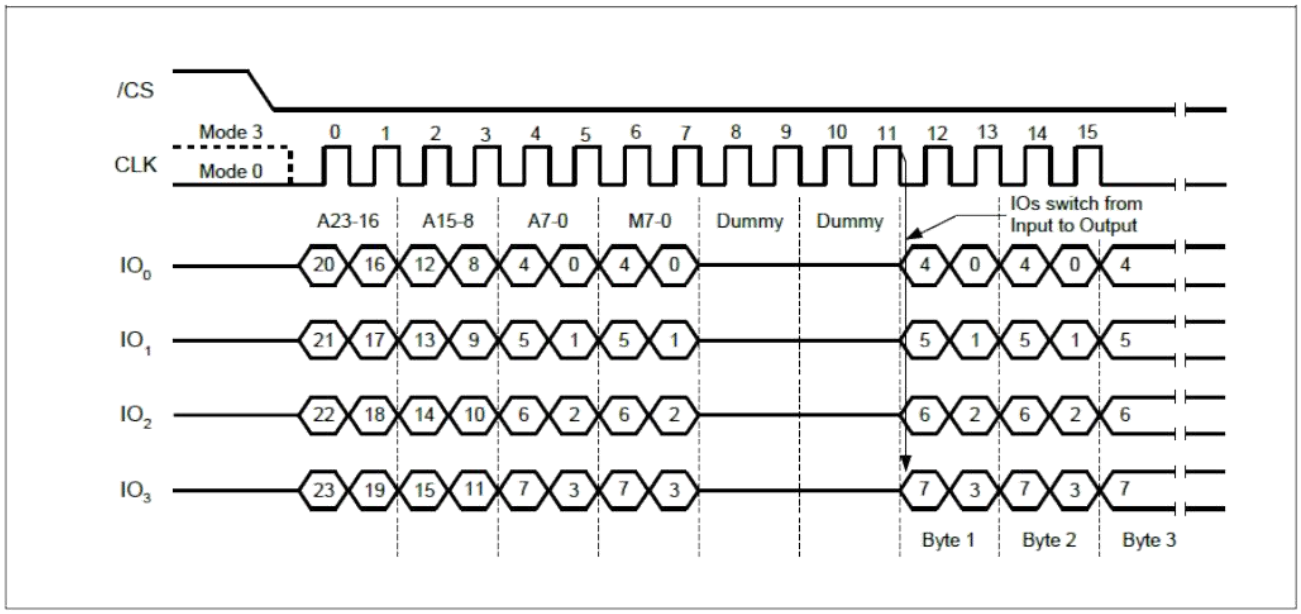


Figure 14b. Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page.

The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section 9.2.13 for detail descriptions.

9.2.12. Word Read Quad I/O (E7h)

The Word Read Quad I/O (E7h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lowest Address bit (A0) must equal 0 and only two Dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.

Word Read Quad I/O with "Continuous Read Mode"

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 15a. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the E7h instruction code, as shown in Figure 15b. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

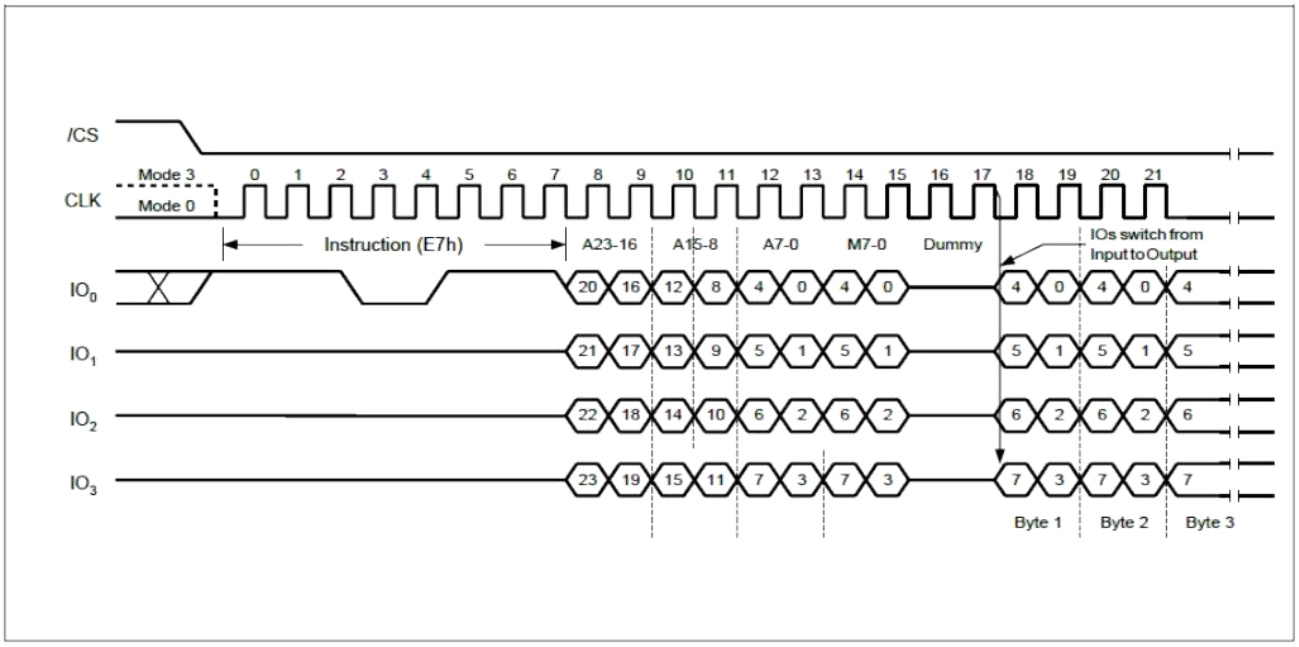


Figure 15a. Word Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

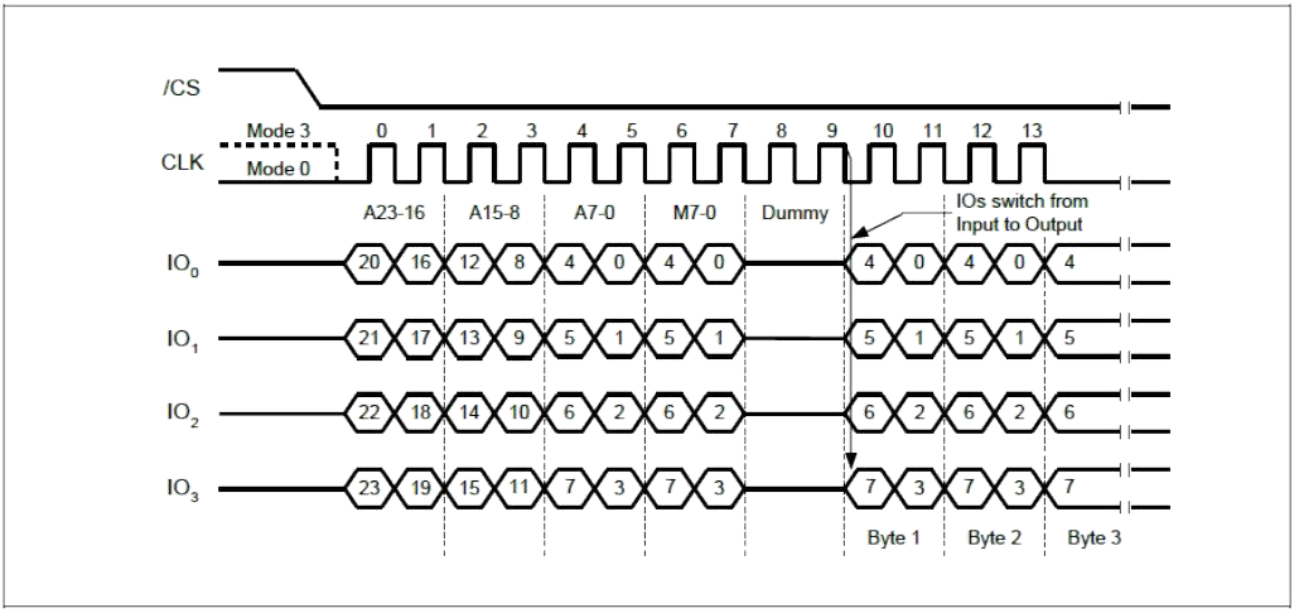


Figure 15b. Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)

Word Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to E7h. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64- byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See 9.2.13 for detail descriptions.

9.2.13. Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 16. Wrap bit W7 and the lower nibble W3-0 are not used.

	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	**Wrap Length**	**Wrap Around**	**Wrap Length**
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, the following “Fast Read Quad I/O” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

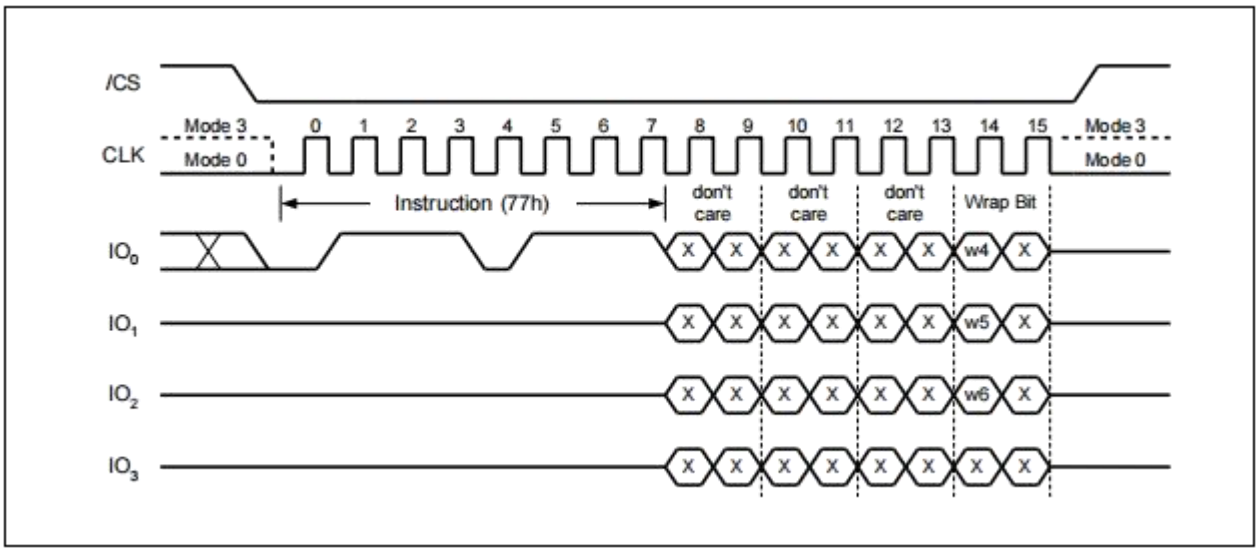


Figure 16. Set Burst with Wrap Instruction

9.2.14. Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 17.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

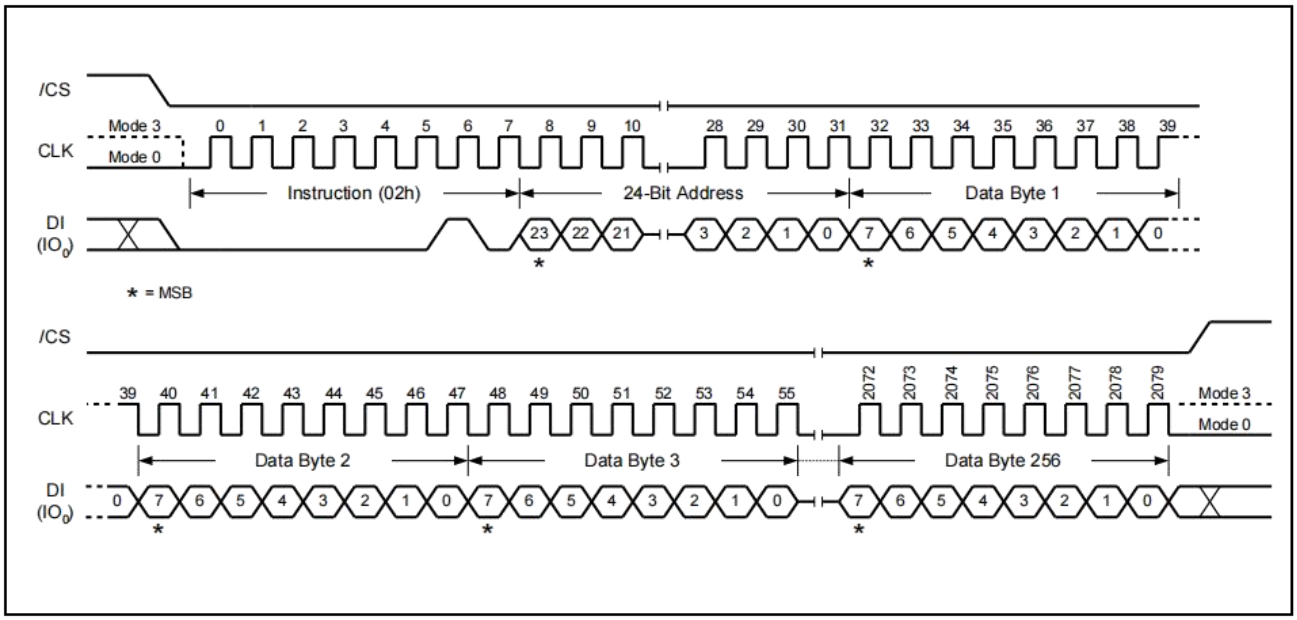


Figure 17. Page Program Instruction

9.2.15. Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO0, IO1, IO2, and IO3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 18.

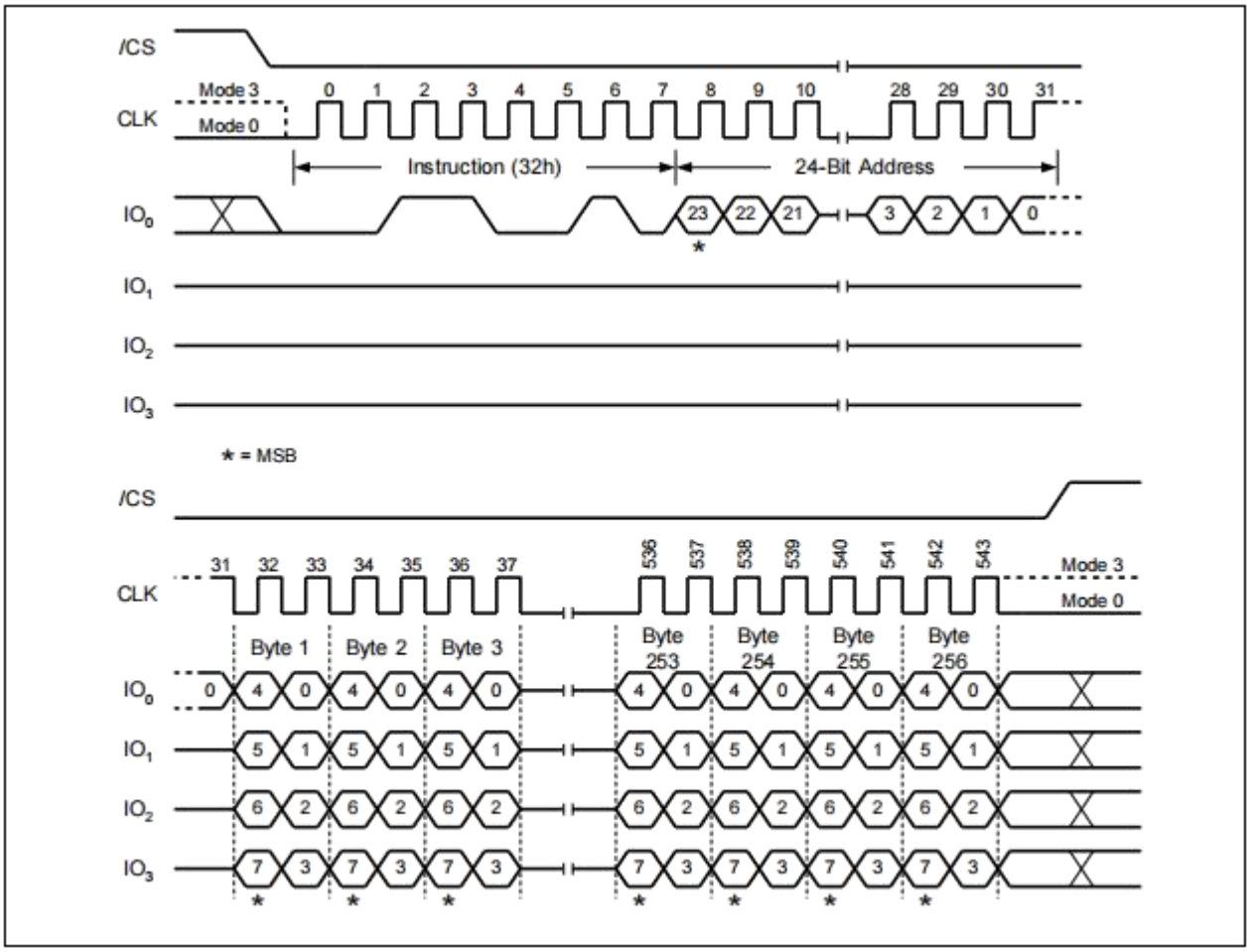


Figure 18. Quad Input Page Program Instruction

8.2.16. Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in Figure19.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

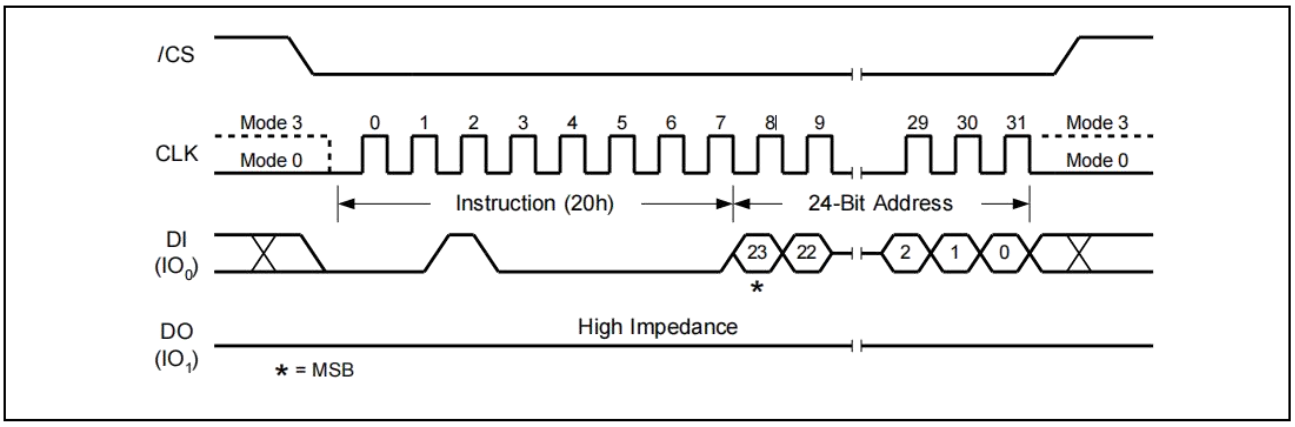


Figure 19. Sector Erase Instruction

9.2.17. 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 20.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

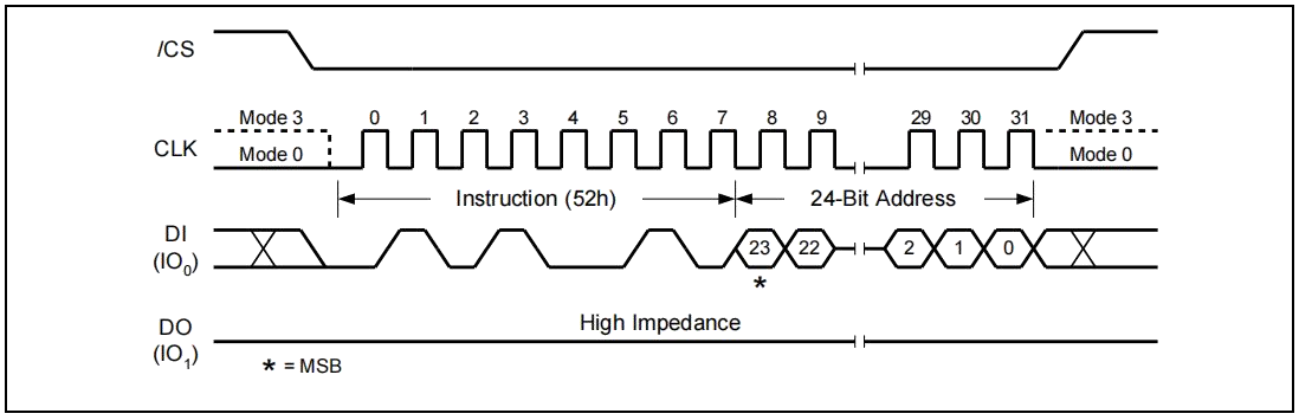


Figure 20. 32KB Block Erase Instruction

9.2.18. 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in Figure 21.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

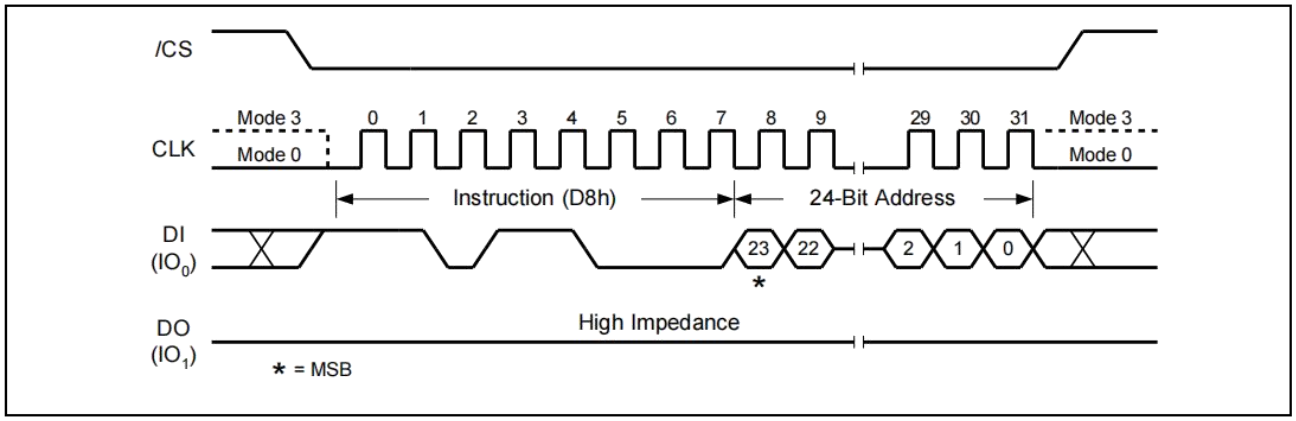


Figure 21. 64KB Block Erase Instruction

9.2.19. Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 22.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits or the Individual Block/Sector Locks.

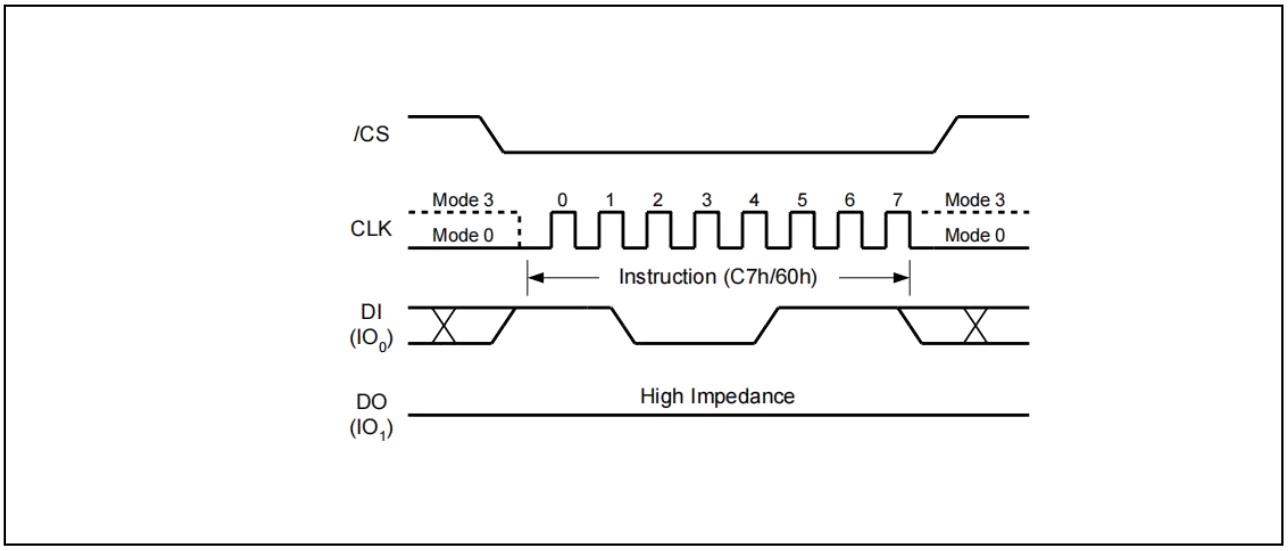


Figure 22. Chip Erase Instruction Sequence Diagram

9.2.20. Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 23.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “tSUS” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “tSUS” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “tSUS” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

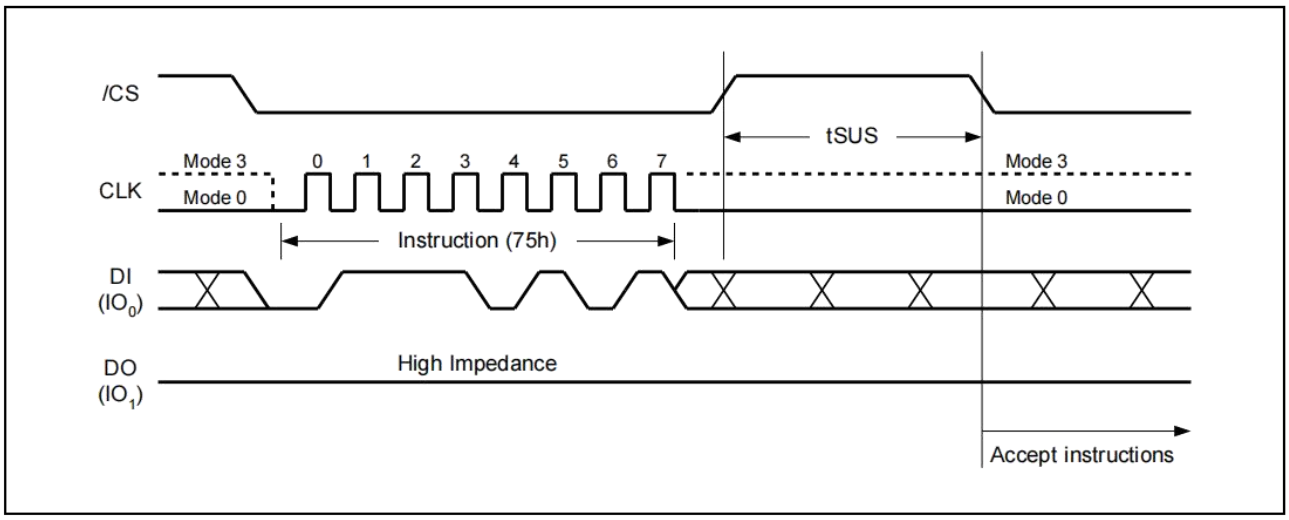


Figure 23. Erase/Program Suspend Instruction

9.2.21. Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 24.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “tSUS” following a previous Resume instruction.

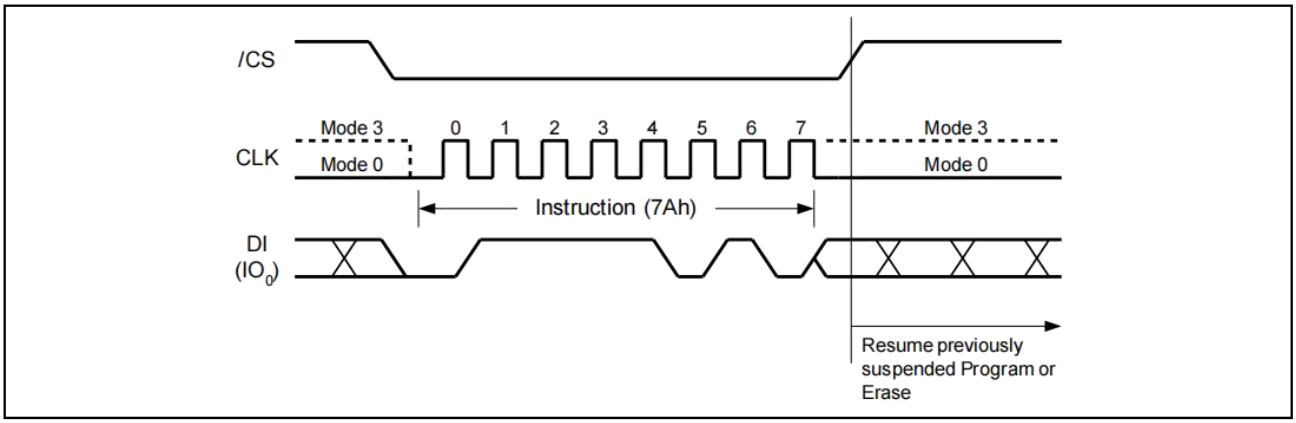


Figure 24. Erase/Program Resume Instruction

9.2.22. Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 25.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release Power-down / Device ID (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

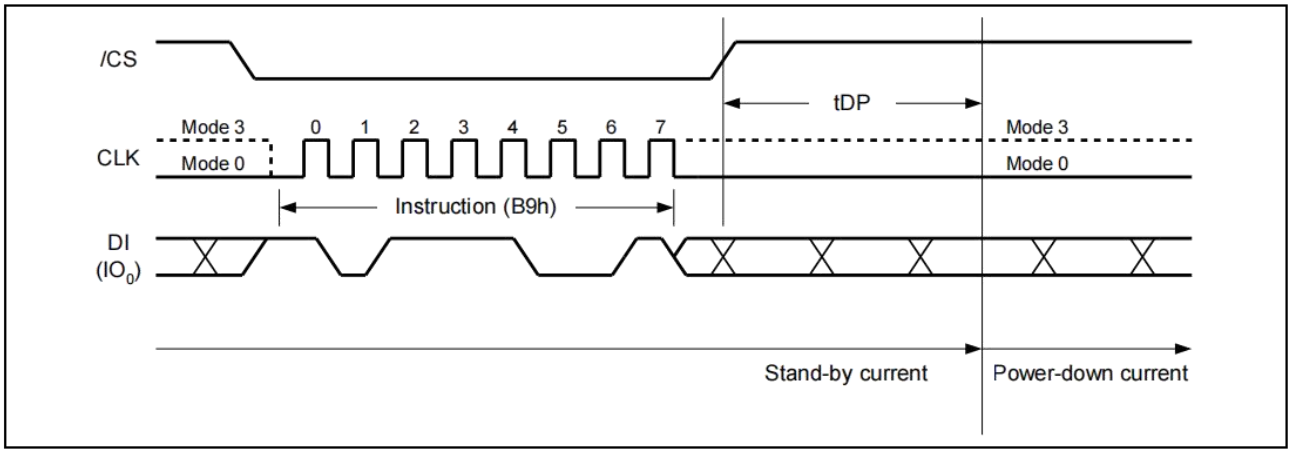


Figure 25. Deep Power-down Instruction

9.2.23. Release Power-down (ABh)

The Release from Power-down instruction is a multi-purpose instruction. It can be used to release the device from the power-down state.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in Figure 26. Release from power-down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

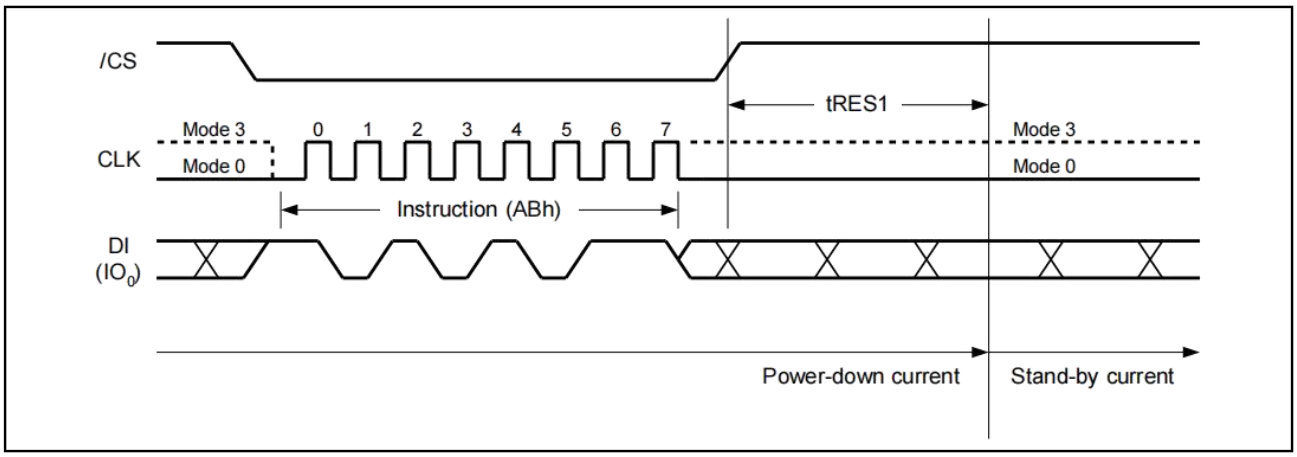


Figure 26. Release Power-down Instruction

9.2.24. Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 27. The Device ID values for the The HG25Q64 are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

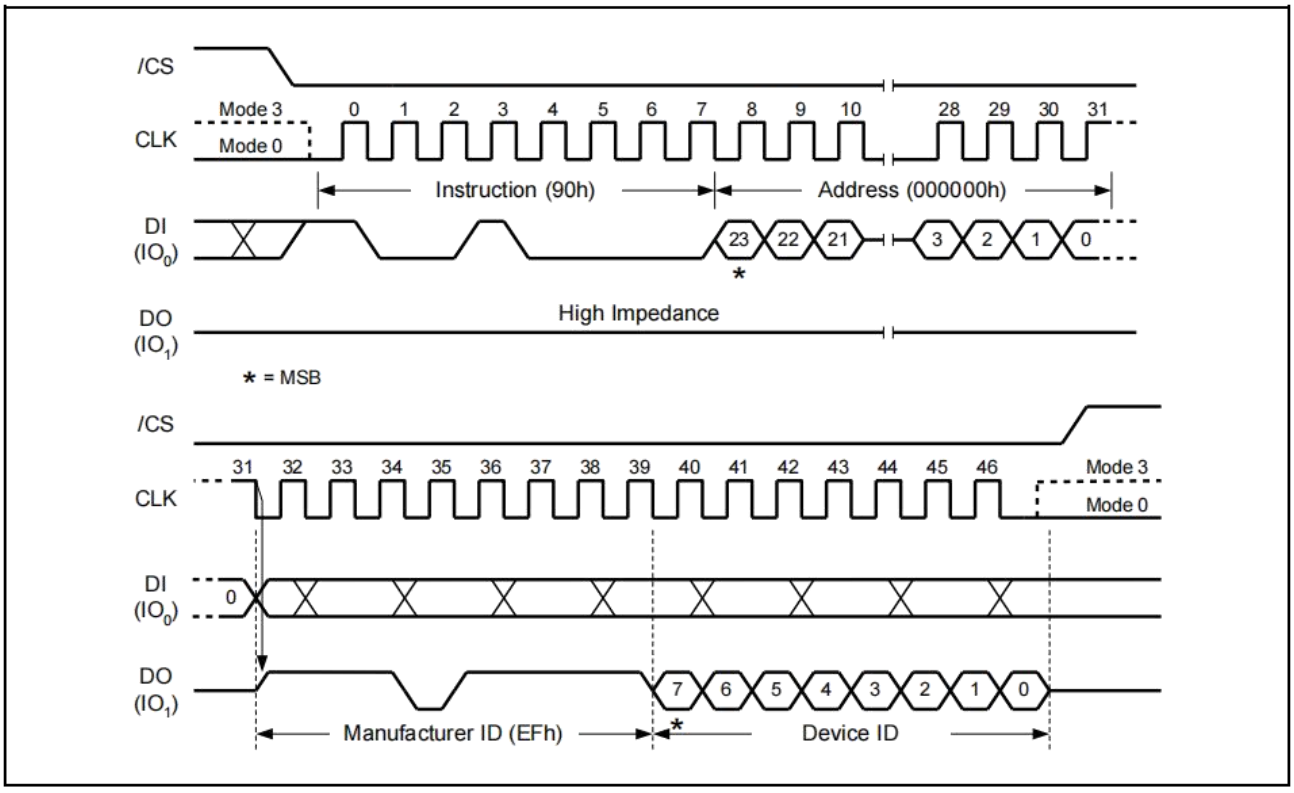


Figure 27. Read Manufacturer / Device ID Instruction

9.2.25. Read JEDEC ID (9Fh)

For compatibility reasons, the HG25Q64provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for Chuangfeixin two Device ID bytes, Memory Type (ID15- ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 28. For memory type and capacity values refer to Manufacturer and Device Identification table.

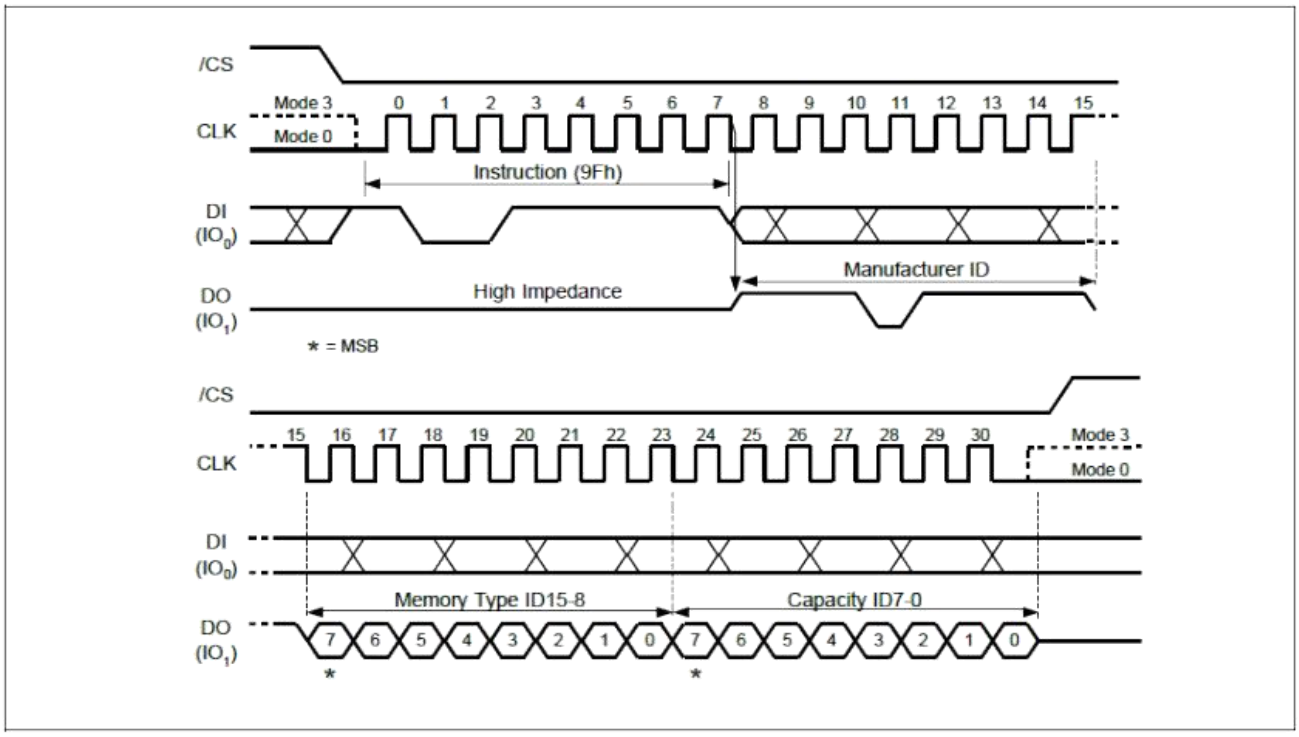


Figure 28. Read JEDEC ID Instruction

9.2.26. Read SFDP Register (5Ah)

The HG25Q64 features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216-serials that is published in 2011. Most Chuangfeixin SPI Flash Memories support the SFDP feature as specified in the applicable datasheet.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0) (1) into the DI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 29. For SFDP register values and descriptions, please refer to the Chuangfeixin SFDP Definition Table.

Notes:

1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

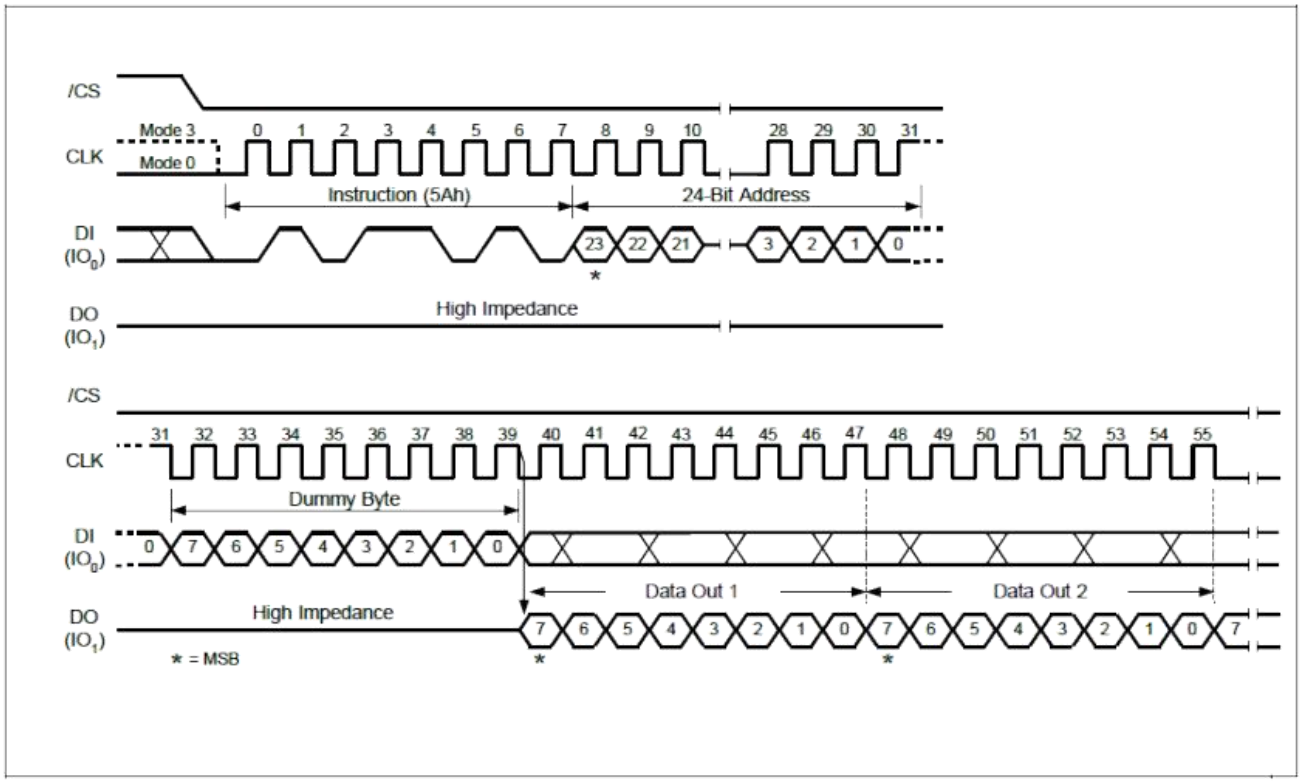


Figure 29. Read SFDP Register Instruction Sequence Diagram

Table 9.2.26a.SFDP Headers Definition Table

SFDP Byte Address	SFDP DWORD Name	Data	Description
00h	SFDP Header 1st DWORD	53h	"S" ASCII. This is the entry point for Read SFDP (5Ah) command i.e. location zero within53h SFDP space
01h		46h	"F" ASCII
02h		44h	"D" ASCII
03h		50h	"P" ASCII
04h	SFDP Header 2nd DWORD	00h	SFDP Minor Revision
05h		01h	SFDP Major Revision
06h		01h	Number of Parameters Headers (zero based, 01h = 2 parameters)
07h		FFh	Unused
08h	Parameter Header 01st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
09h		08h	Parameter Minor Revision(08h=JESD216D)
0Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
0Bh		09h	Parameter Table Length (in double words = Dwords = 4-byte units) 09h = 9 Dwords
0Ch	Parameter Header 02nd DWORD	80h	Parameter Table Pointer Byte 0 (Dwords = 4-byte aligned) JEDEC Basic SPI Flash parameter byte offset = 80h
0Dh		00h	Parameter Table Pointer Byte 1
0Eh		00h	Parameter Table Pointer Byte 2
0Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
10h	Parameter Header 11st DWORD	1Ch	Parameter ID LSB (CFX Vendor Specific ID parameter) 1C
11h		00h	Parameter Minor Revision
12h		01h	Parameter Major Revision
13h		02h	Parameter Table Length (in double words = Dwords = 4-byte units) 02h = 2 Dwords
14h	Parameter Header 12nd DWORD	F8h	Parameter Table Pointer Byte 0 (Dwords = 4-byte aligned)
15h		00h	Parameter Table Pointer Byte 1
16h		00h	Parameter Table Pointer Byte 2
17h		0Ch	Parameter ID MSB (0Ch = JEDEC JEP106B Bank Number 12)

Table 9.2.26b.JEDEC Basic Flash Parameter Definition Table

SFDP Byte Address	SFDP DWORD Name	Data	Description
80h	JEDEC Basic Flash Parameter Dword-1	E5h	Start of SFDP JEDEC parameterBits 7:5 = unused = 111b Bits 4:3 = 05h is volatile status register write instruction and status register is default non-volatile= 00b Bit 2 = Program Buffer > 64Bytes = 1 Bits 1:0 = Uniform 4KB erase is supported throughout the device = 01b
81h		20h	Bits 15:8 = Uniform 4KB erase instruction = 20h
82h		F1h	Bit 23 = Unused = 1b Bit 22 = Supports QOR (1-1-4) Read, Yes = 1b Bit 21 = Supports QIO (1-4-4) Read, Yes =1b Bit 20 = Supports DIO (1-2-2) Read, Yes = 1b Bit 19 = Supports DDR, Yes = 1b, No = 0b Bits 18:17 = Number of Address Bytes, 3 or 4 = 01b Bit 16 = Supports Fast Read SIO and DIO Yes = 1b
83h		FFh	Bits 31:24 = Unused = FFh
84h	JEDEC Basic Flash Parameter Dword-2	FFh	Density in bits, zero based, 16Mb = 00FFFFFFh; 32Mb = 01FFFFFFh; 64Mb = 03FFFFFFh; 128Mb = 07FFFFFFh;256Mb = 0FFFFFFFh;512Mb = 1FFFFFFFh
85h		FFh	
86h		FFh	
87h		03h	
88h	JEDEC Basic Flash Parameter Dword-3	44h	Bits 7:5 = number of QIO Mode cycles = 010b Bits 4:0 = number of Fast Read QIO Dummy cycles = 00100b for default latency code
89h		EBh	Fast Read QIO instruction code
8Ah		08h	Bits 23:21 = number of Quad Out Mode cycles = 000b Bits 20:16 = number of Quad Out Dummy cycles = 01000b for default latency code
8Bh		6Bh	Quad Out instruction code
8Ch	JEDEC Basic Flash Parameter Dword-4	08h	Bits 7:5 = number of Dual Out Mode cycles = 000b Bits 4:0 = number of Dual Out Dummy cycles = 01000b for default latency code
8Dh		3Bh	Dual Out instruction code
8Eh		40h	Bits 23:21 = number of Dual I/O Mode cycles = 010b Bits 20:16 = number of Dual I/O Dummy cycles = 00000b for not support
8Fh		BBh	Dual I/O instruction code
90h	JEDEC Basicn Flash Parameter Dword-5	EEh	Bits 7:5 RFU (Reserved for Future Use) = 111bBit 4 = QPI (4-4-4) not supported = 0b Bits 3:1 RFU = 111b Bit 0 = Dual All (2-2-2) not supported = 0b
91h		FFh	Bits 15:8 = RFU = FFh
92h		FFh	Bits 23:16 = RFU = FFh
93h		FFh	Bits 31:24 = RFU = FFh

Continued – next page JEDEC Basic Flash Parameter Definition Table (cont'd)

94h	JEDEC Basic Flash Parameter Dword-6	FFh	Bits 7:0 = RFU = FFh
95h		FFh	Bits 15:8 = RFU = FFh
96h		00h	Bits 23:21 = number of Dual All Mode cycles not supported = 000b Bits 20:16 = number of Dual All Dummy cycles not supported = 00000b
97h		FFh	Bits 23:16 = RFU = FFh
98h	JEDEC Basic Flash Parameter Dword-7	FFh	Bits 7:0 = RFU = FFh
99h		FFh	Bits 15:8 = RFU = FFh
9Ah		00h	Bits 23:21 = number of QPI Mode cycles not supported = 000b Bits 20:16 = number of QPI Dummy cycles not supported = 00000b for default latencycode
9Bh		FFh	QPI Fast Read instruction code not supported
9Ch	JEDEC Basic Flash Parameter Dword-8	0Ch	Sector type 1 size 2^N Bytes = 4KB = 0Ch (for Uniform 4KB)
9Dh		20h	Sector type 1 instruction
9Eh		0Fh	Sector type 2 size 2^N Bytes = 32KB = 0Fh (for Uniform 32KB)
9Fh		52h	Sector type 2 instruction
A0h	JEDEC Basic Flash Parameter Dword-9	10h	Sector type 3 size 2^N Bytes = 64KB = 10h (for Uniform 64KB)
A1h		D8h	Sector type 3 instruction
A2h		00h	Sector type 4 size 2^N Bytes = not supported = 00h
A3h		FFh	Sector type 4 instruction = not supported = FFh

Table 9.2.26c. Vendor specific Definition Table

SFDP Byte Address	SFDP DWORD Name	Data	Description
F8h	Unique Id Parameter Dword-1	01h	Unique Id
F9h		XXh	
FAh		XXh	
FBh		XXh	
FCh	Unique Id Parameter Dword-2	XXh	
FDh		XXh	
FEh		XXh	
FFh		F6h	

9.2.27. Erase Security Registers (44h)

The HG25Q64 offers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Don’t Care
Security Register #2	00h	0 0 1 0	0 0 0 0	Don’t Care
Security Register #3	00h	0 0 1 1	0 0 0 0	Don’t Care

The Erase Security Register instruction sequence is shown in Figure 30. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to section 8.1.9 for detail descriptions).

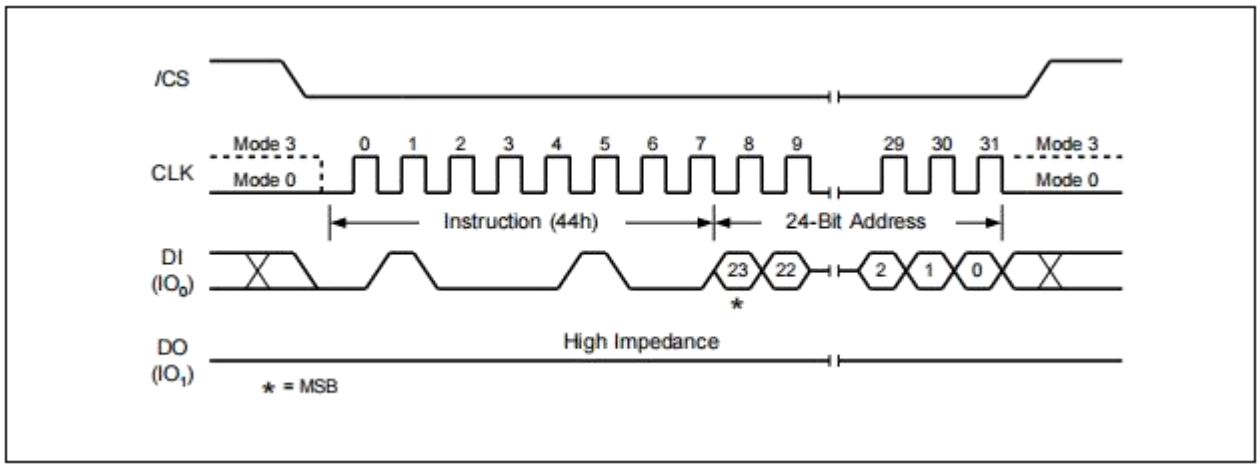


Figure 30. Erase Security Registers Instruction

9.2.28. Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin.

The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

The Program Security Register instruction sequence is shown in Figure 31. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See 8.1.9,for detail descriptions)

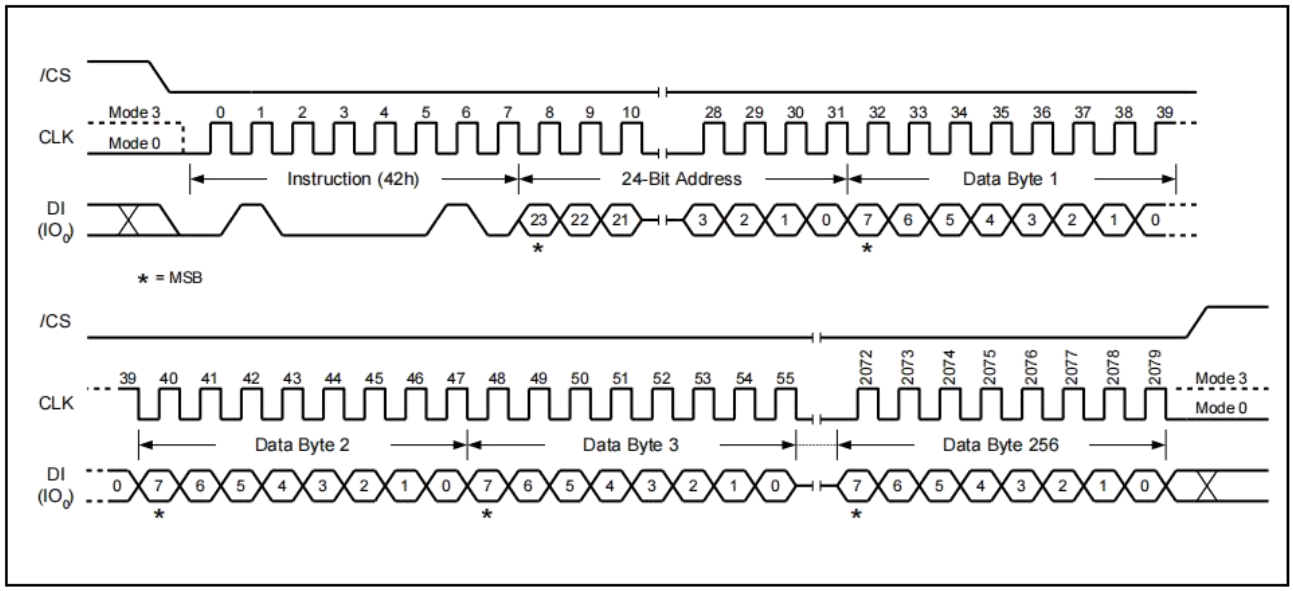


Figure 31. Program Security Registers Instruction

9.2.29. Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the four security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 32. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Register #1	00h	0 0 0 1	0 0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0 0	Byte Address

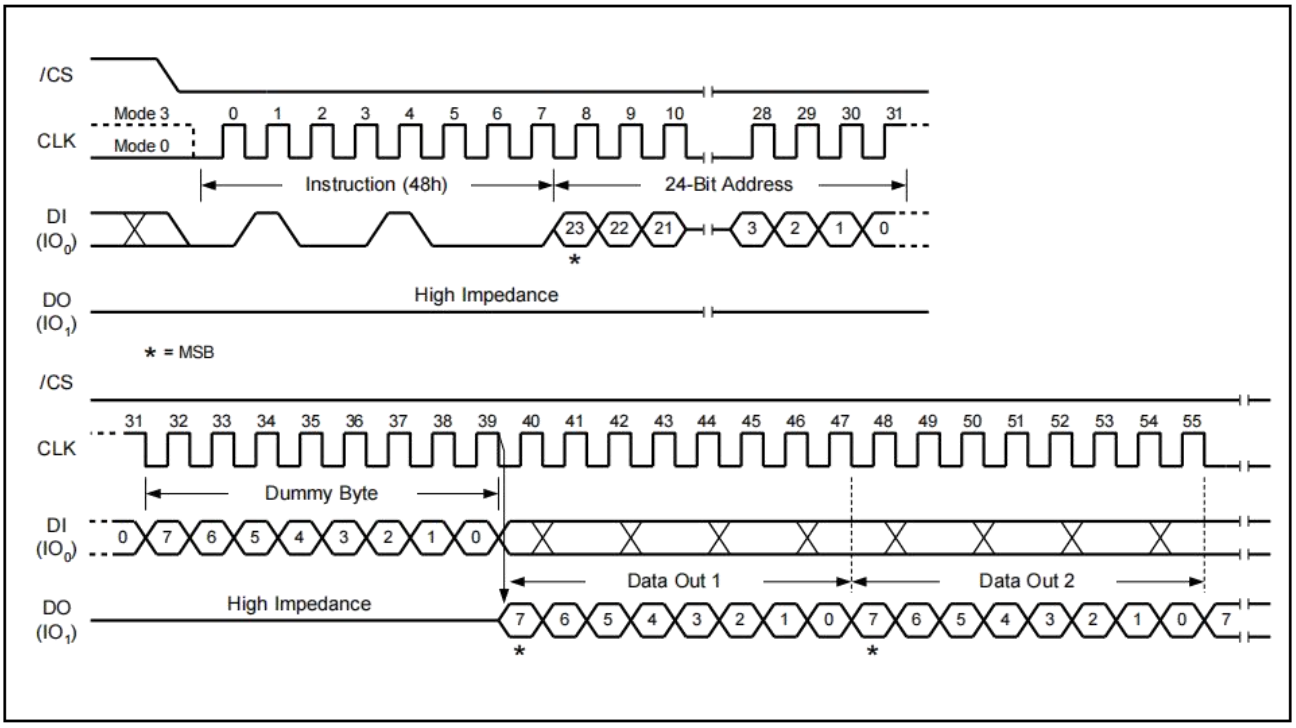


Figure 32. Read Security Registers Instruction

9.2.30. Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the HG25Q64 provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), and Wrap Bit setting (W6-W4).

“Enable Reset (66h)” and “Reset (99h)” instructions can be issued in SPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

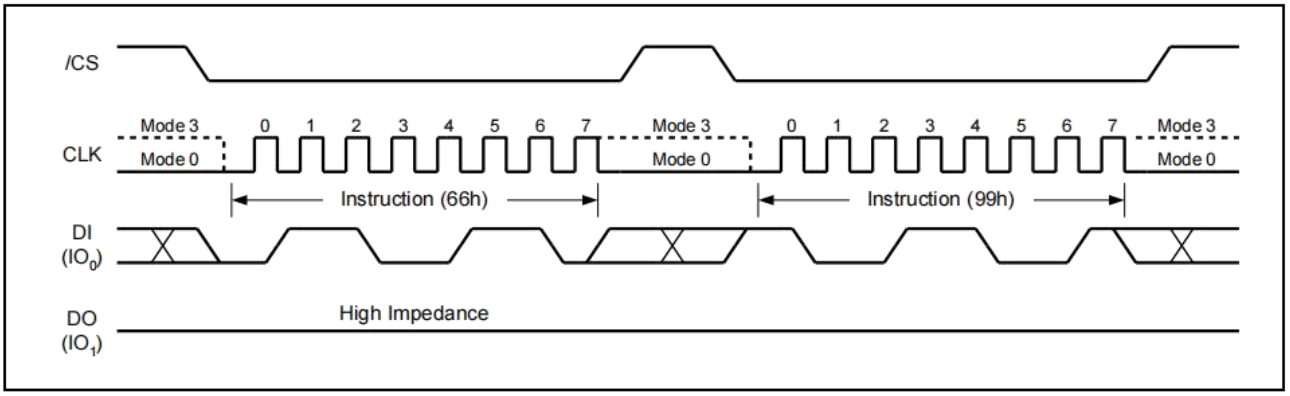


Figure 33. Enable Reset and Reset Instruction Sequence

10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to 4.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		245	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

10.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	Industrial and industrial Plus Temp	3.0	3.6	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C
		Industrial Plus	–40	+105	°C

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

10.3 Power-Up Power-Down Timing and Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}[1]	20		μs
Time Delay Before Write Instruction	t_{PUW}[1]	5		ms
Write Inhibit Threshold Voltage	V_{WI}[1]	1	2	V

Note:

1. These parameters are characterized only.
2. Normal precautions must be taken for supply rail decoupling to stabilize the VCC supply at the device. Each device in a system should have the VCC rail decoupled by a suitable capacitor close to the package supply connection (this capacitor is generally of the order of 20μf, 0.1μf and 0.01μf in parallel).
3. CS# must track Vcc during power up, if it is not available, CS# ahead of Vcc power up timing sequence is recommended.

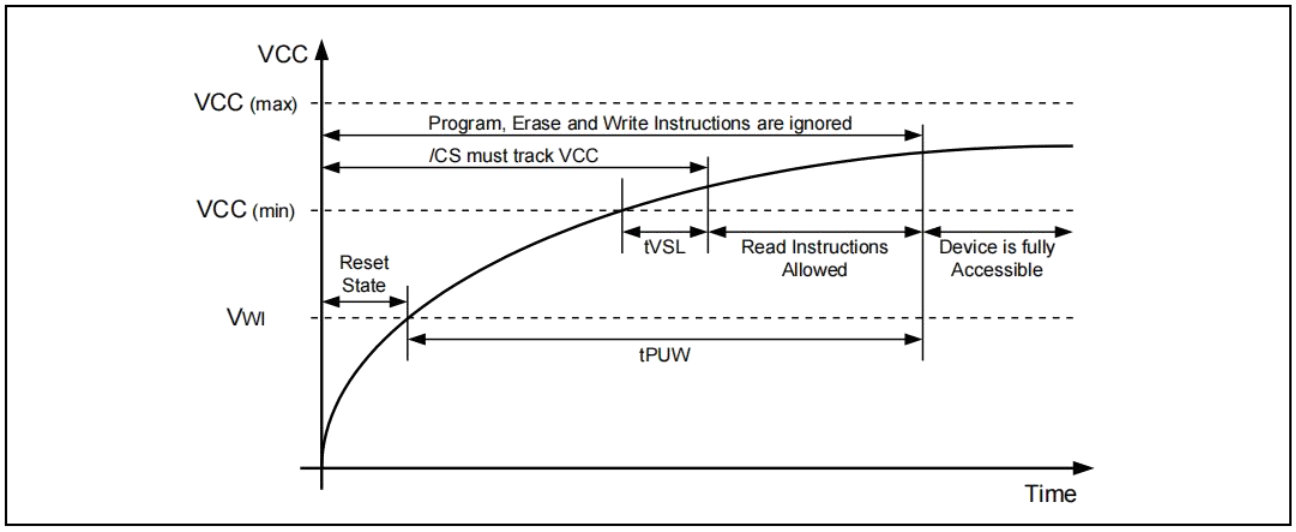


Figure 34a. Power-up Timing and Voltage Levels

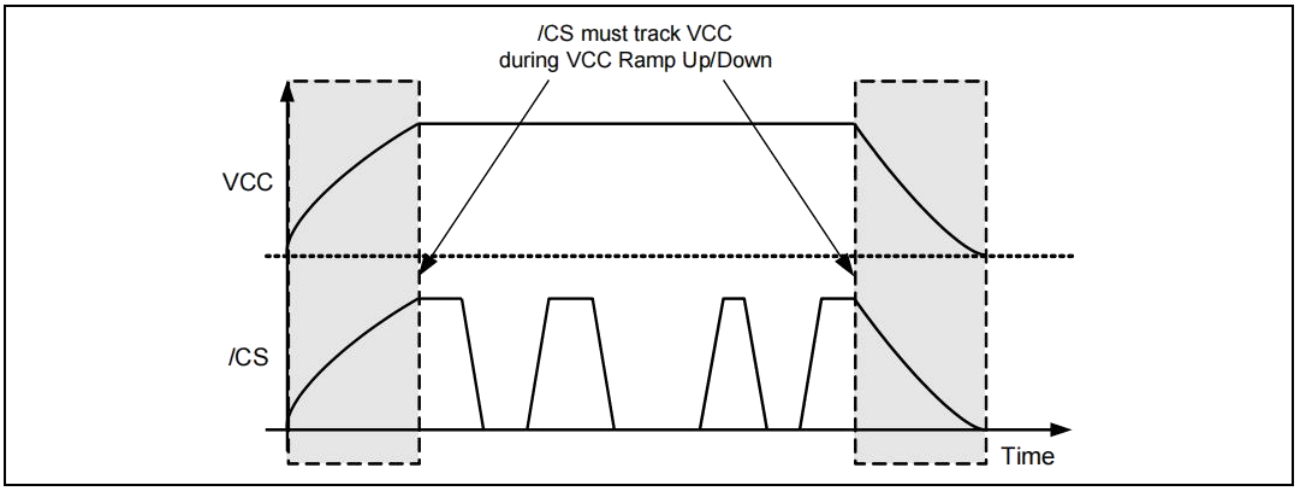


Figure 34b. Power-up, Power-Down Requirement

10.4 DC Electrical Characteristics-

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V(1)			6	pF
Output Capacitance	Cout(1)	V_{OUT} = 0V(1)			8	pF
Input Leakage	I_{LI}				±2	μA
I/O Leakage	I_{LO}				±2	μA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		10	50	μA
Power-down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC		1	15	μA
Current Read Data / Dual /Quad 50MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		8	15	mA
Current Read Data / Dual /Quad 80MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		10	18	mA
Current Read Data / Dual Output Read/QuadOutput Read 104MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		12	20	mA
Current Write StatusRegister	I_{CC4}	/CS = VCC		20	25	mA
Current Page Program	I_{CC5}	/CS = VCC		20	25	mA
Current Sector/BlockErase	I_{CC6}	/CS = VCC		20	25	mA
Current Chip Erase	I_{CC7}	/CS = VCC		20	25	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 μA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = –100 μA	VCC – 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.
2. Checker Board Pattern.

10.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR, TF		5	ns
Input Pulse Voltages	VIN	0.2 VCC to 0.8 VCC		V
Input Timing Reference Voltages	IN	0.5 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

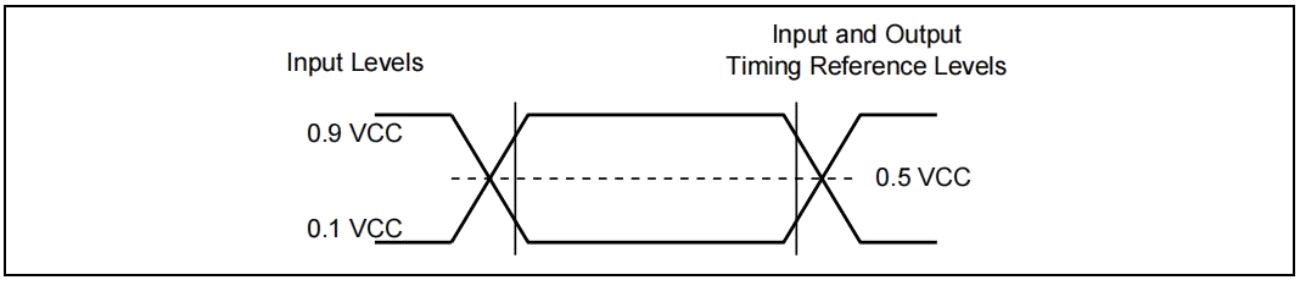


Figure 35. AC Measurement I/O Waveform

10.6 AC Electrical Characteristics

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for Fast Read(0Bh), Dual Output(3Bh), Dual I/O(BBh)	F_{R1}	f_{C1}	D.C		104	MHz
Clock frequency for Quad Output(6Bh), Quad I/O(EBh), Quad I/O Word Fast Read (E7h)	F_{R2}	f_{C2}	D.C		80	MHz
Clock frequency for Read Data(03h), Read Status Register(05h/35h/15h), Read Identification(9Fh)	f_R		D.C		55	MHz
Clock frequency for all Identifications, except Read Data	F_C		D.C		104	MHz
Clock High, Low Time for all instructions except for Read Data (03h)	t_{CLH}, t_{CLL} (1)		45% PC			ns
Clock High, Low Time for Read Data (03h) instruction	t_{CRLH}, t_{CRLL} (1)		45% PC			ns
Clock Rise Time peak to peak	t_{CLCH} (2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL} (2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	3			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		3			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	3.5			ns
Data In Hold Time	t_{CHDX}	t_{DH}	2			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (for Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Erase or Program or Write)	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	t_{SHQZ} (2)	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_V			8	ns
Output Hold Time	t_{CLQX}	t_{HO}	1.5			ns

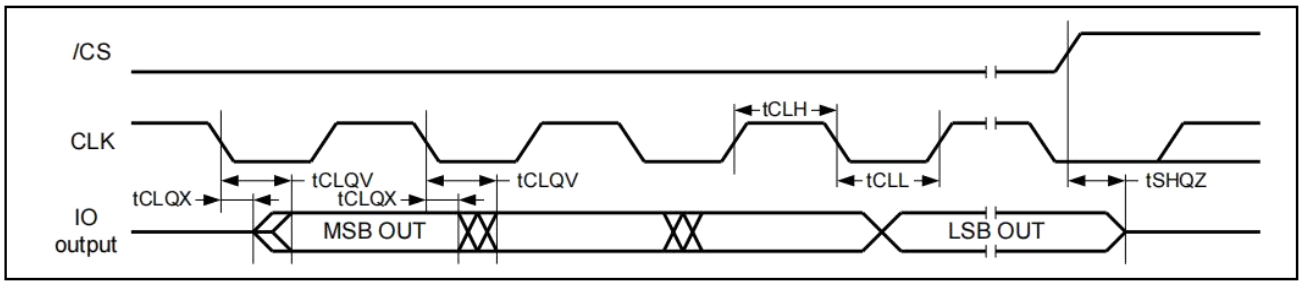
Continued – next page AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Write Protect Setup Time Before /CS Low	t_{WHSL}(3)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}(3)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without ID Read	t_{RES1}(2)				3	µs
/CS High to Standby Mode with ID Read	t_{RES2}(2)				1.8	µs
/CS High to next Instruction after Suspend	t_{SUS}(2)				20	µs
/CS High to next Instruction after Reset	t_{RST}(2)				30	µs
/RESET pin Low period to reset the device	t_{RESET}(2)		1			µs
Write Status Register Time	t_W			10	15	ms
Page Program Time	t_{PP}			0.4	3	ms
Sector Erase Time (4KB)	t_{SE}			45	400	ms
Block Erase Time (32KB)	t_{BE1}			120	1,600	ms
Block Erase Time (64KB)	t_{BE2}			150	2,000	ms
Chip Erase Time	t_{CE}			20	100	s

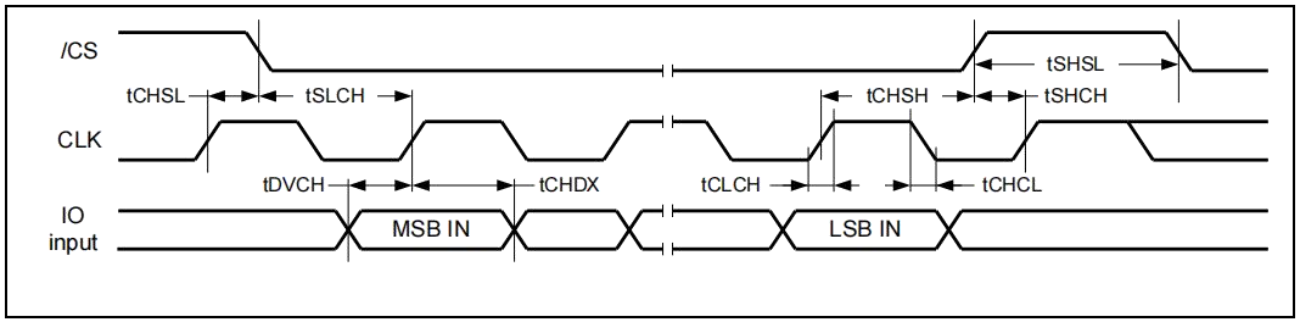
Notes:

1. Clock high or Clock low must be more than or equal to 45%Pc. Pc=1/$f_{C(MAX)}$
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.
4. Quad Read are available at VIH>=0.9Vcc & VIL<=0.1Vcc

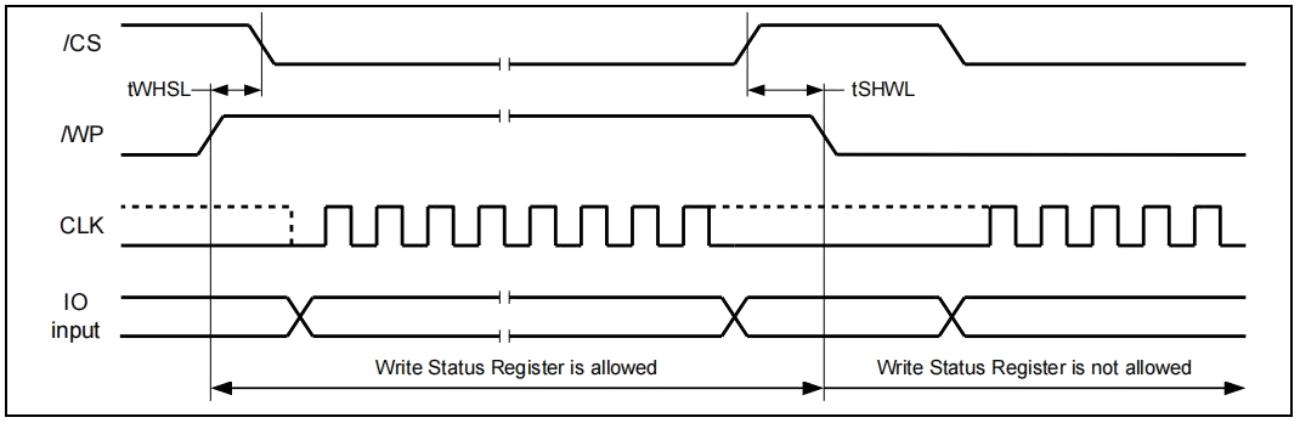
10.7 Serial Output Timing



10.8 Serial Input Timing

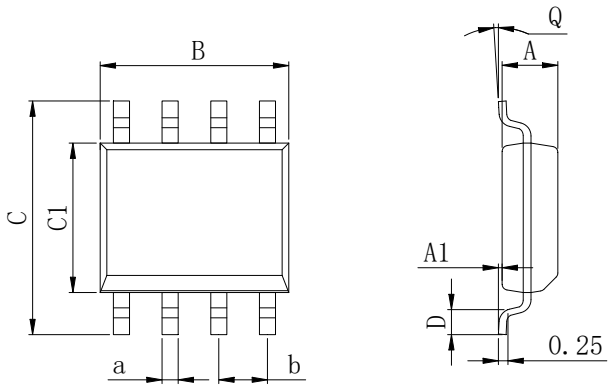


10.9 /WP Timing



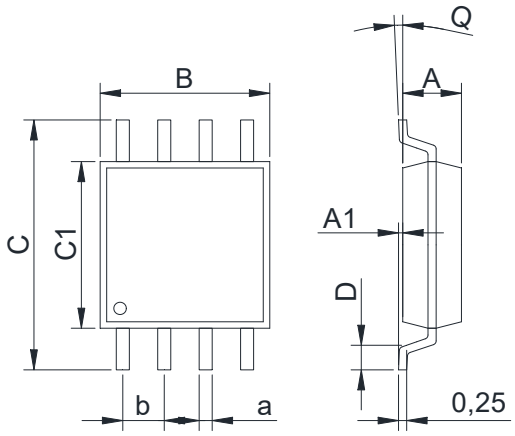
11. Physical Dimensions

11.1. SOP-8 150mil



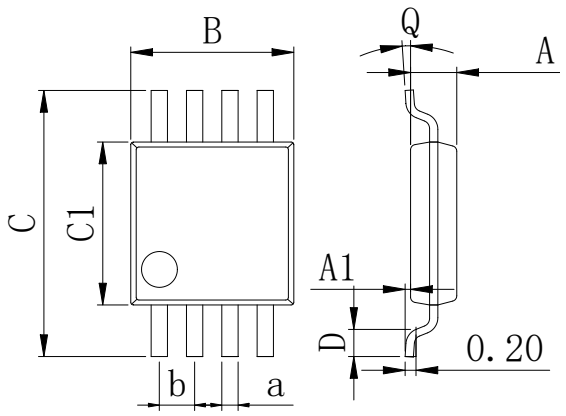
Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

11.2. SOP-8 208MIL



Dimensions In Millimeters(SOP-8 208MIL)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.70	0.05	5.18	7.70	5.18	0.5	0°	0.35	1.27 BSC
Max:	1.91	0.25	5.38	8.70	5.38	0.8	8°	0.48	

11.3. MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

Revision History

DATE	REVISION	PAGE
2020-3-4	New	1-61
2023-7-21	Update encapsulation type	1

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