TC6321

N- and P-Channel Enhancement-Mode MOSFET Pair

Features

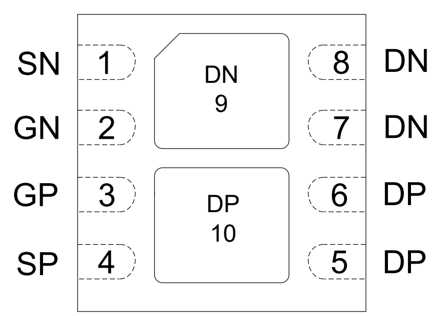
- Integrated Gate-to-Source Resistor
- Integrated Gate-to-Source Zener Diode
- Low Threshold
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speeds
- Free from Secondary Breakdown
- Low Input and Output Leakage
- Independent, Electrically Isolated N- and P-Channels
- 8-Lead Very Thin Plastic Dual Flat, No Lead, 6 x 5 mm VDFN Package

Applications

- High-Voltage Pulser
- Amplifiers
- Buffers
- Piezoelectric Transducer Drivers
- General-Purpose Line Drivers
- Logic-Level Interfaces

Package Types

TC6321
6 x 5 VDFN*



* Includes Dual Exposed Thermal Pads (EP); see Table 3-1.

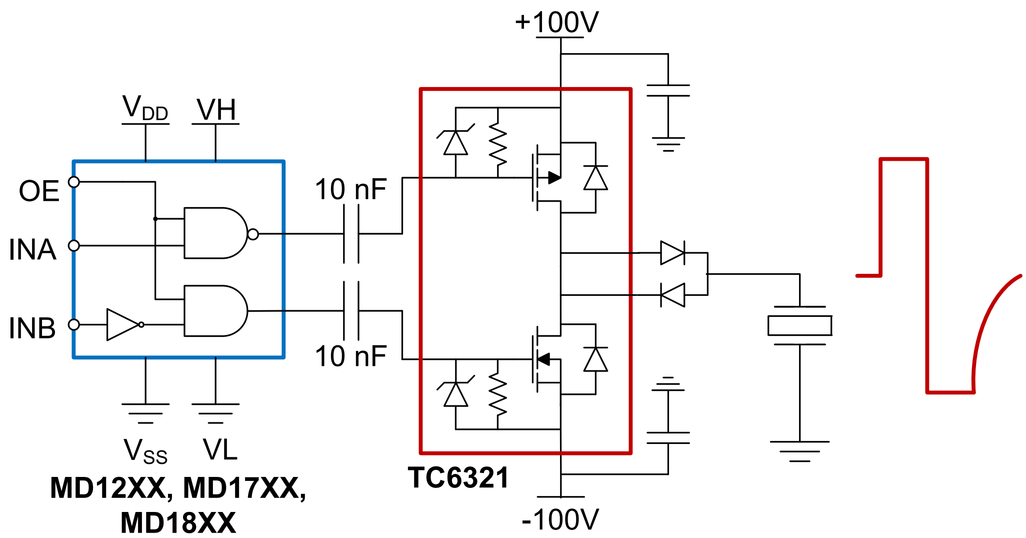
Description

The TC6321 consists of high-voltage, low-threshold N-channel and P-channel MOSFETs in an 8-Lead VDFN package. Both MOSFETs have integrated gate-to-source resistors and gate-to-source Zener diode clamps, which are desired for high-voltage pulser applications.

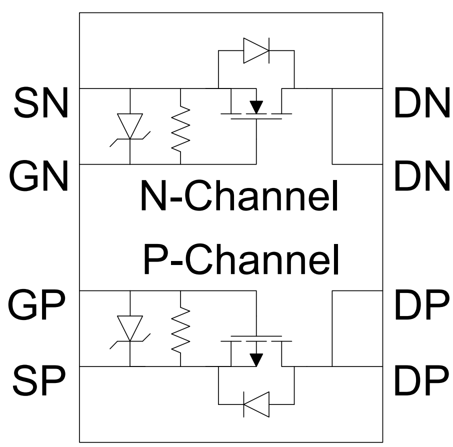
The TC6321 is a complimentary, high-speed, high-voltage, gate-clamped N- and P-channel MOSFET pair, which utilizes an advanced vertical DMOS structure and the well-proven silicon-gate manufacturing process. This combination produces a device with the power-handling capabilities of bipolar transistors and with the high-input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Drain-to-Source Voltage .... BV_{DSX}
Drain-to-Gate Voltage .... BV_{DGX}
Operating and Storage Temperature .... -55°C to +175°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL DC AND AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $T_A = T_J = +25°C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
DC Parameters (Note 1)						
Drain-to-Source Breakdown Voltage	BV_{DSS}	200	—	—	V	V_{GS} = 0V, I_D = 2.0 mA
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	2.0	V	$V_{GS} = V_{DS}$, I_D = 1.0 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	–4.5	mV/ºC	$V_{GS} = V_{DS}$, I_D = 1.0 mA **(Note 2)**
Gate-to-Source Shunt Resistor	R_{GS}	10	—	50	kΩ	I_{GS} = 100 µA
Gate-to-Source Zener Voltage	VZ_{GS}	13.2	—	25	V	I_{GS} = 2 mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	10.0	µA	V_{DS} = 200V V_{GS} = 0V
		—	—	1.0	mA	V_{DS} = 200V, V_{GS} = 0V T_J = +125°C **(Note 2)**
On-State Drain Current	$I_{D(ON)}$	1.0	—	—	A	V_{GS} = 4.5V, V_{DS} = 25V
		2.0	—	—		V_{GS} = 10V, V_{DS} = 25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	8.0	Ω	V_{GS} = 4.5V, I_D = 150 mA
		—	—	7.0		V_{GS} = 10V, I_D = 1.0A
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1.0	%/ºC	V_{GS} = 4.5V, I_D = 150 mA **(Note 2)**
AC Parameters (Note 2)						
Forward Transconductance	G_{FS}	400	—	—	mmho	V_{GS} = 25V, I_D= 500 mA
Input Capacitance	C_{ISS}	—	—	110	pF	V_{GS} = 0V V_{DS} = 25V f = 1.0 MHz
Common Source Output Capacitance	C_{OSS}	—	—	60		
Reverse Transfer Capacitance	C_{RSS}	—	—	23		
Turn-On Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{GS} = 10V V_{DS} = 25V I_D = 1.0A R_{GEN} = 25Ω
Rise Time	t_r	—	—	15		
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	20		
Fall Time	t_f	—	—	15		

Note 1: Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 µs pulse, 2% duty cycle

2: Specification is obtained by characterization and is not 100% tested.

N-CHANNEL DC AND AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $T_A = T_J = +25°C$.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Diode Parameters						
Diode Forward Voltage Drop	V_{SD}	—	—	1.8	V	V_{GS}= 0V, I_{SD}= 500 mA (Note 1)
Reverse Recovery Time	t_{rr}	—	100	—	ns	V_{GS} = 0V, I_{SD} = 500 mA $d_{iF/dt}$ = 25 A/µ (Note 2)

Note 1: Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 µs pulse, 2% duty cycle

2: Specification is obtained by characterization and is not 100% tested.

P-CHANNEL DC AND AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $T_A = T_J = +25°C$.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
DC Parameters (Note 1)						
Drain-to-Source Breakdown Voltage	BV_{DSS}	–200	—	—	V	V_{GS}= 0V, I_D= –2.0 mA
Gate Threshold Voltage	$V_{GS(th)}$	–1.0	—	–2.4	V	$V_{GS} = V_{DS}$, I_D = –1.0 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	4.5	mV/ºC	$V_{GS} = V_{DS}$, I_D = –1.0 mA (Note 2)
Gate-to-Source Shunt Resistor	R_{GS}	10	—	50	kΩ	I_{GS} = 100 µA
Gate-to-Source Zener Voltage	VZ_{GS}	13.2	—	25	V	I_{GS} = –2 mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	–10.0	µA	V_{DS} = 200V, V_{GS} = 0V
		—	—	–1.0	mA	V_{DS} = 200V, V_{GS} = 0V T_J = +125°C, (Note 2)
On-State Drain Current	$I_{D(ON)}$	–1.0	—	—	A	V_{GS} = –4.5V, V_{DS} = –25V
		–2.0	—	—		V_{GS} = –10V, V_{DS} = –25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	10	Ω	V_{GS} = –4.5V, I_D = –150 mA
		—	—	8.0		V_{GS} = –10V, I_D = –1.0A
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1.0	%/°C	V_{GS} = –25V, I_D = –200 mA (Note 2)
AC Parameters (Note 2)						
Forward Transconductance	G_{FS}	400	—	—	mmho	V_{GS} = –25V, I_D = –500 mA
Input Capacitance	C_{ISS}	—	—	200	pF	V_{GS} = 0V V_{DS} = –25V f = 1.0 MHz
Common Source Output Capacitance	C_{OSS}	—	—	55		
Reverse Transfer Capacitance	C_{RSS}	—	—	30		
Turn-On Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{GS} = –10V V_{DS} = –25V I_D = –1.0A R_{GEN} = 25Ω
Rise Time	t_r	—	—	15		
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	20		
Fall Time	t_f	—	—	15		

Note 1: Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 µs pulse, 2% duty cycle

2: Specification is obtained by characterization and is not 100% tested.

P-CHANNEL DC AND AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $T_A = T_J = +25°C$.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
Diode Parameters						
Diode Forward Voltage Drop	V_{SD}	—	—	–1.8	V	V_{GS}= 0V, I_{SD}= –500 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	100	—	ns	V_{GS} = 0V, I_{SD} = –500 mA $d_{iF/dt}$ = -25 A/µs (**Note 2**)

Note 1: Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 µs pulse, 2% duty cycle

2: Specification is obtained by characterization and is not 100% tested.

Temperature Specifications						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature	T_J	–40	—	+150	°C	
Storage Temperature	T_A	–55	—	+175	°C	
Thermal Package Resistances						
Thermal Resistance, 6x5 mm VDFN-8LD	θ_{JC}	—	1.43	—	°C/W	
	θ_{JA}	—	34.4	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

> **Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (for example, outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = T_J = 25°C$.

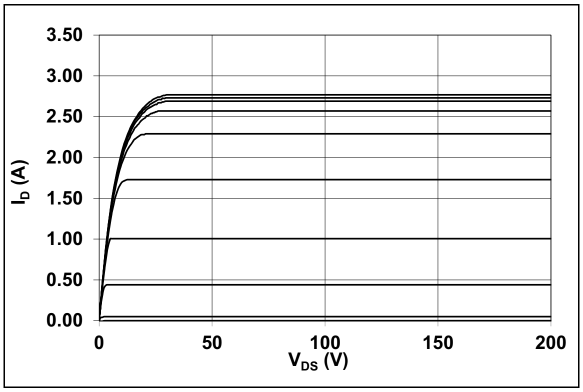


FIGURE 2-1: N-Channel I_D vs. V_{DS} (Output Characteristics).

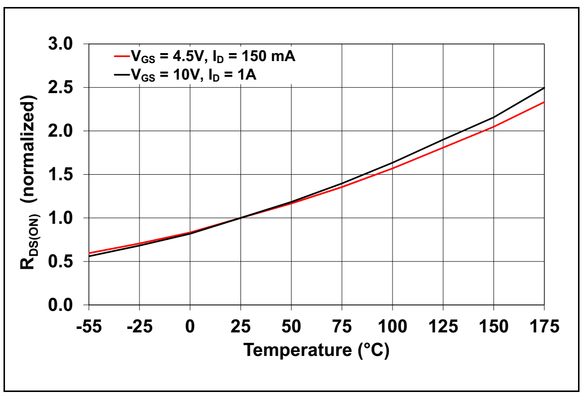


FIGURE 2-2: N-Channel On-Resistance vs. Temperature.

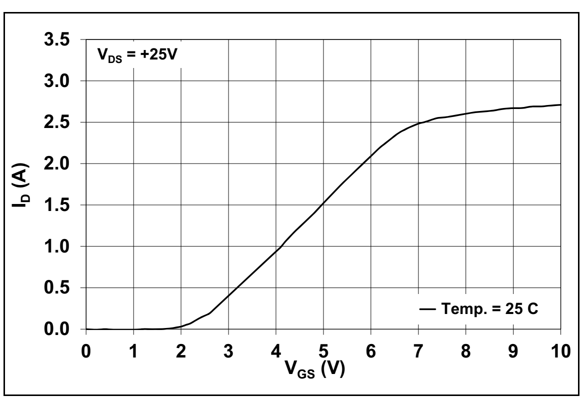


FIGURE 2-3: N-Channel I_D vs. V_{GS}.

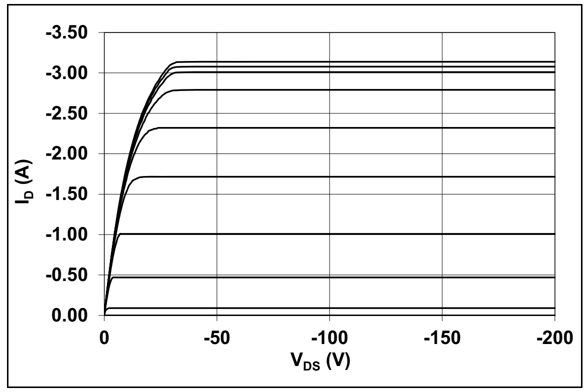


FIGURE 2-4: P-Channel I_D vs. V_{DS} (Output Characteristics).

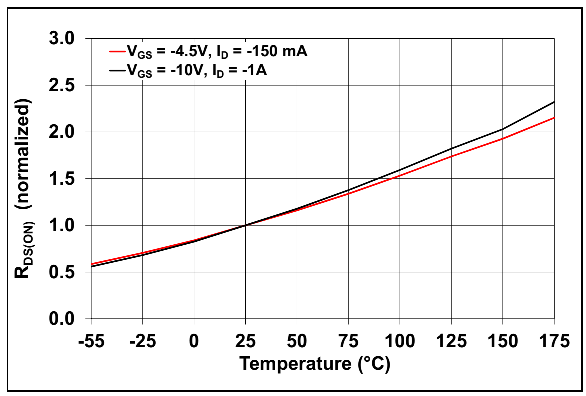


FIGURE 2-5: P-Channel On-Resistance vs. Temperature.

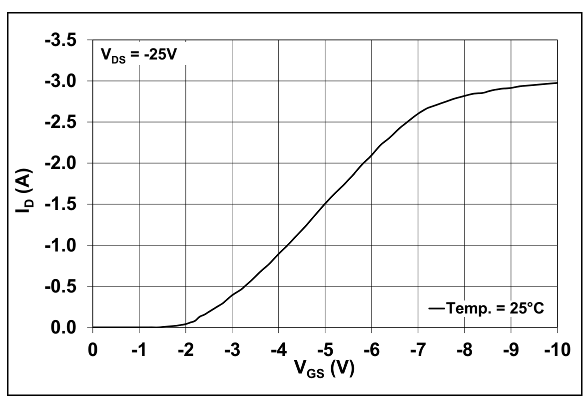


FIGURE 2-6: P-Channel I_D vs. V_{GS}.

Note: Unless otherwise indicated, $T_A = T_J = 25°C$.

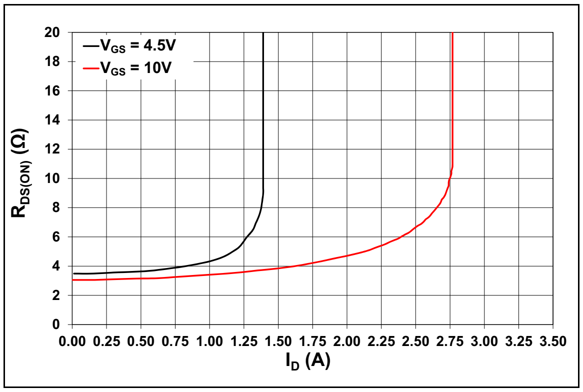


FIGURE 2-7: *N-Channel On-Resistance vs. Drain Current.*

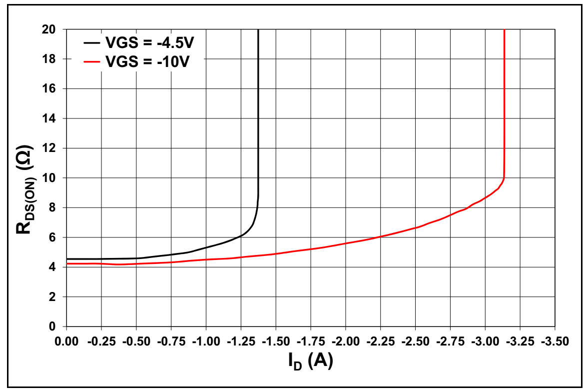


FIGURE 2-10: *P-Channel On-Resistance vs. Drain Current.*

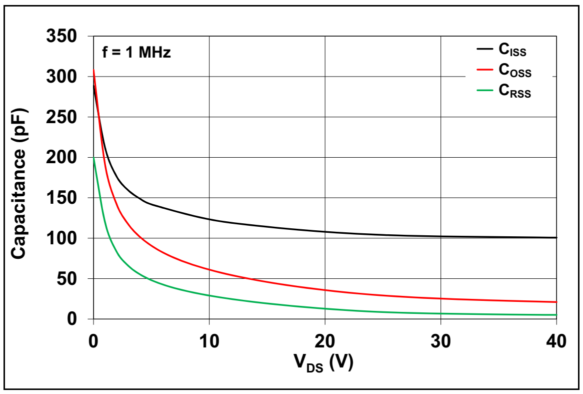


FIGURE 2-8: *N-Channel Capacitance vs. Drain-to-Source Voltage.*

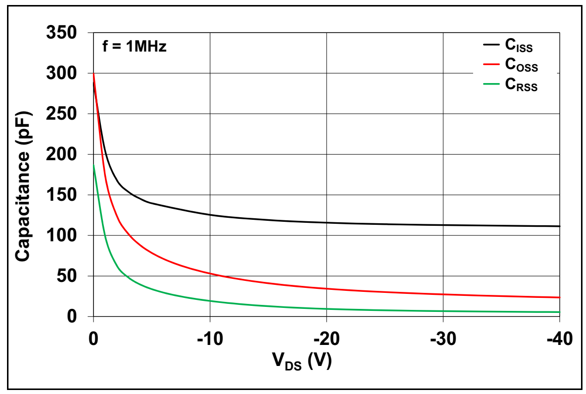


FIGURE 2-11: *P-Channel Capacitance vs. Drain-to-Source Voltage.*

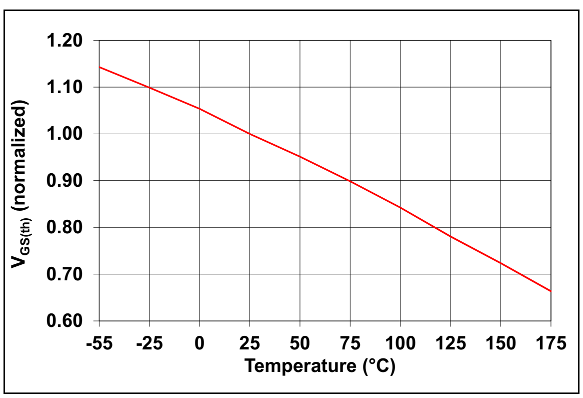


FIGURE 2-9: *N-Channel $V_{GS(th)}$ vs. Temperature.*

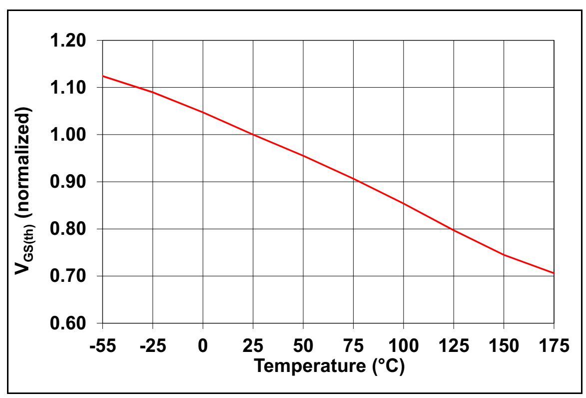


FIGURE 2-12: *P-Channel $V_{GS(th)}$ vs. Temperature.*

Note: Unless otherwise indicated, $T_A = T_J = 25°C$.

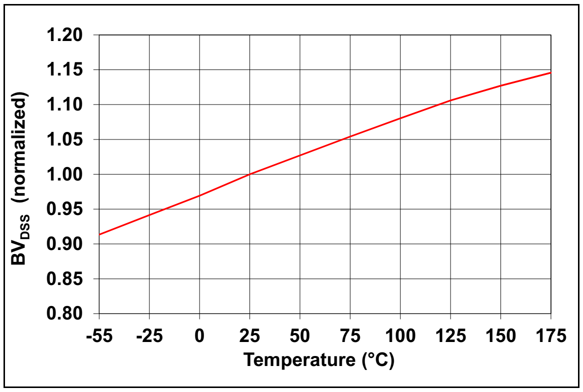


FIGURE 2-13: *N-Channel BV_{DSS} vs. Temperature.*

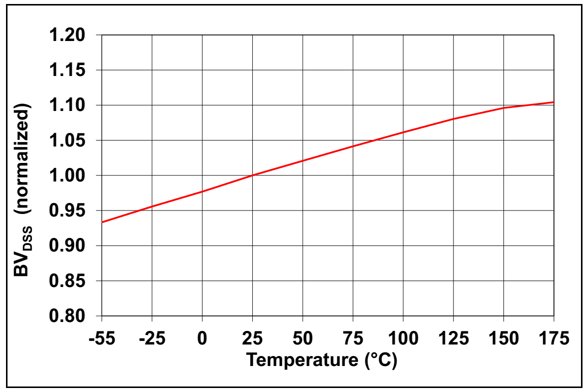


FIGURE 2-14: *P-Channel BV_{DSS} vs. Temperature.*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

TC6321 6x5 VDFN	**Name**	**Description**
1	SN	Source N-Channel
2	GN	Gate N-Channel
3	GP	Gate P-Channel
4	SP	Source P-Channel
5, 6	DP	Drain P-Channel
7, 8	DN	Drain N-Channel
9	DN	Drain N-Channel
10	DP	Drain P-Channel

4.0 FUNCTIONAL DESCRIPTION

4.1 N-Channel Switching Waveforms and Test Circuit

Figure 4-1 shows the N-channel switching waveforms and test circuit.

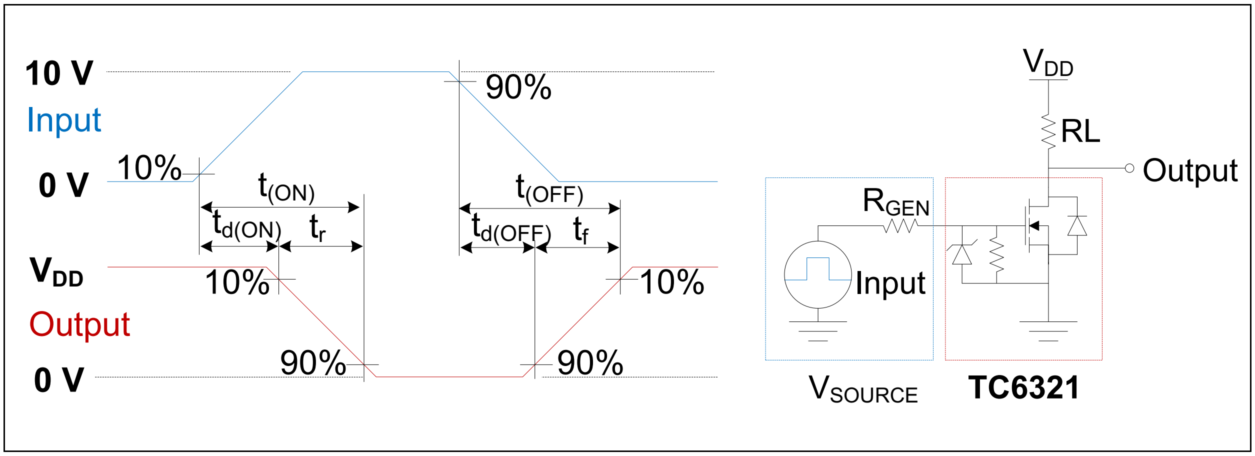


FIGURE 4-1: N-Channel Switching Waveforms and Test Circuit.

4.2 P-Channel Switching Waveforms and Test Circuit

Figure 4-2 shows the P-channel switching waveforms and test circuit.

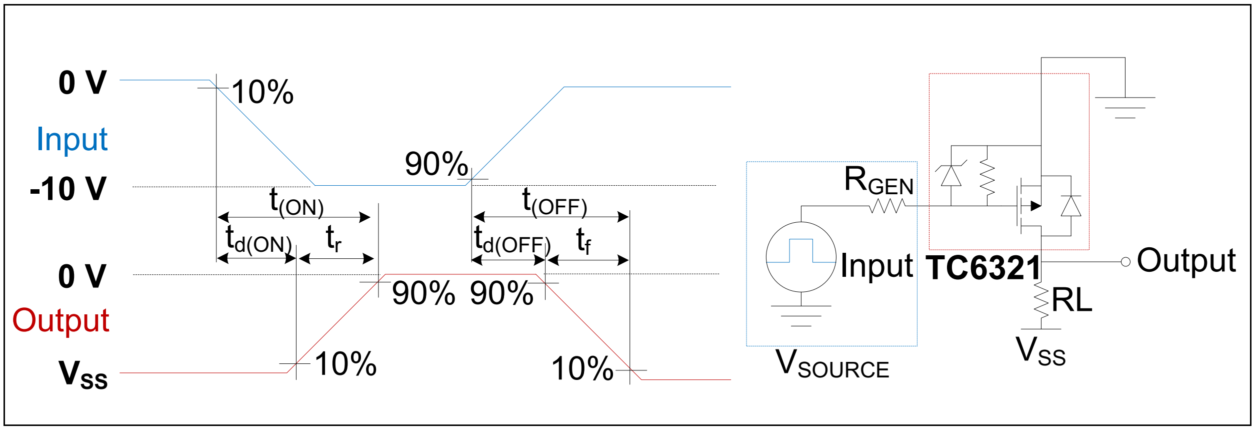


FIGURE 4-2: P-Channel Switching Waveforms and Test Circuit.

5.0 APPLICATION INFORMATION

The TC6321 N- and P-MOSFET pair is designed for a wide range of switching and amplifying applications where high-voltage, high-current drive, and fast switching speeds are required, especially for medical ultrasound applications.

A typical application pairs the TC6321 with any of MD12xx, MD17xx, or MD18xx ultrasound family MOSFET Drivers to form a high-speed and high-voltage (+/–100V 2.5A) pulser circuit. Figure 5-1 illustrates the application circuit digram for a two-level pulser.

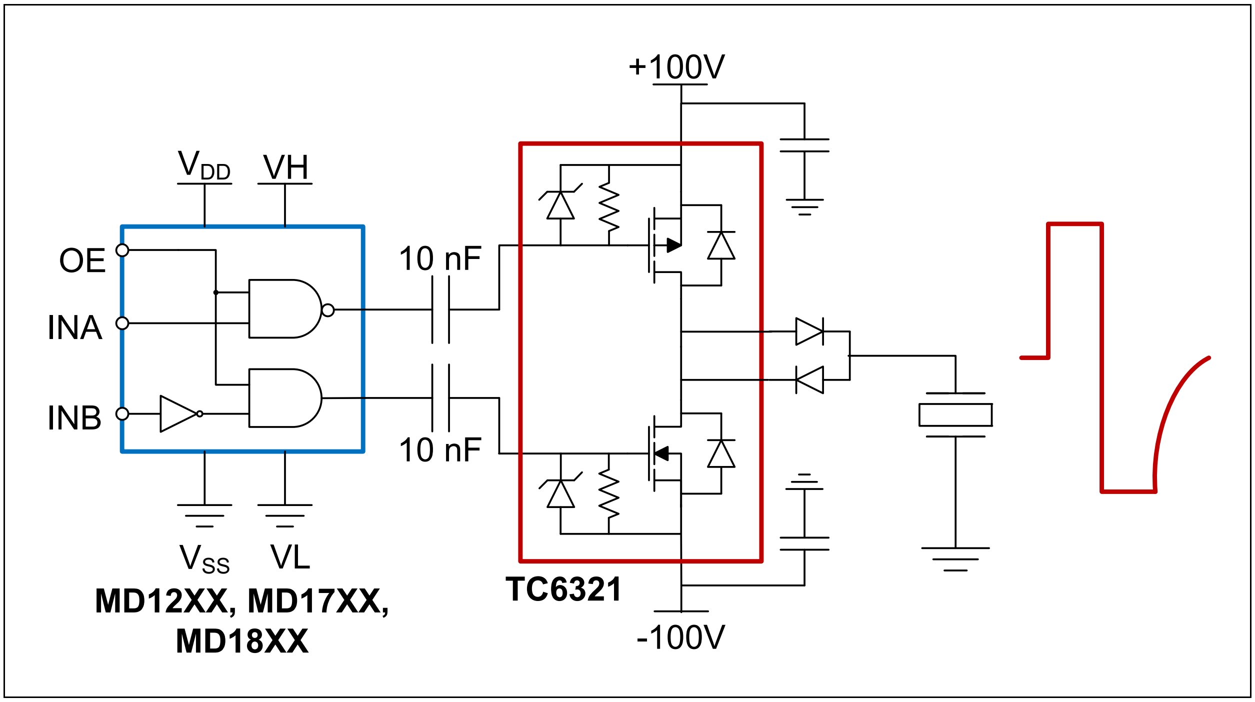


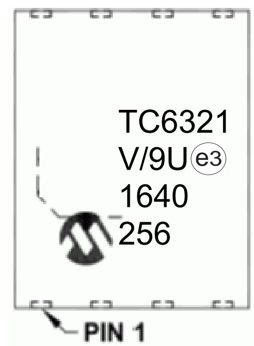
FIGURE 5-1: *TC6321 - Application Circuit Diagram.*

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

8-Lead VDFN (6 x 5 mm)

Example

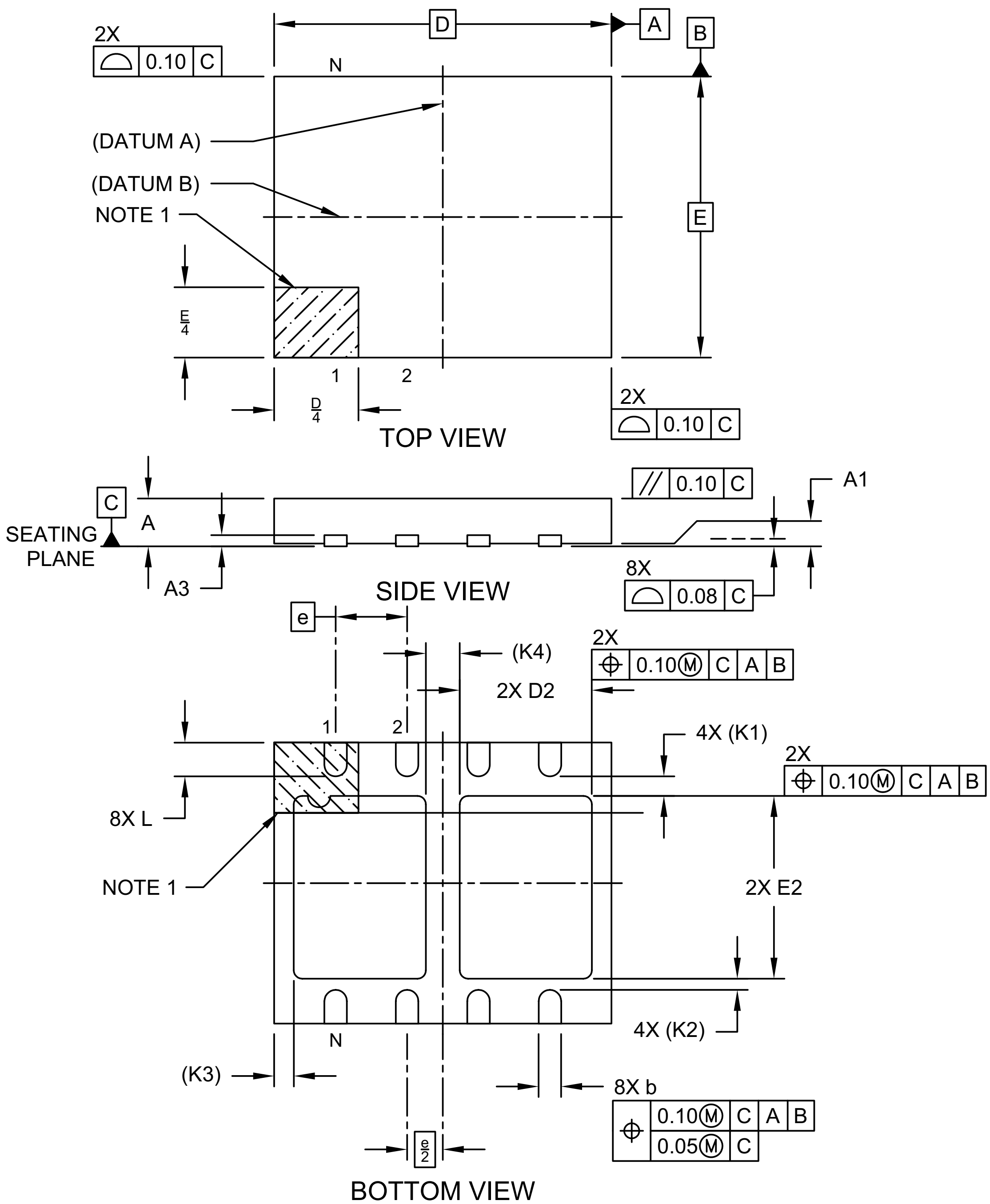


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Very Thin Plastic Dual Flat, No Lead (9U) - 6x5 mm Body [VDFN] With Dual Exposed Pads

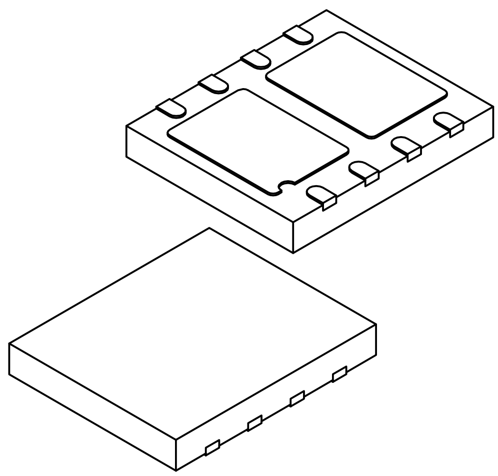
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-413A Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead (9U) - 6x5 mm Body [VDFN] With Dual Exposed Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length (X2)	D2	2.25	2.35	2.45
Overall Width	E		5.00 BSC	
Exposed Pad Width (X2)	E2	3.15	3.25	3.35
Terminal Width	b	0.35	0.40	0.45
Terminal Length	L	0.55	0.60	0.65
Terminal to Exposed Pad (X4)	K1		0.35 REF	
Terminal to Exposed Pad (X4)	K2		0.20 REF	
Molded Package Edge to Exposed Pad	K3		0.35 REF	
Exposed Pad to Exposed Pad	K4		0.60 REF	

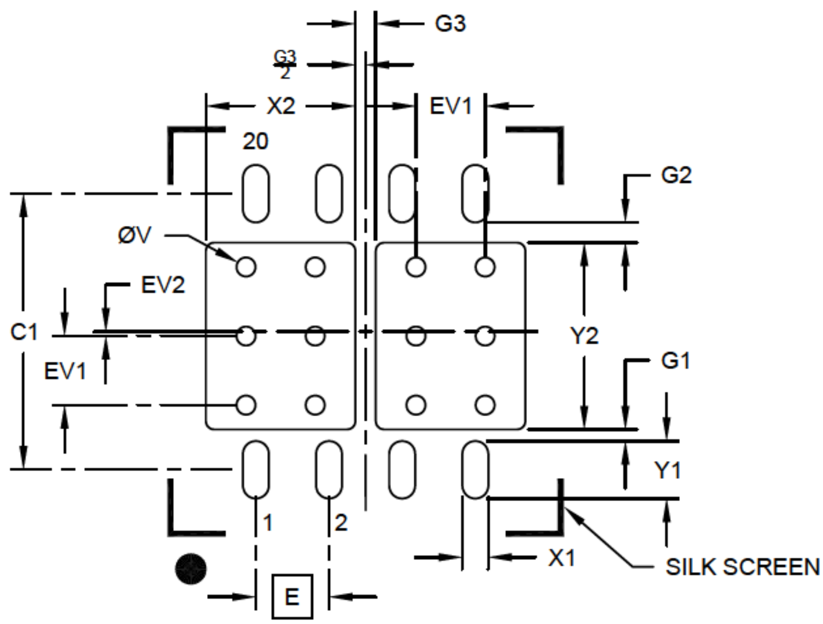
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-413A Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead (9U) - 6x5 mm Body [VDFN] With Dual Exposed Pads

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width (X2)	X2			2.60
Optional Center Pad Length	Y2			3.25
Contact Pad Spacing	C1		4.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X4)	G1	0.20		
Contact Pad to Center Pad (X4)	G2	0.35		
Center Pad to Center Pad	G3		0.35	
Thermal Via Diameter (X12)	V		0.33	
Thermal Via Pitch	EV1		1.20	
Thermal Via Offset	EV2		0.08	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2413A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (March 2018)

- Updated the Package Types illustration.
- Updated Table 3-1.

Revision A (March 2017)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, for example, on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X/	XX
Device	Temperature	Package

Device:	TC6321T:	N- and P-Channel Enhancement-Mode MOSFET Pair, Tape and Reel
Temperature:	V =	-55°C to +175°C (Various temperature levels) (1)
Package Type:	9U =	Very Thin Plastic Dual Flat, No Lead, VDFN, 8-Lead, 6x5 mm Body, with Dual Exposed Pads

Examples:

a) TC6321T-E/MQ: Tape and Reel,
Various temperature levels,
8-LD VDFN package

Note 1: Shipment of these devices may require an end-use/end-user certificate per SPI-43508.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV

ISO/TS 16949

Trademarks

ISBN: 978-1-5224-2784-1

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

10/25/17