R818 Datasheet

Audio Application Processor

Revision 1.5

Aug. 12, 2020

Revision History

Revision	Date	Description
1.5	Aug. 12, 2020	Updated the pin information of MICIN1/2 in Table 4-2 Pin Characteristics.
1.4	Jul. 29, 2020	Updated 5.12.1. Power-On Sequence.
1.3	Jul. 1, 2020	Updated the Ta and Tj values in Table 5-2 Recommended Operating Conditions.
1.2	Jun. 10, 2020	Removed GPU power, and modified the memory capacity of DDR.
1.1	Apr. 26, 2020	Removed TCON_TRIG signal in section 4.3 and 4.4.
1.0	Apr. 15, 2020	Initial version

Declaration

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About This Documentation

Purpose

The documentation describes features of each module, pin/signal characteristics, current consumption, the interface timing, thermal and package, and part reliability of the R818 processor. For details about register descriptions of each module, see the ***Allwinner_R818_User_Manual***.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 **WARNING**	A warning means that injury or death is possible if the instructions are not obeyed.
 **CAUTION**	A caution means that damage to equipment is possible.
 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency, data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

1. Overview

R818 is a high performance quad-core application processor for audio application markets. The application processor incorporates a high efficient 64-bit quad-core Cortex™-A53 processor, advanced Imagination PowerVR GE8300 GPU, 13M camera ISP, and high-definition 4K@30fps video decoder. An extensive set of audio interfaces such as audio codec, I2S/PCM, DMIC, one wire audio (OWA) are included for microphone voice wake-up/recognition/record/playback applications on connected audio products. Rich memory interfaces (DDR4, DDR3, DDR3L, LPDDR3, LPDDR4, eMMC, Nand) provide high flexibility to support variant memory configurations.

Lots of high-performance interfaces can get very flexible solution, such as MIPI CSI, MIPI DSI, EMAC, USB, UART, SPI, PWM, TWI, LEDC, etc. The Allwinner SDK features high stability and ease of use, supports rapid mass production.

2. Features

2.1. CPU Architecture

- Quad-core ARM Cortex™-A53 processor
- Power-efficient ARM v8 architecture
- 64-bit and 32-bit execution states for scalable high performance
- Trustzone technology supported
- Supports NEON Advanced SIMD(Single Instruction Multiple Data) instruction for acceleration of media and signal processing functions
- VFPv4 Floating Point Unit
- 32 KB L1 Instruction cache and 32 KB L1 Data cache for per CPU
- 512 KB L2 cache shared

2.2. GPU Architecture

- Imagination GE8300
- Supports OpenGL ES 1.1/2.0/3.2, Vulkan 1.1, OpenCL 1.2

2.3. Memory Subsystem

2.3.1. Boot ROM

- On-chip memory
- Supports system boot from the following devices:
  - SD/eMMC(SMHC0, SMHC2)
  - Nand Flash
  - SPI Nor Flash
  - SPI Nand Flash
- Supports secure boot and normal boot
- Supports mandatory upgrade process through SMHC0 and USB
- Supports GPIO pin to select the kind of boot media to boot
- Supports GPADC to select the kind of boot media to boot
- Supports SID(efuse) to select the kind of boot media to boot
- Secure brom supports load only certified firmware
- Secure brom ensures that the secure boot is a trusted environment

2.3.2. SDRAM

- 32-bit DDR4/DDR3/DDR3L/LPDDR3/LPDDR4 interface
- DDR4: clock frequency up to 792 MHz
- DDR3/DDR3L: clock frequency up to 792 MHz
- LPDDR3: clock frequency up to 792 MHz
- LRDDR4: clock frequency up to 792 MHz
- Memory capacity up to 4 GB

2.3.3. NAND Flash

- Compliant with ONFI 2.0 and Toggle 2.0

- Up to 80-bit ECC per 1024 bytes
- Supports 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports 2 chip selects, and 2 ready_busy signals
- Supports SLC/MLC flash and EF-NAND
- Supports SDR, ONFI DDR1.0, Toggle DDR1.0, ONFI DDR2.0 and Toggle DDR2.0 RAW NAND FLASH

2.3.4. SMHC

- Three SD/MMC host controller(SMHC) interfaces
- SMHC0 controls the devices that comply with the Secure Digital(SD3.0)
  - 4-bit bus width
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
  - DDR mode 100 MHz@1.8V IO pad
- SMHC1 controls the devices that comply with the Secure Digital Input/Output(SDIO3.0)
  - 4-bit bus width
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
  - DDR mode 100 MHz@1.8V IO pad
- SMHC2 controls the devices that comply with the Multimedia Card(eMMC 5.1)
  - 8-bit bus width
  - SDR mode 50 MHz@3.3V IO pad
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
  - DDR mode 100 MHz@1.8V IO pad
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.4. Video Engine

2.4.1. Video Decoder

- Supports multi-formats video decoder, including:
  - H.265 MP@L5.0: 4K@30fps
  - H.264 BP/MP/HP@L5.1: 4K@30fps
  - VP9: 720p@30fps
  - MPEG-4 SP/ASP: 1080p@60fps
  - MPEG-2 MP/HL: 1080p@60fps
  - MPEG-1 MP/HL: 1080p@60fps
  - VP8: 1080p@60fps
  - AVS/AVS+ JiZhun@L6.0: 1080p@60fps
  - H.263 BP: 1080p@60fps
  - MJPEG: 1080p@60fps
  - VC1 SP/MP/AP: 1080p@30fps

2.4.2. Video Encoder

- H.264 BP/MP/HP
- Maximum 16-megapixel(4096 x 4096) resolution for H.264 encoding
- H.264 encoding performance of 1080p@60fps
- MJPEG encoding performance of 1080p@30fps

2.5. Video and Graphics

2.5.1. Display Engine(DE)

- Output size up to 2048 x 2048
- Four alpha blending channels for main display, three channels for aux display
- Four overlay layers in each channel, and has an independent scaler
- Potter-duff compatible blending operation
- Input format: YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
  - Content adaptive backlight control
- Supports write back only for high efficient main display and miracast

2.5.2. Graphic 2D (G2D)

- Supports layer size up to 2048 x 2048 pixels
- Supports input/output formats: YUV422(semi-planar and planar format)/YUV420(semi-planar and planar format)/P010/P210/P410/Y8/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/ARGB2101010 and RGB565
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

2.6. System Peripherals

2.6.1. Timer

- The timer module implements the timing and counting functions, which includes Timer0, Timer1, Watchdog and AVS0, AVS1
- Timer0 and Timer1 for system scheduler counting
  - Configurable 8 prescale factors
  - Programmable 32-bit down timer
  - Supports two working modes: continue mode and single count mode
  - Generates an interrupt when the count is decreased to 0
- 1 Watchdog for transmitting a reset signal to reset the entire system after an exception occurs in the system
  - Supports 12 initial values to configure
  - Generation of timeout interrupts
  - Generation of reset signal
  - Watchdog restart the timing
- 2 AVS counters (AVS0 and AVS1) for synchronizing video and audio in the player
  - Programmable 33-bit up timer
  - Initial value can be updated anytime
  - 12-bit frequency divider factor
  - Pause/Start function

2.6.2. High Speed Timer

- One high speed timer with 56-bit counter
- Configurable 5 prescale factor
- Clock source is synchronized with AHB1 clock, much more accurate than other timers
- Supports 2 working modes: continuous mode and single mode
- Generates an interrupt when the count is decreased to 0

2.6.3. RTC

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Timer frequency: 1 kHz
- Configurable initial value by software anytime
- Periodically alarm to wake up the external devices
- Supports a calibration function of 32.768 kHz obtained by RC16M clock division
- Supports fanout function of internal 32K clock
- 8 general purpose registers for storing power-off information

2.6.4. GIC

- Supports 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 160 Shared Peripheral Interrupts(SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Interrupt masking and prioritization

2.6.5. DMA

- Up to 8-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- DMA channel supports pause function

2.6.6. CCU

- 12 PLLs
- One on-chip RC oscillator
- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.6.7. Thermal Sensor Controller

- Temperature accuracy: ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Three thermal sensors: sensor0 located in the CPU, sensor1 located in the GPU, and sensor2 located in the DDR

2.6.8. CPU Configuration

- Capable of CPU reset, including core reset, debug circuit reset, etc
- Capable of other CPU-related control, including interface control, CP15 control, and power on/off control
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc
- Including CPU debug control and status register

2.6.9. IOMMU

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE0, VE, CSI, ISP, G2D parallel address mapping
- Supports DE0, VE, CSI, ISP, G2D bypass function independently
- Supports DE0, VE, CSI, ISP, G2D prefetch independently
- Supports DE0, VE, CSI, ISP, G2D interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

2.6.10. Spinlock

- Provides a hardware synchronization mechanism in multi-core system
- Supports 32 lock units to prevent multi processors from handling the shared data at the same time
- Two kinds of lock status: locked and unlocked
- The lock time of the processor is less than 200 cycles

2.6.11. Message Box

- Provides interrupt communication mechanism for on-chip processor
- The communication parties transmit information by a channel
- Interrupt alarm function

2.7. Image Input

2.7.1. MIPI CSI

- Supports 2 MIPI CSI interfaces(one for 4-lane, the other for 2-lane)
- Supports image crop function
- Supports MIPI Version 1.0
- Supports 1.0 Gbps/lane
- Maximum video capture resolution up to 8M@30fps(for online mode) or 13M@10fps(for offline mode) or 4*1080p@25fps(for de-interleaver conversion chip)

2.7.2. ISP

- Supports one sensor in online mode, or two sensors in offline mode
- Maximum frame rate of 8M@30fps(for online mode) or 13M@10fps(for offline mode)
- Adjustable 3A functions, including automatic exposure(AE), automatic white balance(AWB) and automatic focus (AF)
- Highlight compensation, backlight compensation, gamma correction and color enhancement
- Defect pixel correction, 2D denoising
- Global tone mapping
- Graphics mirror and flip
- ISP tuning tools for the PC

2.8. Video Output

2.8.1. TCON_LCD

- RGB interface with DE/SYNC mode, up to 1920 x 1200@60fps
- Serial RGB/dummy RGB interface, up to 800 x 480@60fps
- LVDS interface with dual link, up to 1920 x 1200@60fps

- LVDS interface with single link, up to 1366 x 768@60fps
- i8080 interface, up to 800 x 480@60fps
- Supports BT656 interface for NTSC and PAL
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence

2.8.2. MIPI DSI

- One 4-lane MIPI DSI
- Compliance with MIPI DSI v1.01
- Compliance with MIPI DCS v1.01, bidirectional communication in LP through data lane 0
- Maximum performance up to 1920 x 1200@60fps
- Supports non-burst mode with sync pulse/sync event, burst mode and command mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports ULPS and escape modes
- Hardware checksum capabilities

2.9. Audio Subsystem

2.9.1. Audio Codec

- Two audio digital-to-analog(DAC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 95±3dB SNR
- Two audio analog-to-digital(ADC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 48 kHz ADC sample rate
  - 95±3dB SNR
- Two audio output interfaces:
  - One stereo headphone output (HPOUTL and HPOUTR)
  - One differential line output (LINEOUTLP and LINEOUTLN)
- Two audio input interfaces:
  - Two differential microphone inputs (MICIN1P/N and MICIN2P/N)
- Two low-noise analog microphone bias output
- Supports Dynamic Range Controller adjusting the DAC playback and ADC capture
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- DMA and Interrupt support

2.9.2. I2S/PCM

- Four I2S/PCM interfaces
- Supports Left-justified, Right-justified, Standard I2S mode, PCM mode, and TDM mode
- I2S mode supports 8 channels, and 32-bit/192kbit sample rate
- I2S and TDM modes support maximum 16 channels, and 32-bit/96kbit sample rate

2.9.3. DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

2.9.4. OWA

- One OWA TX
- Compliance with S/PDIF interface
- IEC-60958 transmitter functionality
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 128×24bits TXFIFO for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports 16-bit, 20-bit and 24-bit data formats

2.10. Security Engine

2.10.1. Crypto Engine(CE)

- Encryption and decryption algorithms implemented by using hardware, including AES, XTS-AES, DES, TDES, SM4
  - ECB, CBC, CTS, CTR, CFB, OFB, CBC-MAC, GCM mode for AES
  - 128/192/256-bit key for AES
  - 256-bit, 512-bit key for XTS-AES
  - ECB, CBC, CTR, CBC-MAC mode for DES
- Hash tamper proofing algorithms implemented by using hardware, including MD5, SHA, SM3, HMAC
  - SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
  - HMAC-SHA1, HMAC-SHA256 for HMAC
  - Supports hardware padding
  - Supports multi-package mode
- Signature and verification algorithms implemented by using hardware, including RSA, ECC
  - RSA supports 512/1024/2048/3072/4096-bit width
  - ECC supports 160/224/256/384/521-bit width
- Hardware random number generator: PRNG, TRNG, HASH+DRBG
- Security strategy and system feature
  - Symmetric, asymmetric, HASH/RBG control logics are separate, which can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time
  - Supports task chain mode for each request. Task or task chain are executed at request order
  - 8 scatter group(sg) are supported for both input and output data
  - Supports secure and non-secure interfaces respectively, each world issues task request through its own interface, they do not know the existence of each other
  - Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other

2.10.2. Security ID

- Supports 2 Kbits EFUSE for chip ID and security application
- EFUSE has secure zone and non-secure zone
- Supports a SRAM to backup fuse information

2.10.3. Secure Memory Control (SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Set secure area of DRAM
- Set secure property that Master accesses to DRAM
- Set DRM area
- Set whether DRM master can access to DRM area or not

2.10.4. Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Set secure property of peripherals

2.11. External Peripherals

2.11.1. USB

- One USB 2.0 OTG(USB0), with integrated USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) in host mode
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a for host mode
  - Up to 10 User-Configurable Endpoints (EPs) for Bulk, Isochronous and Interrupt bi-directional transfers
  - Supports (8 KB+64 Bytes) FIFO for all EPs (including EP0)
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- One USB 2.0 HOST(USB1), with integrated USB 2.0 analog PHY
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) device

2.11.2. EMAC

- One EMAC interface
- Compliant with IEEE 802.3-2002 standard
- Supports 10/100/1000 Mbit/s data transfer rates
- Supports RMII/RGMII PHY interface
- Supports both full-duplex and half-duplex operation
- Supports MDIO
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- 2 KB TXFIFO for transmission packets and 8 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

2.11.3. UART

- Up to 6 UART controllers(UART0, UART1, UART2, UART3, UART4, S_UART)
- UART0: 2-wire; UART1, UART2, UART3, UART4: 4-wire
- Compatible with industry-standard 16550 UARTs
- Capable of speed up to 4 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

2.11.4. SPI

- Up to 3 SPI controllers(SPI0, SPI1, SPI2)
- Full-duplex synchronous serial interface
- Master/slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64 bytes FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
- Interrupt or DMA support
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 1-bit to 32-bit
- Supports Standard SPI, Dual-Output/Dual-Input SPI, Dual IO SPI, Quad-Output/Quad-Input SPI

2.11.5. Two Wire Interface (TWI)

- Up to 6 TWI controllers(TWI0, TWI1, TWI2, TWI3, S_TWI0, S_TWI1)
- Software-programmable for slave or master
- Supports repeated START signal
- Multi-master system supported
- Allows 10-bit addressing transactions
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports Standard mode(up to 100 kbit/s) and Fast mode(up to 400 kbit/s)
- Allows operation from a wide range of input clock frequency
- TWI driver supports packet transmission and DMA when TWI works in Master mode

2.11.6. PWM

- 5 PWM channels(PWM0~3, S_PWM)
- PWM0~3 channels divide to 2 PWM pairs: PWM01 pair, PWM23 pair
- S_PWM channel has the single channel characteristics of PWM module, and has no pair function
- Supports pulse, cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveforms: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0~24 MHz/100 MHz
- Various duty-cycle: 0%~100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input
- Supports PWM group mode(4 groups), the starting phase of each channel in same group is configurable

2.11.7. Low Rate ADC (LRADC)

- One LRADC input channel
- 6-bit resolution
- Sample rate up to 2 kHz
- Supports hold Key and general Key
- Supports normal, continue and single work mode
- Power supply voltage: 1.8 V, power reference voltage: 1.35 V, analog input and detected voltage range: 0~LEVELB (the maximum value is 1.266 V)

2.11.8. General Purpose ADC (GPADC)

- One GPADC input channel
- 12-bit resolution and 8-bit effective SAR type A/D converter
- Power supply voltage: 1.8 V, analog input range: 0 to 1.8 V
- Maximum sampling frequency: 1 MHz
- Support three operation modes
  - Single conversion mode
  - Continuous conversion mode
  - Outbreak conversion mode

2.11.9. LEDC

- LEDC is used to control the external intelligent control LED lamp
- Configurable input high/low level width of LED
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configurable mode
- Maximum 1024 LEDs serial connect

2.11.10. CIR Transmitter (CIR_TX)

- Supports arbitrary wave generator
- Configurable carrier frequency
- Supports DMA shake and wait mode
- 128 bytes FIFO for data buffer

2.11.11. CIR Receiver (CIR_RX)

- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.12. Package

- LFBGA346 balls, 0.5 mm ball pitch, 0.3 mm ball size, 12 mm x 12 mm body

3. Block Diagram

Figure 3-1 shows the system block diagram of the R818.

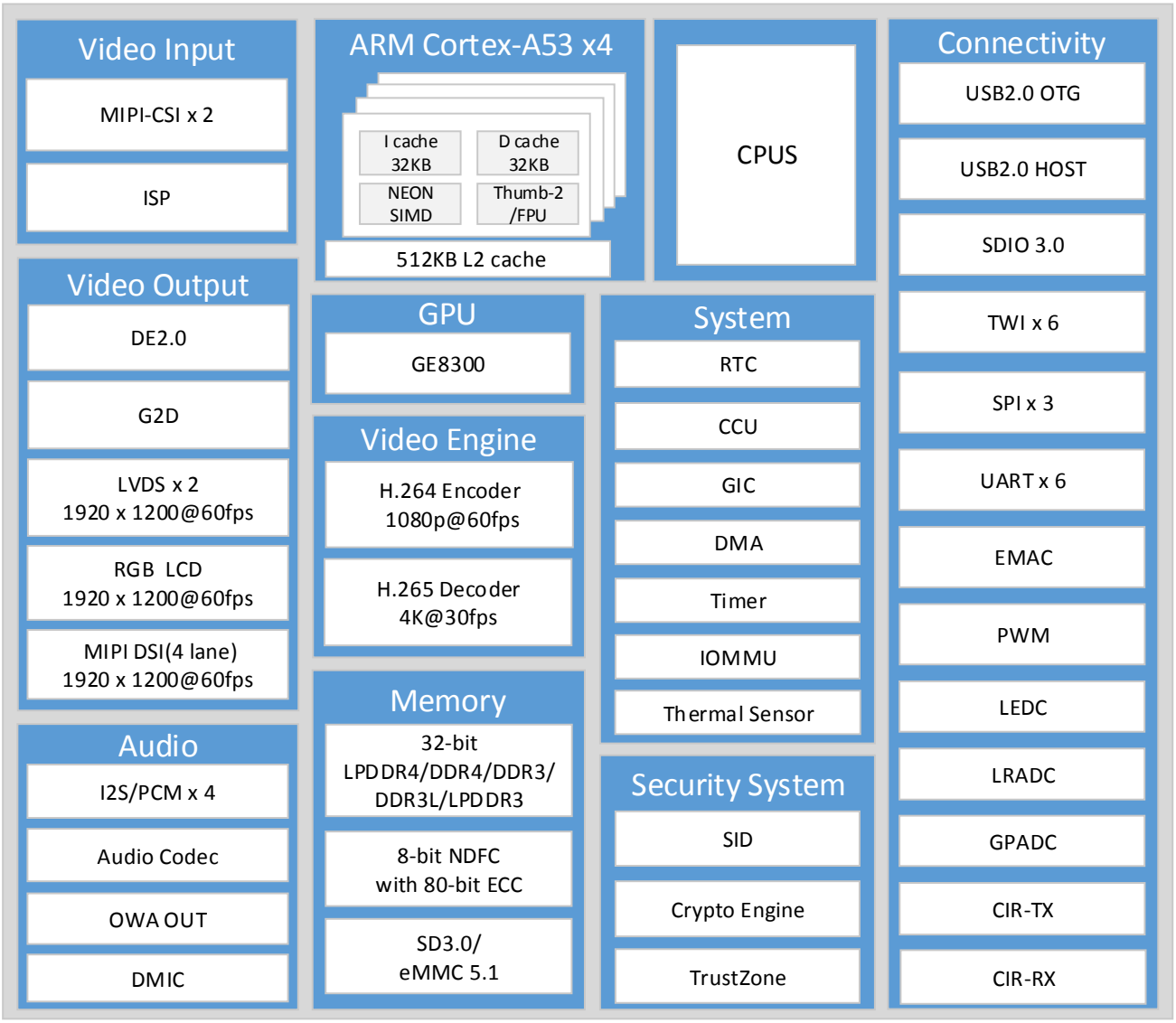


Figure 3-1. R818 System Block Diagram

4. Pin Description

4.1. Pin Quantity

Table 4-1 lists the pin quantity of the R818.

Table 4-1. Pin Quantity

Pin Type	Quantity
I/O	243
Power	31
Ground	65
DDR Power	7
Total	346

4.2. Pin Characteristics

Table 4-2 lists the characteristics of the R818 pins from the following seven aspects.

[1].Ball#: Package ball numbers associated with each signals.

[2].Pin Name: The name of the package pin.

[3].Type: Denotes the signal direction

I (Input),
O (Output),
I/O (Input/Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output),
P (Power),
G (Ground)

[4].Ball Reset State: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5].Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled by software.

[6].Default Buffer Strength: Defines default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6mA.

[7].Power Supply: The voltage supply for the terminal's IO buffers.

Table 4-2. Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
SDRAM						
AA17	SA0	O	Z	NA	NA	VCC_DRAM
AB13	SA1	O	Z	NA	NA	VCC_DRAM
AA12	SA2	O	Z	NA	NA	VCC_DRAM
U15	SA3	O	Z	NA	NA	VCC_DRAM
U13	SA4	O	Z	NA	NA	VCC_DRAM
W13	SA5	O	Z	NA	NA	VCC_DRAM
Y13	SA6	O	Z	NA	NA	VCC_DRAM
W17	SA7	O	Z	NA	NA	VCC_DRAM
AB18	SA8	O	Z	NA	NA	VCC_DRAM

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
AA19	SA9	O	Z	NA	NA	VCC_DRAM
AC17	SA10	O	Z	NA	NA	VCC_DRAM
AC19	SA11	O	Z	NA	NA	VCC_DRAM
Y17	SA12	O	Z	NA	NA	VCC_DRAM
AB16	SA13	O	Z	NA	NA	VCC_DRAM
AC13	SA14	O	Z	NA	NA	VCC_DRAM
AB12	SA15	O	Z	NA	NA	VCC_DRAM
AB15	SA16	O	Z	NA	NA	VCC_DRAM
Y7	SDQ0	I/O	Z	NA	NA	VCC_DRAM
V7	SDQ1	I/O	Z	NA	NA	VCC_DRAM
Y5	SDQ2	I/O	Z	NA	NA	VCC_DRAM
W7	SDQ3	I/O	Z	NA	NA	VCC_DRAM
W1	SDQ4	I/O	Z	NA	NA	VCC_DRAM
W4	SDQ5	I/O	Z	NA	NA	VCC_DRAM
W2	SDQ6	I/O	Z	NA	NA	VCC_DRAM
W3	SDQ7	I/O	Z	NA	NA	VCC_DRAM
AA1	SDQ8	I/O	Z	NA	NA	VCC_DRAM
AB4	SDQ9	I/O	Z	NA	NA	VCC_DRAM
AB1	SDQ10	I/O	Z	NA	NA	VCC_DRAM
AB3	SDQ11	I/O	Z	NA	NA	VCC_DRAM
AC3	SDQ12	I/O	Z	NA	NA	VCC_DRAM
AA4	SDQ13	I/O	Z	NA	NA	VCC_DRAM
AA3	SDQ14	I/O	Z	NA	NA	VCC_DRAM
AA2	SDQ15	I/O	Z	NA	NA	VCC_DRAM
AC9	SDQ16	I/O	Z	NA	NA	VCC_DRAM
AB9	SDQ17	I/O	Z	NA	NA	VCC_DRAM
AA8	SDQ18	I/O	Z	NA	NA	VCC_DRAM
AB8	SDQ19	I/O	Z	NA	NA	VCC_DRAM
AC5	SDQ20	I/O	Z	NA	NA	VCC_DRAM
AB5	SDQ21	I/O	Z	NA	NA	VCC_DRAM
AA6	SDQ22	I/O	Z	NA	NA	VCC_DRAM
AB6	SDQ23	I/O	Z	NA	NA	VCC_DRAM
Y11	SDQ24	I/O	Z	NA	NA	VCC_DRAM
W9	SDQ25	I/O	Z	NA	NA	VCC_DRAM
V9	SDQ26	I/O	Z	NA	NA	VCC_DRAM
Y9	SDQ27	I/O	Z	NA	NA	VCC_DRAM
AC11	SDQ28	I/O	Z	NA	NA	VCC_DRAM
W11	SDQ29	I/O	Z	NA	NA	VCC_DRAM
AB11	SDQ30	I/O	Z	NA	NA	VCC_DRAM
V11	SDQ31	I/O	Z	NA	NA	VCC_DRAM
U7	SDQM0	O	Z	NA	NA	VCC_DRAM
AA5	SDQM1	O	Z	NA	NA	VCC_DRAM
AA9	SDQM2	O	Z	NA	NA	VCC_DRAM

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
U11	SDQM3	O	Z	NA	NA	VCC_DRAM
Y2	SDQS0P	I/O	Z	NA	NA	VCC_DRAM
AB2	SDQS1P	I/O	Z	NA	NA	VCC_DRAM
AB7	SDQS2P	I/O	Z	NA	NA	VCC_DRAM
AB10	SDQS3P	I/O	Z	NA	NA	VCC_DRAM
Y3	SDQS0N	I/O	Z	NA	NA	VCC_DRAM
AC2	SDQS1N	I/O	Z	NA	NA	VCC_DRAM
AC7	SDQS2N	I/O	Z	NA	NA	VCC_DRAM
AA10	SDQS3N	I/O	Z	NA	NA	VCC_DRAM
AA20	SACT	O	Z	NA	NA	VCC_DRAM
W15	SBA0	O	Z	NA	NA	VCC_DRAM
Y15	SBA1	O	Z	NA	NA	VCC_DRAM
AB17	SBG0	O	Z	NA	NA	VCC_DRAM
AB20	SBG1	O	Z	NA	NA	VCC_DRAM
AA14	SCKP	O	Z	NA	NA	VCC_DRAM
AB14	SCKN	O	Z	NA	NA	VCC_DRAM
AA16	SCKE0	O	Z	NA	NA	VCC_DRAM
AA15	SCKE1	O	Z	NA	NA	VCC_DRAM
AC15	SCS0	O	Z	NA	NA	VCC_DRAM
AB19	SCS1	O	Z	NA	NA	VCC_DRAM
AA21	SODT0	O	Z	NA	NA	VCC_DRAM
AC21	SODT1	O	Z	NA	NA	VCC_DRAM
U17	SRST	O	Z	NA	NA	VCC_DRAM
Y19	SZQ	AI	Z	NA	NA	VCC_DRAM
R9, R10, R11, R12, R13, R14	VCC_DRAM	P	NA	NA	NA	NA
R15	VDD18_DRAM	P	NA	NA	NA	NA
GPIOB						
E5	PB0	I/O	Z	PU/PD	4	VCC_IO
D4	PB1	I/O	Z	PU/PD	4	VCC_IO
G4	PB2	I/O	Z	PU/PD	4	VCC_IO
D5	PB3	I/O	Z	PU/PD	4	VCC_IO
D3	PB4	I/O	Z	PU/PD	4	VCC_IO
D2	PB5	I/O	Z	PU/PD	4	VCC_IO
E3	PB6	I/O	Z	PU/PD	4	VCC_IO
E2	PB7	I/O	Z	PU/PD	4	VCC_IO
E1	PB8	I/O	Z	PU/PD	4	VCC_IO
F2	PB9	I/O	Z	PU/PD	4	VCC_IO
F3	PB10	I/O	Z	PU/PD	4	VCC_IO
GPIOC						
N19	PC0	I/O	Z	PU/PD	4	VCC_PC
P22	PC1	I/O	Z	PU/PD	4	VCC_PC
M21	PC2	I/O	Z	PU/PD	4	VCC_PC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
M22	PC3	I/O	PU	PU/PD	4	VCC_PC
L23	PC4	I/O	PU	PU/PD	4	VCC_PC
N23	PC5	I/O	Z	PU/PD	4	VCC_PC
L22	PC6	I/O	PU	PU/PD	4	VCC_PC
N20	PC7	I/O	PU	PU/PD	4	VCC_PC
P21	PC8	I/O	Z	PU/PD	4	VCC_PC
N21	PC9	I/O	Z	PU/PD	4	VCC_PC
K22	PC10	I/O	Z	PU/PD	4	VCC_PC
J22	PC11	I/O	Z	PU/PD	4	VCC_PC
L19	PC12	I/O	Z	PU/PD	4	VCC_PC
L21	PC13	I/O	Z	PU/PD	4	VCC_PC
K21	PC14	I/O	Z	PU/PD	4	VCC_PC
J23	PC15	I/O	Z	PU/PD	4	VCC_PC
L20	PC16	I/O	Z	PU/PD	4	VCC_PC
L18	VCC_PC	P	NA	NA	NA	NA
GPIOD						
V22	PD0	I/O	Z	PU/PD	4	VCC_PD
V23	PD1	I/O	Z	PU/PD	4	VCC_PD
W22	PD2	I/O	Z	PU/PD	4	VCC_PD
W23	PD3	I/O	Z	PU/PD	4	VCC_PD
AA22	PD4	I/O	Z	PU/PD	4	VCC_PD
AA23	PD5	I/O	Z	PU/PD	4	VCC_PD
Y22	PD6	I/O	Z	PU/PD	4	VCC_PD
Y23	PD7	I/O	Z	PU/PD	4	VCC_PD
AB22	PD8	I/O	Z	PU/PD	4	VCC_PD
AB23	PD9	I/O	Z	PU/PD	4	VCC_PD
R22	PD10	I/O	Z	PU/PD	4	VCC_PD
R23	PD11	I/O	Z	PU/PD	4	VCC_PD
T21	PD12	I/O	Z	PU/PD	4	VCC_PD
T22	PD13	I/O	Z	PU/PD	4	VCC_PD
U22	PD14	I/O	Z	PU/PD	4	VCC_PD
U23	PD15	I/O	Z	PU/PD	4	VCC_PD
U21	PD16	I/O	Z	PU/PD	4	VCC_PD
U20	PD17	I/O	Z	PU/PD	4	VCC_PD
W21	PD18	I/O	Z	PU/PD	4	VCC_PD
W20	PD19	I/O	Z	PU/PD	4	VCC_PD
U19	PD20	I/O	Z	PU/PD	4	VCC_PD
U18	PD21	I/O	Z	PU/PD	4	VCC_PD
R20	PD22	I/O	Z	PU/PD	4	VCC_PD
R19	PD23	I/O	Z	PU/PD	4	VCC_PD
N18	VCC_LVDS0	P	NA	NA	NA	NA
R18	VCC_PD	P	NA	NA	NA	NA
GPIOE						

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
E23	PE0	I/O	Z	PU/PD	4	VCC_PE
E20	PE1	I/O	Z	PU/PD	4	VCC_PE
G20	PE2	I/O	Z	PU/PD	4	VCC_PE
D19	PE3	I/O	Z	PU/PD	4	VCC_PE
G21	PE4	I/O	Z	PU/PD	4	VCC_PE
G19	PE5	I/O	Z	PU/PD	4	VCC_PE
F22	PE6	I/O	Z	PU/PD	4	VCC_PE
E22	PE7	I/O	Z	PU/PD	4	VCC_PE
F23	PE8	I/O	Z	PU/PD	4	VCC_PE
E21	PE9	I/O	Z	PU/PD	4	VCC_PE
E17	VCC_PE	P	NA	NA	NA	NA
GPIOF						
B10	PF0	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
C9	PF1	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
A9	PF2	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
B9	PF3	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
B8	PF4	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
C8	PF5	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
C10	PF6	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
GPIOG						
J2	PG0	I/O	Z	PU/PD	4	VCC_PG
H2	PG1	I/O	PU	PU/PD	4	VCC_PG
G1	PG2	I/O	PU	PU/PD	4	VCC_PG
G3	PG3	I/O	PU	PU/PD	4	VCC_PG
G2	PG4	I/O	PU	PU/PD	4	VCC_PG
H3	PG5	I/O	PU	PU/PD	4	VCC_PG
K2	PG6	I/O	Z	PU/PD	4	VCC_PG
J5	PG7	I/O	Z	PU/PD	4	VCC_PG
K3	PG8	I/O	Z	PU/PD	4	VCC_PG
L3	PG9	I/O	Z	PU/PD	4	VCC_PG
J1	PG10	I/O	Z	PU/PD	4	VCC_PG
G5	PG11	I/O	Z	PU/PD	4	VCC_PG
G6	PG12	I/O	Z	PU/PD	4	VCC_PG
J4	PG13	I/O	Z	PU/PD	4	VCC_PG
J6	VCC_PG	P	NA	NA	NA	NA
GPIOH						
C7	PH0	I/O	Z	PU/PD	4	VCC_IO
A5	PH1	I/O	Z	PU/PD	4	VCC_IO

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
B6	PH2	I/O	Z	PU/PD	4	VCC_IO
B5	PH3	I/O	Z	PU/PD	4	VCC_IO
C6	PH4	I/O	Z	PU/PD	4	VCC_IO
C5	PH5	I/O	Z	PU/PD	4	VCC_IO
F9	PH6	I/O	Z	PU/PD	4	VCC_IO
C4	PH7	I/O	Z	PU/PD	4	VCC_IO
E9	PH8	I/O	Z	PU/PD	4	VCC_IO
D9	PH9	I/O	Z	PU/PD	4	VCC_IO
B4	PH10	I/O	Z	PU/PD	4	VCC_IO
D7	PH11	I/O	Z	PU/PD	4	VCC_IO
A3	PH12	I/O	Z	PU/PD	4	VCC_IO
B2	PH13	I/O	Z	PU/PD	4	VCC_IO
C1	PH14	I/O	Z	PU/PD	4	VCC_IO
B3	PH15	I/O	Z	PU/PD	4	VCC_IO
C3	PH16	I/O	Z	PU/PD	4	VCC_IO
A2	PH17	I/O	Z	PU/PD	4	VCC_IO
C2	PH18	I/O	Z	PU/PD	4	VCC_IO
B1	PH19	I/O	Z	PU/PD	4	VCC_IO
GPIOL						
N5	PL0	I/O	PU	PU/PD	4	VCC_PL
L6	PL1	I/O	PU	PU/PD	4	VCC_PL
P3	PL2	I/O	Z	PU/PD	4	VCC_PL
N1	PL3	I/O	Z	PU/PD	4	VCC_PL
R4	PL4	I/O	Z	PU/PD	4	VCC_PL
N3	PL5	I/O	Z	PU/PD	4	VCC_PL
N2	PL6	I/O	Z	PU/PD	4	VCC_PL
L2	PL7	I/O	Z	PU/PD	4	VCC_PL
L1	PL8	I/O	Z	PU/PD	4	VCC_PL
M3	PL9	I/O	Z	PU/PD	4	VCC_PL
U4	PL10	I/O	Z	PU/PD	4	VCC_PL
M2	PL11	I/O	Z	PU/PD	4	VCC_PL
L4	VCC_PL	P	NA	NA	NA	NA
System						
R5	NMI	I/O,OD	No Pull	PU/PD	NA	VCC_RTC
A7	FEL	I	PU	PU/PD	NA	VCC_IO
F11	BOOT_SEL	I	PU	PU/PD	NA	VCC_IO
B7	JTAG_SEL	I	PU	PU/PD	NA	VCC_IO
R6	RESET	I/O	No Pull	PU/PD	NA	VCC_PLL
GPADC						
A11	GPADC1	AI	NA	NA	NA	AVCC
B11	BOOT_SEL_ADC	AI	NA	NA	NA	AVCC
LRADC						
E11	LRADC	AI	NA	NA	NA	AVCC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
USB						
G22	USB0_DM	A I/O	NA	NA	NA	VCC_USB
G23	USB0_DP	A I/O	NA	NA	NA	VCC_USB
H22	USB1_DM	A I/O	NA	NA	NA	VCC_USB
H23	USB1_DP	A I/O	NA	NA	NA	VCC_USB
J20	VCC_USB	P	NA	NA	NA	NA
J18	VDD_USB	P	NA	NA	NA	NA
MIPI CSI						
A22	MCSIA_CKN	AI	NA	NA	NA	VCC_MCSI
A21	MCSIA_CKP	AI	NA	NA	NA	VCC_MCSI
D21	MCSIA_D0N	AI	NA	NA	NA	VCC_MCSI
D22	MCSIA_D0P	AI	NA	NA	NA	VCC_MCSI
C22	MCSIA_D1N	AI	NA	NA	NA	VCC_MCSI
C23	MCSIA_D1P	AI	NA	NA	NA	VCC_MCSI
B21	MCSIA_D2N	AI	NA	NA	NA	VCC_MCSI
C21	MCSIA_D2P	AI	NA	NA	NA	VCC_MCSI
B22	MCSIA_D3N	AI	NA	NA	NA	VCC_MCSI
B23	MCSIA_D3P	AI	NA	NA	NA	VCC_MCSI
A19	MCSIB_CKN	AI	NA	NA	NA	VCC_MCSI
B19	MCSIB_CKP	AI	NA	NA	NA	VCC_MCSI
B20	MCSIB_D0N	AI	NA	NA	NA	VCC_MCSI
C20	MCSIB_D0P	AI	NA	NA	NA	VCC_MCSI
B18	MCSIB_D1N	AI	NA	NA	NA	VCC_MCSI
C18	MCSIB_D1P	AI	NA	NA	NA	VCC_MCSI
D17	VCC_MCSI	P	NA	NA	NA	NA
Audio Codec						
D11	AGND	G	NA	NA	NA	NA
F13	VRA1	AO	NA	NA	NA	AVCC
E13	VRA2	AO	NA	NA	NA	AVCC
D13	AVCC	P	NA	NA	NA	NA
D15	VEE	P	NA	NA	NA	CPVIN
C15	CPVDD	P	NA	NA	NA	CPVIN
E15	CPVEE	P	NA	NA	NA	CPVIN
C13	CPVIN	P	NA	NA	NA	NA
B15	MBIAS	AO	NA	NA	NA	VCC_IO
B16	HBIAS	AO	NA	NA	NA	VCC_IO
C11	HP_DET	AI	NA	NA	NA	AVCC
B17	HPOUTFB	AO	NA	NA	NA	CPVIN
A17	HPOUTL	AO	NA	NA	NA	CPVIN
A16	HPOUTR	AO	NA	NA	NA	CPVIN
B14	LINEOUTLN	AO	NA	NA	NA	AVCC
A14	LINEOUTLP	AO	NA	NA	NA	AVCC
A15	MIC_DET	AI	NA	NA	NA	AVCC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
A13	MICIN1P	AI	NA	NA	NA	AVCC
B13	MICIN1N	AI	NA	NA	NA	AVCC
A12	MICIN2P	AI	NA	NA	NA	AVCC
B12	MICIN2N	AI	NA	NA	NA	AVCC
RTC						
T2	X32KIN	AI	NA	NA	NA	VCC_RTC
T3	X32KOUT	AO	NA	NA	NA	VCC_RTC
U3	X32KFOUT	AO,OD	NA	NA	NA	VCC_PL, or VDD_CPUS
P2	RTC_VIO	AO	NA	NA	NA	VCC_RTC
L5	VCC_RTC	P	NA	NA	NA	NA
DCXO						
R2	DXIN	AI	NA	NA	NA	VCC_RTC
R1	DXOUT	AO	NA	NA	NA	VCC_RTC
U1	DXLDO_OUT	AO	NA	NA	NA	VCC_RTC
R3	REFCLK_OUT	AO	NA	NA	NA	VCC_RTC
U2	WREQIN	I	NA	NA	NA	VCC_PG
Power						
J19	VCC_EFUSE	P	NA	NA	NA	NA
E7	VCC_IO	P	NA	NA	NA	NA
K8, K9, L8, M8, N8	VDD_CPU	P	NA	NA	NA	NA
P8	VDD_CPUFB	P	NA	NA	NA	NA
N4	VDD_CPUS	P	NA	NA	NA	NA
H12	VDD_SYSFB	P	NA	NA	NA	NA
H13,H14,H15, H16,J16	VDD_SYS	P	NA	NA	NA	NA
N6	VCC_PLL	P	NA	NA	NA	NA
Ground						
A1,A23,AA11, AA13,AA18, AA7,AC1,AC22, AC23,C17,C19, H10,H11,H8, H9,J10,J15,J21, J3,J8,J9,K10, K11,K12,K13, K14,K15,K16, L10,L14,L15, L16,L9,M10, M11,M12,M13 ,M14,M15, M16,M9,N15, N16,N22,N9, P10,P11,P12, P13,P14,P15, P16,P9,R16, R21,R8,U5,U9,	GND	G	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
V13,V15,V17, V2,V3,Y4						

For details about schematic diagram and PCB design recommendations, see the ***Allwinner R818 Hardware Design Guide***.

4.3. GPIO Multiplex Function

The following table provides a description of the R818 GPIO multiplex function.

NOTE

For each GPIO, Function0 is input function; Function1 is output function.

Table 4-3. GPIO Multiplex Function

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6
PB0	GPIOB	I/O	UART2_TX	SPI2_CS	JTAG_MS		PB_EINT0
PB1		I/O	UART2_RX	SPI2_CLK	JTAG_CK		PB_EINT1
PB2		I/O	UART2_RTS	SPI2_MOSI	JTAG_DO		PB_EINT2
PB3		I/O	UART2_CTS	SPI2_MISO	JTAG_DI		PB_EINT3
PB4		I/O	TWI1_SCK	I2S0_MCLK	JTAG_MS_GPU		PB_EINT4
PB5		I/O	TWI1_SDA	I2S0_BCLK	JTAG_CK_GPU		PB_EINT5
PB6		I/O		I2S0_LRCK	JTAG_DO_GPU		PB_EINT6
PB7		I/O		I2S0_DOUT0	I2S0_DIN1		PB_EINT7
PB8		I/O	OWA_OUT	I2S0_DIN0	I2S0_DOUT1		PB_EINT8
PB9		I/O	UART0_TX	TWI0_SCK	JTAG_DI_GPU		PB_EINT9
PB10		I/O	UART0_RX	TWI0_SDA	PWM1		PB_EINT10
PC0	GPIOC	I/O	NAND_WE	SDC2_DS			PC_EINT0
PC1		I/O	NAND_ALE	SDC2_RST			PC_EINT1
PC2		I/O	NAND_CLE		SPI0_MOSI		PC_EINT2
PC3		I/O	NAND_CE1		SPI0_CS0		PC_EINT3
PC4		I/O	NAND_CE0		SPI0_MISO		PC_EINT4
PC5		I/O	NAND_RE	SDC2_CLK			PC_EINT5
PC6		I/O	NAND_RB0	SDC2_CMD			PC_EINT6
PC7		I/O	NAND_RB1		SPI0_CS1		PC_EINT7
PC8		I/O	NAND_DQ7	SDC2_D3			PC_EINT8
PC9		I/O	NAND_DQ6	SDC2_D4			PC_EINT9
PC10		I/O	NAND_DQ5	SDC2_D0			PC_EINT10
PC11		I/O	NAND_DQ4	SDC2_D5			PC_EINT11
PC12		I/O	NAND_DQS		SPI0_CLK		PC_EINT12
PC13		I/O	NAND_DQ3	SDC2_D1			PC_EINT13
PC14		I/O	NAND_DQ2	SDC2_D6			PC_EINT14
PC15		I/O	NAND_DQ1	SDC2_D2	SPI0_WP		PC_EINT15
PC16		I/O	NAND_DQ0	SDC2_D7	SPI0_HOLD		PC_EINT16
PD0	GPIOD	I/O	LCD0_D2	LVDS0_D0P	DSI_DP0		PD_EINT0
PD1		I/O	LCD0_D3	LVDS0_D0N	DSI_DM0		PD_EINT1
PD2		I/O	LCD0_D4	LVDS0_D1P	DSI_DP1		PD_EINT2
PD3		I/O	LCD0_D5	LVDS0_D1N	DSI_DM1		PD_EINT3
PD4		I/O	LCD0_D6	LVDS0_D2P	DSI_CKP		PD_EINT4
PD5		I/O	LCD0_D7	LVDS0_D2N	DSI_CKM		PD_EINT5
PD6		I/O	LCD0_D10	LVDS0_CKP	DSI_DP2		PD_EINT6
PD7		I/O	LCD0_D11	LVDS0_CKN	DSI_DM2		PD_EINT7

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6
PD8		I/O	LCD0_D12	LVDS0_D3P	DSI_DP3		PD_EINT8
PD9		I/O	LCD0_D13	LVDS0_D3N	DSI_DM3		PD_EINT9
PD10		I/O	LCD0_D14	LVDS1_D0P	SPI1_CS		PD_EINT10
PD11		I/O	LCD0_D15	LVDS1_D0N	SPI1_CLK		PD_EINT11
PD12		I/O	LCD0_D18	LVDS1_D1P	SPI1_MOSI		PD_EINT12
PD13		I/O	LCD0_D19	LVDS1_D1N	SPI1_MISO		PD_EINT13
PD14		I/O	LCD0_D20	LVDS1_D2P	UART3_TX		PD_EINT14
PD15		I/O	LCD0_D21	LVDS1_D2N	UART3_RX		PD_EINT15
PD16		I/O	LCD0_D22	LVDS1_CKP/ PLL_TEST_CKP	UART3_RTS		PD_EINT16
PD17		I/O	LCD0_D23	LVDS1_CKN/ PLL_TEST_CKN	UART3_CTS		PD_EINT17
PD18		I/O	LCD0_CLK	LVDS1_D3P	UART4_TX		PD_EINT18
PD19		I/O	LCD0_DE	LVDS1_D3N	UART4_RX		PD_EINT19
PD20		I/O	LCD0_HSYNC	PWM2	UART4_RTS		PD_EINT20
PD21		I/O	LCD0_VSYNC	PWM3	UART4_CTS		PD_EINT21
PD22		I/O	PWM1		TWI0_SCK		PD_EINT22
PD23		I/O	PWM0		TWI0_SDA		PD_EINT23
PE0	GPIOE	I/O	MIPI_MCLK0				PE_EINT0
PE1		I/O	TWI2_SCK				PE_EINT1
PE2		I/O	TWI2_SDA				PE_EINT2
PE3		I/O	TWI3_SCK				PE_EINT3
PE4		I/O	TWI3_SDA				PE_EINT4
PE5		I/O	MIPI_MCLK1	PLL_LOCK_DBG	I2S2_MCLK	LEDC	PE_EINT5
PE6		I/O		BIST_RESULT0	I2S2_BCLK		PE_EINT6
PE7		I/O	CSI_SM_VS	BIST_RESULT1	I2S2_LRCK		PE_EINT7
PE8		I/O		BIST_RESULT2	I2S2_DOUT0		PE_EINT8
PE9		I/O		BIST_RESULT3	I2S2_DIN0		PE_EINT9
PF0	GPIOF	I/O	SDC0_D1	JTAG_MS	JTAG_MS_GPU		PF_EINT0
PF1		I/O	SDC0_D0	JTAG_DI	JTAG_DI_GPU		PF_EINT1
PF2		I/O	SDC0_CLK	UART0_TX			PF_EINT2
PF3		I/O	SDC0_CMD	JTAG_DO	JTAG_DO_GPU		PF_EINT3
PF4		I/O	SDC0_D3	UART0_RX			PF_EINT4
PF5		I/O	SDC0_D2	JTAG_CK	JTAG_CK_GPU		PF_EINT5
PF6		I/O					PF_EINT6
PG0	GPIOG	I/O	SDC1_CLK				PG_EINT0
PG1		I/O	SDC1_CMD				PG_EINT1
PG2		I/O	SDC1_D0				PG_EINT2
PG3		I/O	SDC1_D1				PG_EINT3
PG4		I/O	SDC1_D2				PG_EINT4
PG5		I/O	SDC1_D3				PG_EINT5
PG6		I/O	UART1_TX				PG_EINT6
PG7		I/O	UART1_RX				PG_EINT7
PG8		I/O	UART1_RTS				PG_EINT8
PG9		I/O	UART1_CTS	I2S1_MCLK			PG_EINT9
PG10		I/O		I2S1_BCLK			PG_EINT10
PG11		I/O		I2S1_LRCK			PG_EINT11
PG12		I/O		I2S1_DOUT0	I2S1_DIN1		PG_EINT12
PG13		I/O		I2S1_DIN0	I2S1_DOUT1		PG_EINT13
PH0	GPIOH	I/O	TWI0_SCK			RGMII0_RXD1/ RMII0_RXD1	PH_EINT0
PH1		I/O	TWI0_SDA			RGMII0_RXD0/ RMII0_RXD0	PH_EINT1

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6
PH2		I/O	TWI1_SCK	CPU_CUR_W		RGMII0_RXCTL/ RMII0_CRS_DV	PH_EINT2
PH3		I/O	TWI1_SDA	CIR_OUT		RGMII0_CLKIN/ RMII0_RXER	PH_EINT3
PH4		I/O	UART3_TX	SPI1_CS	CPU_CUR_W	RGMII0_TXD1/ RMII0_TXD1	PH_EINT4
PH5		I/O	UART3_RX	SPI1_CLK	LEDC	RGMII0_TXD0/ RMII0_TXD0	PH_EINT5
PH6		I/O	UART3_RTS	SPI1_MOSI		RGMII0_TXCK/ RMII0_TXCK	PH_EINT6
PH7		I/O	UART3_CTS	SPI1_MISO	OWA_OUT	RGMII0_TXCTL/ RMII0_TXEN	PH_EINT7
PH8		I/O	DMIC_CLK	SPI2_CS	I2S2_MCLK	I2S2_DIN2	PH_EINT8
PH9		I/O	DMIC_DATA0	SPI2_CLK	I2S2_BCLK	MDC0	PH_EINT9
PH10		I/O	DMIC_DATA1	SPI2_MOSI	I2S2_LRCK	MDIO0	PH_EINT10
PH11		I/O	DMIC_DATA2	SPI2_MISO	I2S2_DOUT0	I2S2_DIN1	PH_EINT11
PH12		I/O	DMIC_DATA3	TWI3_SCK	I2S2_DIN0	I2S2_DOUT1	PH_EINT12
PH13		I/O		TWI3_SDA	I2S3_MCLK	EPHY0_25	PH_EINT13
PH14		I/O			I2S3_BCLK	RGMII0_RXD3/ RMII0_NULL	PH_EINT14
PH15		I/O			I2S3_LRCK	RGMII0_RXD2/ RMII0_NULL	PH_EINT15
PH16		I/O		I2S3_DOUT0	I2S3_DIN1	RGMII0_RXCK/ RMII0_NULL	PH_EINT16
PH17		I/O		I2S3_DOUT1	I2S3_DIN0	RGMII0_TXD3/ RMII0_NULL	PH_EINT17
PH18		I/O	CIR_OUT	I2S3_DOUT2	I2S3_DIN2	RGMII0_TXD2/ RMII0_NULL	PH_EINT18
PH19		I/O	CIR_IN	I2S3_DOUT3	I2S3_DIN3	LEDC	PH_EINT19
PL0	GPIOL	I/O	S_TWI0_SCK				S_PL_EINT0
PL1		I/O	S_TWI0_SDA				S_PL_EINT1
PL2		I/O	S_UART_TX				S_PL_EINT2
PL3		I/O	S_UART_RX				S_PL_EINT3
PL4		I/O	S_JTAG_MS				S_PL_EINT4
PL5		I/O	S_JTAG_CK				S_PL_EINT5
PL6		I/O	S_JTAG_DO				S_PL_EINT6
PL7		I/O	S_JTAG_DI				S_PL_EINT7
PL8		I/O	S_TWI1_SCK				S_PL_EINT8
PL9		I/O	S_TWI1_SDA				S_PL_EINT9
PL10		I/O	S_PWM				S_PL_EINT10
PL11		I/O	S_CPU_CUR_W	S_CIR_IN			S_PL_EINT11

4.4. Detailed Signal Description

Table 4-4 shows the detailed function description of every signal based on the different interface.

[1].**Signal Name**: The name of every signal.

[2].**Description**: The detailed function description of every signal.

[3].**Type**: Denotes the signal direction:

I (Input),
O (Output),
I/O (Input/Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),

AO (Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)

Table 4-4. Detailed Signal Description

Signal Name[1]	Description[2]	Type[3]
DRAM		
SDQ[31:0]	DRAM bidirectional data line to the memory device	I/O
SDQS[3:0]P	DRAM active-high bidirectional data strobes to the memory device	I/O
SDQS[3:0]N	DRAM active-Low bidirectional data strobes to the memory device	I/O
SDQM[3:0]	DRAM data mask signal to the memory device	O
SCKP	DRAM active-high clock signal to the memory device	O
SCKN	DRAM active-low clock signal to the memory device	O
SCKE[1:0]	DRAM clock enable signal to the memory device	O
SA[16:0]	DRAM address signal to the memory device	O
SBA[1:0]	DRAM bank address signal to the memory device	O
SBG[1:0]	DRAM bank group address signal to the memory device	O
SACT	DRAM activation command output	O
SCS[1:0]	DRAM chip select signal to the memory device	O
SODT[1:0]	DRAM on-die termination output signal	O
SZQ	DRAM ZQ calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer)	AI
SRST	DRAM reset signal to the memory device	O
VCC_DRAM	DRAM power supply	P
VDD18_DRAM	SDRAM controller power supply	P
System Control		
NMI	Non-maskable interrupt	OD
FEL	Boot select Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process. For more details, see section 3.4 “BROM System” in the ***Allwinner R818 User Manual***.	I
BOOT_SEL	Boot media select	I
JTAG_SEL	JTAG mode select The signal is used to select the port from which JTAG function outputs.	I
RESET	Reset signal(low active)	I/O
RTC		
X32KIN	Clock input of 32.768 kHz crystal	AI
X32KOUT	Clock output of 32.768 kHz crystal	AO
X32KFOUT	32.768 kHz clock fanout Provides low frequency clock for external devices	OD
RTC_VIO	RTC low voltage(generated by internal LDO)	AO
VCC_RTC	RTC power	P
DCXO		

Signal Name[1]	Description[2]	Type[3]
DXLDO_OUT	Internal supply regulator output	AO
REFCLK_OUT	Digital compensated crystal oscillator clock fanout	AO
DXIN	Digital compensated crystal oscillator input	AI
DXOUT	Digital compensated crystal oscillator output	AO
WREQIN	Request signal of REFCLK_OUT	AI
USB		
USB0_DM	USB2.0 OTG data signal DM	A I/O
USB0_DP	USB2.0 OTG data signal DP	A I/O
USB1_DM	USB2.0 HOST data signal DM	A I/O
USB1_DP	USB2.0 HOST data signal DP	A I/O
VCC_USB	USB analog power supply	P
VDD_USB	USB digital power supply	P
GPADC		
GPADC1	General purpose ADC input channel	AI
BOOT_SEL_ADC	BROM boot select	AI
LRADC		
LRADC	Low rate ADC input channel	AI
AUDIO CODEC		
AGND	Analog ground	G
VRA1	Reference voltage	AO
VRA2	Reference voltage	AO
AVCC	Power supply for analog part	P
VEE	PA negative voltage input	P
CPVDD	Analog power for headphone charge pump	P
CPVEE	Charge pump negative voltage output	P
CPVIN	Analog power for LDO	P
MBIAS	First bias voltage output for main microphone	AO
HBIAS	Second bias voltage output for headset microphone	AO
HP_DET	Headphone Jack detect	AI
HPOUTFB	Pseudo differential headphone ground reference	AI
HPOUTL	Headphone left output	AO
HPOUTR	Headphone right output	AO
LINEOUTLN	Negative differential output for lineout	AO
LINEOUTLP	Positive differential output for lineout	AO
MIC_DET	Headphone MIC detect	AI
MICIN1N	Negative differential input for MIC1	AI
MICIN1P	Positive differential input for MIC1	AI
MICIN2N	Negative differential input for MIC2	AI
MICIN2P	Positive differential input for MIC2	AI
MIPI CSI		
MCSIA_CKN	MIPI CSI controller A clock negative signal	AI
MCSIA_CKP	MIPI CSI controller A clock positive signal	AI
MCSIA_D0N	MIPI CSI controller A data0 negative signal	AI
MCSIA_D0P	MIPI CSI controller A data0 positive signal	AI

Signal Name[1]	Description[2]	Type[3]
MCSIA_D1N	MIPI CSI controller A data1 negative signal	AI
MCSIA_D1P	MIPI CSI controller A data1 positive signal	AI
MCSIA_D2N	MIPI CSI controller A data2 negative signal	AI
MCSIA_D2P	MIPI CSI controller A data2 positive signal	AI
MCSIA_D3N	MIPI CSI controller A data3 negative signal	AI
MCSIA_D3P	MIPI CSI controller A data3 positive signal	AI
MCSIB_CKN	MIPI CSI controller B clock negative signal	AI
MCSIB_CKP	MIPI CSI controller B clock positive signal	AI
MCSIB_D0N	MIPI CSI controller B data0 negative signal	AI
MCSIB_D0P	MIPI CSI controller B data0 positive signal	AI
MCSIB_D1N	MIPI CSI controller B data1 negative signal	AI
MCSIB_D1P	MIPI CSI controller B data1 positive signal	AI
VCC_MCSI	MIPI CSI power supply	P
MIPI_MCLK0	MIPI CSI controller A master clock	O
MIPI_MCLK1	MIPI CSI controller B master clock	O
CSI_SM_VS	MIPI CSI slave mode vertical SYNC	O
LEDC		
LEDC	Intelligent control LED signal output	O
NAND Flash		
NAND_WE	Nand Flash write enable	O
NAND_ALE	Nand Flash address latch enable	O
NAND_CLE	Nand Flash command latch enable	O
NAND_CE[1:0]	Nand Flash chip select	O
NAND_RE	Nand Flash read enable	O
NAND_RB[1:0]	Nand Flash ready/busy status indicator signal	I
NAND_DQ[7:0]	Nand Flash data bit	I/O
NAND_DQS	Nand Flash data strobe	I/O
SMHC		
SDC0_D[3:0]	SDC0 data bit	I/O
SDC0_CLK	SDC0 clock	O
SDC0_CMD	SDC0 command signal	I/O,OD
SDC1_D[3:0]	SDC1 data bit	I/O
SDC1_CLK	SDC1 clock	O
SDC1_CMD	SDC1 command signal	I/O,OD
SDC2_D[7:0]	SDC2 data bit	I/O
SDC2_CLK	SDC2 clock	O
SDC2_CMD	SDC2 command signal	I/O,OD
SDC2_DS	SDC2 data strobe	I
SDC2_RST	SDC2 reset	O
LCD		
LCD0_D[7:2], LCD0_D[15:10], LCD0_D[23:18]	LCD data bit	O
LCD0_CLK	LCD clock signal	O
LCD0_DE	LCD data enable	O

Signal Name[1]	Description[2]	Type[3]
LCD0_HSYNC	LCD horizontal sync	O
LCD0_VSYNC	LCD vertical sync	O
LVDS		
LVDS0_D[3:0]P	LVDS0 differential data positive signal	O
LVDS0_D[3:0]N	LVDS0 differential data negative signal	O
LVDS0_CKP	LVDS0 differential clock positive signal	O
LVDS0_CKN	LVDS0 differential clock negative signal	O
LVDS1_D[3:0]P	LVDS1 differential data positive signal	O
LVDS1_D[3:0]N	LVDS1 differential data negative signal	O
LVDS1_CKP/PLL_TEST_CKP	LVDS1 differential clock positive signal	O
LVDS1_CKN/PLL_TEST_CKN	LVDS1 differential clock negative signal	O
VCC_LVDS	LVDS0/1 power	P
DSI		
DSI_DP0	DSI differential data0 positive signal	I/O
DSI_DM0	DSI differential data0 negative signal	I/O
DSI_DP1	DSI differential data1 positive signal	O
DSI_DM1	DSI differential data1 negative signal	O
DSI_DP2	DSI differential data2 positive signal	O
DSI_DM2	DSI differential data2 negative signal	O
DSI_DP3	DSI differential data3 positive signal	O
DSI_DM3	DSI differential data3 negative signal	O
DSI_CKP	DSI differential clock positive signal	O
DSI_CKM	DSI differential clock negative signal	O
I2S/PCM		
I2S0_MCLK	I2S0 master clock	O
I2S0_LRCK	I2S0/PCM0 sample rate clock/sync	I/O
I2S0_BCLK	I2S0/PCM0 sample rate clock	I/O
I2S0_DOUT[1:0]	I2S0/PCM0 serial data output channel [1:0]	O
I2S0_DIN[1:0]	I2S0/PCM0 serial data input channel [1:0]	I
I2S1_MCLK	I2S1 master clock	O
I2S1_LRCK	I2S1/PCM1 sample rate clock/sync	I/O
I2S1_BCLK	I2S1/PCM1 sample rate clock	I/O
I2S1_DOUT[1:0]	I2S1/PCM1 serial data output channel [1:0]	O
I2S1_DIN[1:0]	I2S1/PCM1 serial data input channel [1:0]	I
I2S2_MCLK	I2S2 master clock	O
I2S2_LRCK	I2S2/PCM2 sample rate clock/sync	I/O
I2S2_BCLK	I2S2/PCM2 sample rate clock	I/O
I2S2_DOUT[1:0]	I2S2/PCM2 serial data output channel [1:0]	O
I2S2_DIN[1:0]	I2S2/PCM2 serial data input channel [1:0]	I
I2S3_MCLK	I2S3 master clock	O
I2S3_LRCK	I2S3/PCM3 sample rate clock/sync	I/O
I2S3_BCLK	I2S3/PCM3 sample rate clock	I/O
I2S3_DOUT[3:0]	I2S3/PCM3 serial data output channel [3:0]	O
I2S3_DIN[3:0]	I2S3/PCM3 serial data input channel [3:0]	I

Signal Name[1]	Description[2]	Type[3]
DMIC		
DMIC_CLK	Digital microphone clock output	O
DMIC_DATA[3:0]	Digital microphone data input	I
OWA		
OWA_OUT	One wire audio output	O
Interrupt		
PB_EINT[10:0]	GPIO B interrupt	I
PC_EINT[16:0]	GPIO C interrupt	I
PD_EINT[23:0]	GPIO D interrupt	I
PE_EINT[9:0]	GPIO E interrupt	I
PF_EINT[6:0]	GPIO F interrupt	I
PG_EINT[13:0]	GPIO G interrupt	I
PH_EINT[19:0]	GPIO H interrupt	I
S_PL_EINT[11:0]	GPIO L interrupt	I
PWM		
PWM[3:0]	Pulse width modulation output channel [3:0] in CPUX	I/O
S_PWM	Pulse width modulation output channel in CPUS	I/O
CIR Receiver		
CIR_IN	Consumer infrared receiver in CPUX	I
S_CIR_IN	Consumer infrared receiver in CPUS	I
CIR_OUT	Consumer infrared transmitter	O
EMAC		
RGMII0_RXD3/RMII0_NULL	RGMII0 receive data3	I
RGMII0_RXD2/RMII0_NULL	RGMII0 receive data2	I
RGMII0_RXD1/RMII0_RXD1	RGMII0/RMII0 receive data1	I
RGMII0_RXD0/RMII0_RXD0	RGMII0/RMII0 receive data0	I
RGMII0_RXCK/RMII0_NULL	RGMII0 receive clock	I
RGMII0_RXCTL/RMII0_CRS_DV	RGMII0 receive control/RMII0 carrier sense receive data valid	I
RGMII0_CLKIN/RMII0_RXER	RGMII0 transmit clock from external/RMII0 receive error For RGMII0, IO type is output; For RMII0, IO type is input	I/O
RGMII0_TXD3/RMII0_NULL	RGMII0 transmit data3	O
RGMII0_TXD2/RMII0_NULL	RGMII0 transmit data2	O
RGMII0_TXD1/RMII0_TXD1	RGMII0/RMII0 transmit data1	O
RGMII0_TXD0/RMII0_TXD0	RGMII0/RMII0 transmit data0	O
RGMII0_TXCK/RMII0_TXCK	RGMII0/RMII0 transmit clock For RGMII0, IO type is output; For RMII0, IO type is input	I/O
RGMII0_TXCTL/RMII0_TXEN	RGMII0 transmit control/RMII0 transmit enable	O
MDC0	RGMII0/RMII0 management data clock	O
MDIO0	RGMII0/RMII0 management data input/output	I/O
EPHY0_25	25MHz output for EMAC PHY	O
SPI		
SPI0_CS0	SPI0 chip select0 signal, low active	I/O

Signal Name[1]	Description[2]	Type[3]
SPI0_CS1	SPI0 chip select1 signal, low active	I/O
SPI0_CLK	SPI0 clock signal	I/O
SPI0_MOSI	SPI0 master data out, slave data in	I/O
SPI0_MISO	SPI0 master data in, slave data out	I/O
SPI0_WP	SPI0 write protect, low active	I/O
SPI0_HOLD	SPI0 hold signal	I/O
SPI1_CS	SPI1 chip select signal, low active	I/O
SPI1_CLK	SPI1 clock signal	I/O
SPI1_MOSI	SPI1 master data out, slave data in	I/O
SPI1_MISO	SPI1 master data in, slave data out	I/O
SPI2_CS	SPI2 chip select signal, low active	I/O
SPI2_CLK	SPI2 clock signal	I/O
SPI2_MOSI	SPI2 master data out, slave data in	I/O
SPI2_MISO	SPI2 master data in, slave data out	I/O
UART		
UART0_TX	UART0 data transmit	O
UART0_RX	UART0 data receive	I
UART1_TX	UART1 data transmit	O
UART1_RX	UART1 data receive	I
UART1_CTS	UART1 data clear to send	I
UART1_RTS	UART1 data request to send	O
UART2_TX	UART2 data transmit	O
UART2_RX	UART2 data receive	I
UART2_CTS	UART2 data clear to send	I
UART2_RTS	UART2 data request to send	O
UART3_TX	UART3 data transmit	O
UART3_RX	UART3 data receive	I
UART3_CTS	UART3 data clear to send	I
UART3_RTS	UART3 data request to send	O
UART4_TX	UART4 data transmit	O
UART4_RX	UART4 data receive	I
UART4_CTS	UART4 data clear to send	I
UART4_RTS	UART4 data request to send	O
S_UART_TX	S_UART data transmit	O
S_UART_RX	S_UART data receive	I
TWI		
TWI0_SCK	TWI0 serial clock signal	I/O
TWI0_SDA	TWI0 serial data signal	I/O
TWI1_SCK	TWI1 serial clock signal	I/O
TWI1_SDA	TWI1 serial data signal	I/O
TWI2_SCK	TWI2 serial clock signal	I/O
TWI2_SDA	TWI2 serial data signal	I/O
TWI3_SCK	TWI3 serial clock signal	I/O
TWI3_SDA	TWI3 serial data signal	I/O

Signal Name[1]	Description[2]	Type[3]
S_TWI0_SCK	S_TWI0 serial clock signal	I/O
S_TWI0_SDA	S_TWI0 serial data signal	I/O
S_TWI1_SCK	S_TWI1 serial clock signal	I/O
S_TWI1_SDA	S_TWI1 serial data signal	I/O
JTAG		
JTAG_MS	JTAG mode select	I
JTAG_CK	JTAG clock signal	I
JTAG_DO	JTAG data output	O
JTAG_DI	JTAG data input	I
JTAG_MS_GPU	JTAG mode select	I
JTAG_CK_GPU	JTAG clock signal	I
JTAG_DO_GPU	JTAG data output	O
JTAG_DI_GPU	JTAG data input	I
S_JTAG_MS	S_JTAG mode select	I
S_JTAG_CK	S_JTAG clock signal	I
S_JTAG_DO	S_JTAG data output	O
S_JTAG_DI	S_JTAG data input	I

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
AVCC	Analog Part Power		-0.3	2.16	V
VCC_PC	Digital GPIO C Power		-0.3	3.96	V
VCC_PD	Digital GPIO D Power		-0.3	3.96	V
VCC_PE	Digital GPIO E Power		-0.3	3.96	V
VCC_PG	Digital GPIO G Power		-0.3	3.96	V
VCC_PL	Digital GPIO L Power		-0.3	3.96	V
VCC_IO	GPIO B, GPIO F, GPIO H and System Control Power		-0.3	3.96	V
VCC_LVDS0	LVDS0/1 Power		-0.3	2.16	V
VCC_USB	USB Analog Power		-0.3	3.96	V
VDD_USB	USB Digital Power		-0.3	1.08	V
VCC_MCSI	MIPI CSI Power		-0.3	2.16	V
VCC_RTC	RTC Power		-0.3	2.16	V
VCC_EFUSE	EFUSE Program Mode Power		-0.3	2.16	V
VDD_CPUS	CPUS Power		-0.3	1.3	V
VDD_CPU	CPU Power		-0.3	1.3	V
VCC_PLL	System PLL Power		-0.3	2.16	V
VDD_SYS	Power Supply for System		-0.3	1.3	V
VCC_DRAM	DRAM Power		-0.3	2.16	V
VDD18_DRAM	DRAM 1.8V Internal PAD Power		-0.3	2.16	V
T_{STG}	Storage Temperature		-40	150	°C
Tj	Working Junction Temperature		-40	125	°C
V_{ESD}	ESD Stress Voltage	Human Body Model(HBM)	-2000	2000	V
		Charged Device Model(CDM)	-500	500	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin		Pass		

(1). Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.
(2). Level listed above is the passing level per ESDA/JEDEC JS-001-2017.
(3). Level listed above is the passing level per ESDA/JEDEC JS-002-2018.

(4). Based on JESD78E; each device is tested with IO pin injection of ±200mA at room temperature.

(5). Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.2. Recommended Operating Conditions

All R818 modules are used under the operating conditions contained in Table 5-2.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-40	-	85	°C
Tj	Working Junction Temperature Range	-40	-	110(1)	°C
AVCC	Analog Part Power	1.764	1.8	1.836	V
VCC_PC	Digital GPIO C Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC_PD	Digital GPIO D Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC_PE	Digital GPIO E Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC_PG	Digital GPIO G Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC_PL	Digital GPIO L Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC_IO	GPIO B, GPIO F, GPIO H and System Control Power	2.97	3.3	3.63	V
VCC_LVDS0	LVDS0/1 Power	1.75	1.8	1.98	V
VCC_USB	USB Analog Power	2.97	3.3	3.63	V
VDD_USB	USB Digital Power	0.837	0.9	0.99	V
VCC_MCSI	MIPI CSI Power	1.62	1.8	1.98	V
VCC_RTC	RTC Power	1.62	1.8	1.98	V
VCC_EFUSE	EFUSE Program Mode Power	1.8	1.89	1.98	V
VDD_CPUS	CPUS Power	0.87	0.9	0.93	V
VDD_CPU	CPU Power	0.81	-	1.2	V
VCC_PLL	System PLL Power	1.62	1.8	1.98	V
VDD_SYS	Power Supply for System	0.9	-	1.0	V
VCC_DRAM	DRAM Power DDR4 IO Domain Power LPDDR4 IO Domain Power LPDDR3 IO Domain Power DDR3 IO Domain Power DDR3L IO Domain Power	 1.14 1.06 1.14 1.425 1.28	 1.2 1.1 1.2 1.5 1.35	 1.26 1.17 1.3 1.575 1.45	V
VDD18_DRAM	DRAM 1.8V Internal PAD Power	1.7	1.8	1.95	V

(1). The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 5-2.

5.3. Power Consumption Parameters

If you have questions about power consumption parameters, contact Allwinner FAE.

5.4. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of the R818.

Table 5-3. DC Electrical Characteristics
(VCC_IO/VCC_PC/VCC-PD/VCC_PE/VCC_PG/VCC_PL)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	80 3.76 12	100 4.7 15	120 5.64 18	kΩ
R_{PD}	Input Pull-down Resistance	80 3.76 12	100 4.7 15	120 5.64 18	kΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO – 0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

NOTE

For PL0~PL1 ports, the R_{PU} and R_{PD} are 4.7kΩ ±20%.
For PC0, PC1, PC3, PC6, PC7, PF3, PF6, and PG1~PG5 ports, the R_{PU} and R_{PD} are 15kΩ ±20%.
For other GPIO ports, the R_{PU} and R_{PD} are 100kΩ ±20%.

5.5. SDIO Electrical Characteristics

The SDIO electrical parameters are related to different supply voltage.

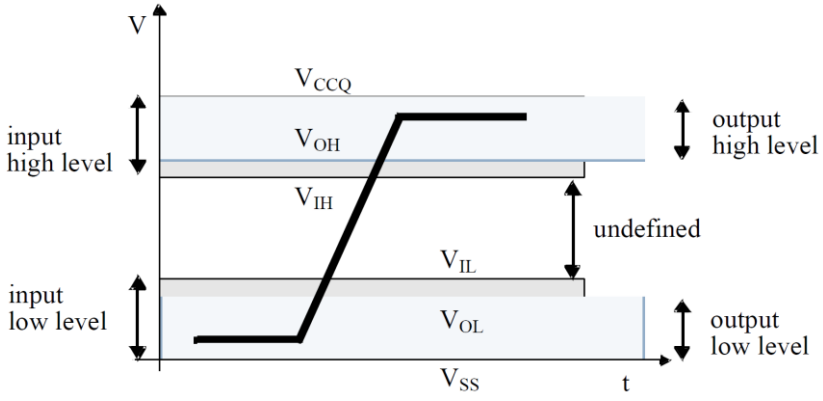


Figure 5-1. SDIO Voltage Waveform

Table 5-4 shows 3.3V SDIO electrical parameters.

Table 5-4. 3.3V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125 * V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 5-5 shows 1.8V SDIO electrical parameters.

Table 5-5. 1.8V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

5.6. GPADC Electrical Characteristics

The GPADC contains 1-ch analog-to-digital (ADC) converter. Table 5-6 lists GPADC electrical characteristics.

Table 5-6. GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	LEVELB(1)	V
Quantizing Error	-	8	-	LSB
Clock Frequency	-	-	1	MHz
Conversion Time	-	14	-	ADC Clock Cycles

5.7. LRADC Electrical Characteristics

The LRADC is 6-bit resolution ADC for key application. The LRADC can work up to 2 kHz conversion rate. Table 5-7 lists LRADC electrical characteristics.

Table 5-7. LRADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range	0	-	LEVELB(1)	V
Quantizing Error	-	2	-	LSB
Clock Frequency	-	-	2	kHz
Conversion Time	-	6	-	ADC Clock Cycles
(1) The maximum value of LEVELB is 1.266 V. For details, see the register description of LRADC in ***Allwinner_R818_User_Manual.***				

5.8. Audio Codec Electrical Characteristics

Test Conditions:

VDD_SYS = 0.9 V, AVCC = 1.8 V, CPVIN = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, fs = 48 kHz, input PGA gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 5-8. Audio Codec Typical Performance

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	**DAC to LINEOUTLP/N(R=10kΩ)**					
	Full-scale	0dBFS 1kHz	-	1.1	-	Vrms
	SNR (A-weighted)	0data	-	94	-	dB
	THD+N	0dBFS 1kHz	-	-80	-	dB
	DAC to Headphone on HPL or HPR(R = 10kΩ, CPVDD =1.2V)					
	Full-scale	0dBFS 1kHz	-	565	-	mVrms
	SNR (A-weighted)	0data	-	94	-	dB
	THD+N	0dBFS 1kHz	-	-80	-	dB
	Crosstalk	R_0dB_L_0data 1kHz/ L_0dB_R_0data 1kHz	-	-80	-	dB
	DAC to Headphone on HPL or HPR(R = 16Ω, CPVDD = 1.2V)					
	Full-scale Level	0dBFS 1kHz	-	420	-	mVrms
	SNR (A-weighted)	0data	-	94	-	dB
	THD+N (P0=11.0mW)	Full-scale Level	-	-40	-	dB
	THD+N (P0=10.0mW)	1kHz	-	-55	-	dB
	THD+N (P0=7.5mW)	1kHz	-	-75	-	dB
	Crosstalk	R_0dB_L_0data 1kHz/ L_0dB_R_0data 1kHz	-	-64	-	dB
	DAC to Headphone on HPL or HPR(R = 32Ω, CPVDD = 1.2V)					
	Full-scale Level	0dBFS 1kHz	-	544	-	mVrms
	SNR (A-weighted)	0data	-	94	-	dB
	THD+N (P0=9.0mW)	Full-scale Level	-	-50	-	dB
	THD+N (P0=7.5mW)	1kHz	-	-75	-	dB
	Crosstalk	R_0dB_L_0data 1kHz/ L_0dB_R_0data 1kHz	-	-74	-	dB
ADC Path	**MIC1 via ADCL or MIC2 via ADCR**					
	Output Level	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1kHz, 0dB Gain	-	885	-	mFFS
	SNR (A-weighted)	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1kHz, 0dB Gain	-	94	-	dB
	THD+N	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1kHz, 0dB Gain	-	-90	-	dB
	Output Level	MICP=1.695Vpp/2, MICN=1.695Vpp/2, 1kHz, 6dB Gain	-	885	-	mFFS
	SNR (A-weighted)	MICP=1.695Vpp/2, MICN=1.695Vpp/2, 1kHz, 6dB Gain	-	94	-	dB
	THD+N	MICP=1.695Vpp/2, MICN=1.695Vpp/2, 1kHz, 6dB Gain	-	-90	-	dB
	Output Level	MICP=803.2mVpp/2, MICN=803.2mVpp/2, 1kHz, 12dB Gain	-	885	-	mFFS
	SNR (A-weighted)	MICP=803.2mVpp/2, MICN=803.2mVpp/2, 1kHz, 12dB Gain	-	92	-	dB
	THD+N	MICP=803.2mVpp/2, MICN=803.2mVpp/2, 1kHz, 12dB Gain	-	-88	-	dB
	Output Level	MICP=404.0mVpp/2, MICN=404.0mVpp/2, 1kHz, 18dB Gain	-	885	-	mFFS
	SNR (A-weighted)	MICP=404.0mVpp/2, MICN=404.0mVpp/2, 1kHz, 18dB Gain	-	90	-	dB
	THD+N	MICP=404.0mVpp/2, MICN=404.0mVpp/2, 1kHz, 18dB Gain	-	-85	-	dB
	Output Level	MICP=204.6mVpp/2, MICN=204.6mVpp/2, 1kHz, 24dB Gain	-	885	-	mFFS
	SNR (A-weighted)	MICP=204.6mVpp/2, MICN=204.6mVpp/2, 1kHz, 24dB Gain	-	85	-	dB
	THD+N	MICP=204.6mVpp/2, MICN=204.6mVpp/2, 1kHz, 24dB Gain	-	-81	-	dB
	Output Level	MICP=104.8mVpp/2, MICN=104.8mVpp/2, 1kHz, 30dB Gain	-	885	-	mFFS

	SNR (A-weighted)	MICP=104.8mVpp/2, MICN=104.8mVpp/2, 1kHz, 30dB Gain	-	80	-	dB
	THD+N	MICP=104.8mVpp/2, MICN=104.8mVpp/2, 1kHz, 30dB Gain	-	-75	-	dB
	Output Level	MICP=55.1mVpp/2, MICN=55.1mVpp/2, 1kHz, 36dB Gain	-	885	-	mFFS
	SNR (A-weighted)	MICP=55.1mVpp/2, MICN=55.1mVpp/2, 1kHz, 36dB Gain	-	75	-	dB
	THD+N	MICP=55.1mVpp/2, MICN=55.1mVpp/2, 1kHz, 36dB Gain	-	-70	-	dB
MBIAS	Current	-	-	2.0	-	mA
	Voltage	-	1.8	2.0	2.55	V
	Noise	20Hz~20kHz	-	5.0	-	uV
HBIAS	Current	-	-	2.0	-	mA
	Voltage	-	1.8	2.0	2.55	V
	Noise	20Hz~20kHz	-	5.0	-	uV

5.9. Clock Electrical Characteristics

5.9.1. Input Clock Requirements

The R818 has two clock inputs. Each clock input passes through an internal oscillator which can be connected to an external crystal.

The 24 MHz oscillator provides a 24 MHz reference clock which is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through DXIN. Table 5-9 lists the recommended values of 24 MHz crystal.

Table 5-9. 24 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
1/(t_{CPMAIN})	Crystal Oscillator Frequency Range	-	24	-	MHz
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-

The 32.768 kHz oscillator provides a 32.768 kHz reference clock which is used for RTC and low frequency operation. It supplies the wake-up domain for operation in low-power mode. The clock is provided through X32KIN. Table 5-10 lists the recommended values of 32.768 kHz crystal.

Table 5-10. 32.768 kHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
1/(t_{CPMAIN})	Crystal Oscillator Frequency Range	-	32.768	-	kHz
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-

5.10. External Memory Electrical Characteristics

5.10.1. SDRAM AC Electrical Characteristics

5.10.1.1. DDR3/DDR3L Parameters

Figure 5-2 shows the DDR3/DDR3L command and address timing diagram. The timing parameters for this diagram shows in Table 5-11.

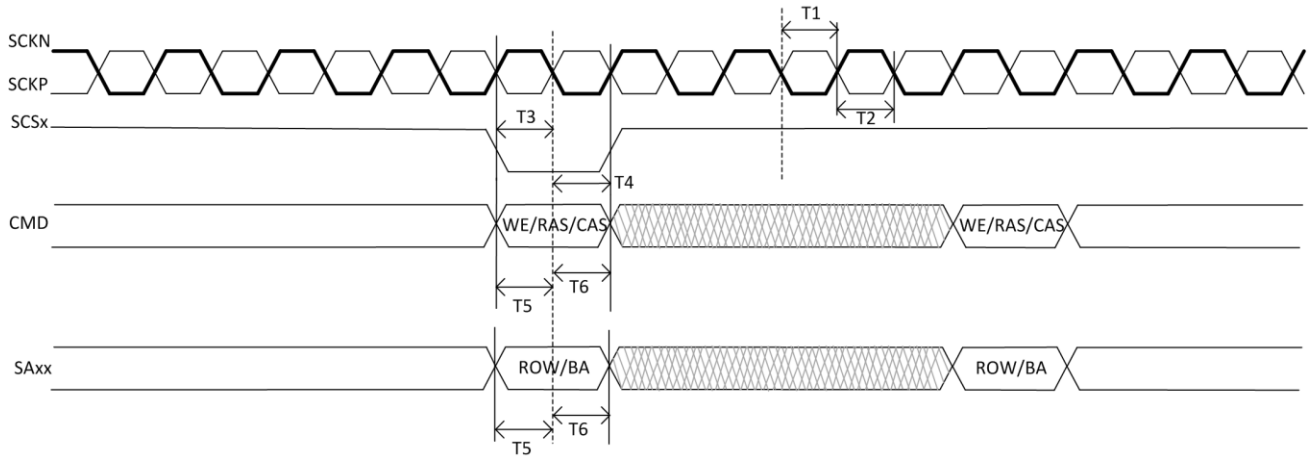


Figure 5-2. DDR3/DDR3L Command and Address Timing

Table 5-11. DDR3/DDR3L Timing Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T1	SCKP clock high-level width	t_{CH}	0.47	-	0.53	tck
T2	SCKP clock low-level width	t_{CL}	0.47	-	0.53	tck
T3	CS setup time	t_{IS}	170	295	-	ps
T4	CS hold time	t_{IH}	120	245	-	ps
T5	Command and Address setup time to Clock edge	t_{IS}	170	295	-	ps
T6	Command and Address hold time to Clock edge	t_{IH}	120	245	-	ps

T1 and T2 are in reference to Vref level.
T3, T4, T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-3 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram shows in Table 5-12.

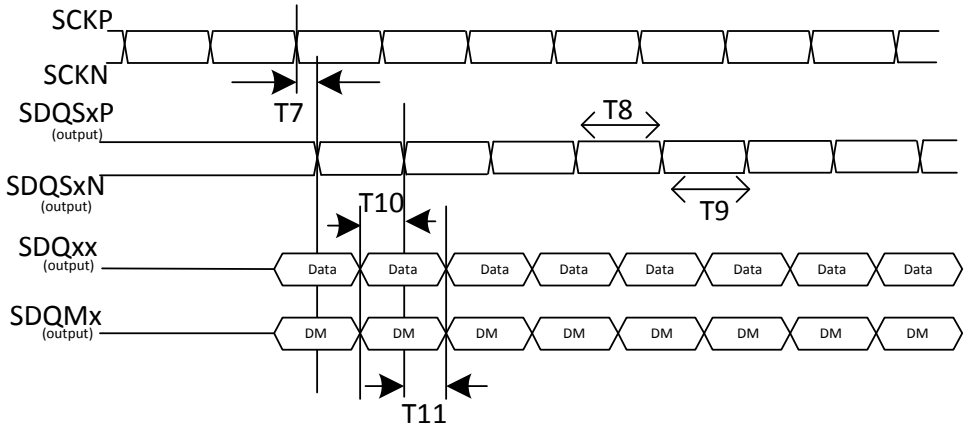


Figure 5-3. DDR3/DDR3L Write Cycle

Table 5-12. DDR3/DDR3L Write Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T7	SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge	t_{DQSS}	-0.27	-	0.27	t_{CK}
T8	SDQSxP high level width	t_{DQSH}	0.45	-	0.55	t_{CK}
T9	SDQSxP low level width	t_{DQSL}	0.45	-	0.55	t_{CK}
T10	Data setup time to SDQSxP/SDQSxN	t_{DS}	10	145	-	ps
T11	Data hold time to SDQSxP/SDQSxN	t_{DH}	45	180	-	ps

To receive the reported setup and hold values, writing calibration should be performed in order to locate the SDQSx in

the middle of SDQxx window.
T7,T8, and T9 are in reference to Vref level.
T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-4 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram shows in Table 5-13.

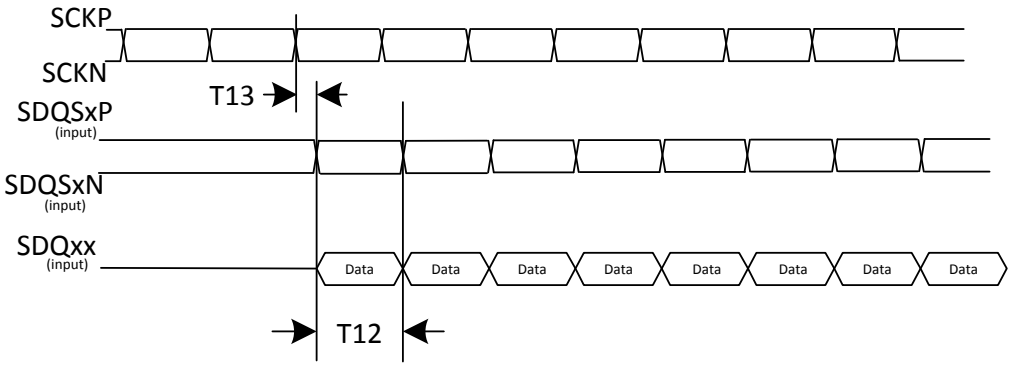


Figure 5-4. DDR3/DDR3L Read Cycle

Table 5-13. DDR3/DDR3L Read Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz		Unit
			Min	Max	
T12	Read Data valid width	t_{Data}	200	-	ps
T13	SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge	t_{DQSCK}	-225	225	ps

To receive the reported setup and hold values, writing calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 and T13 are in reference to Vref level.

5.10.1.2. LPDDR3 Parameters

Figure 5-5 shows the LPDDR3 command and address timing diagram. The timing parameters for this diagram shows in Table 5-14.

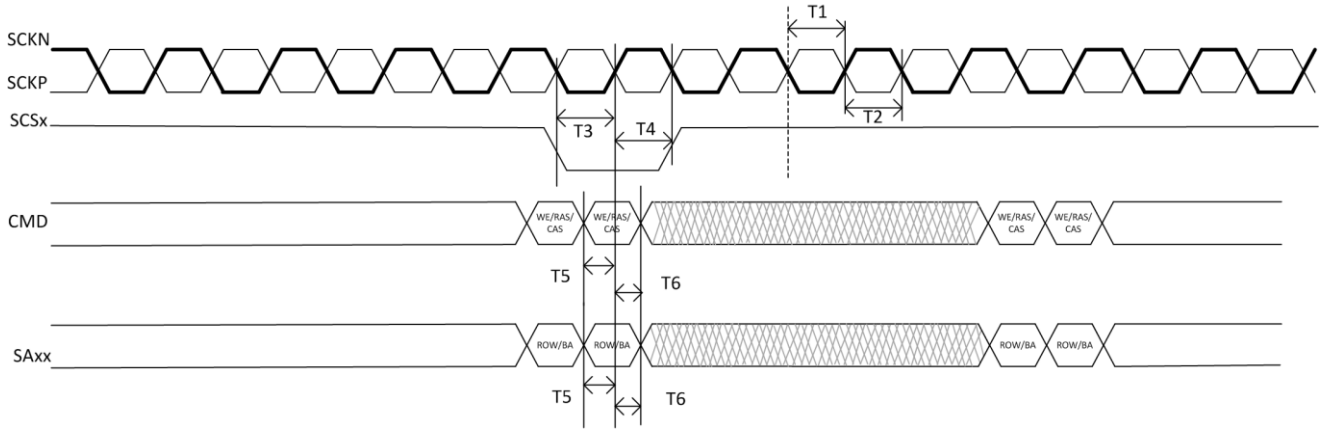


Figure 5-5. LPDDR3 Command and Address Timing Diagram

Table 5-14. LPDDR3 Command and Address Timing Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T1	Clock high pulse width	t_{CH}	0.45	-	0.55	t_{CK}
T2	Clock low pulse width	t_{CL}	0.45	-	0.55	t_{CK}
T3	SCSx input setup time	t_{ISCS}	195	347.5	-	ps
T4	SCSx input hold time	t_{IHCS}	220	372.5	-	ps
T5	Address and control input setup time	t_{IAS}	75	152.5	-	ps

T6	Address and control input hold time	t_{IAH}	100	177.5	-	ps

T1 and T2 are in reference to Vref level.
T3,T4,T5,and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-6 shows the LPDDR3 write timing diagram. The timing parameters for this diagram shows in Table 5-15.

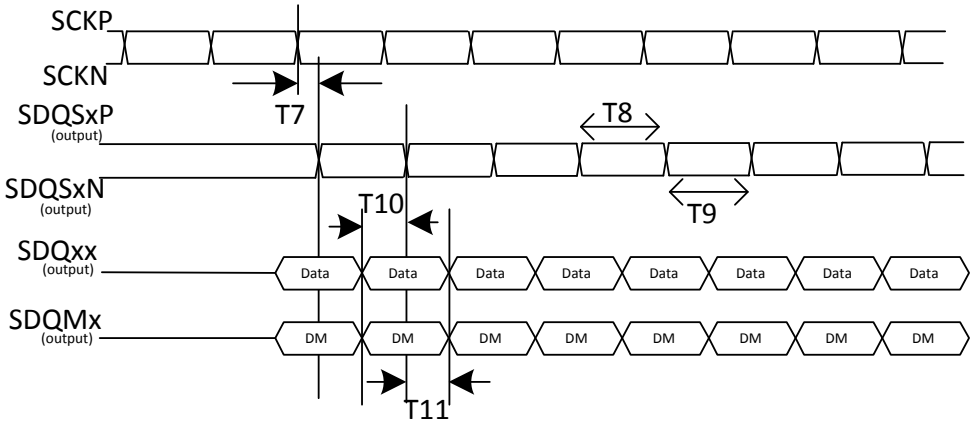


Figure 5-6. LPDDR3 Write Cycle

Table 5-15. LPDDR3 Write Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T7	SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge	t_{DQSS}	0.75	-	1.25	t_{CK}
T8	SDQSx input high-level width	t_{DQSH}	0.4	-	-	t_{CK}
T9	SDQSx input low-level width	t_{DQSL}	0.4	-	-	t_{CK}
T10	SDQxx and SDQMx input setup time	t_{DS}	75	152.5	-	ps
T11	SDQxx and SDQMx input hold time	t_{DH}	100	177.5	-	ps

To receive the reported setup and hold values, the write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T7, T8, and T9 are in reference to Vref level.
T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-7 shows the LPDDR3 read timing diagram. The timing parameters for this diagram shows in Table 5-16.

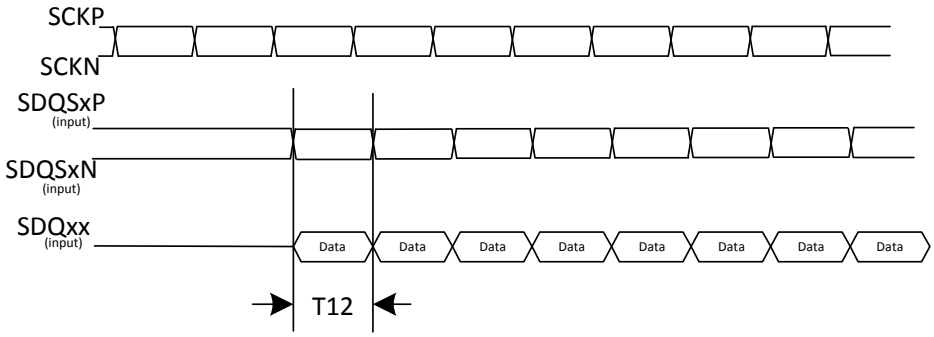


Figure 5-7. LPDDR3 Read Cycle

Table 5-16. LPDDR3 Read Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz		Unit
			Min	Max	
T12	Read Data valid width	t_{DATA}	200	-	ps

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 is in reference to Vref level.

5.10.1.3. DDR4 Parameters

Figure 5-8 shows the DDR4 command and address timing diagram. The timing parameters foe this diagram shows in Table 5-17.

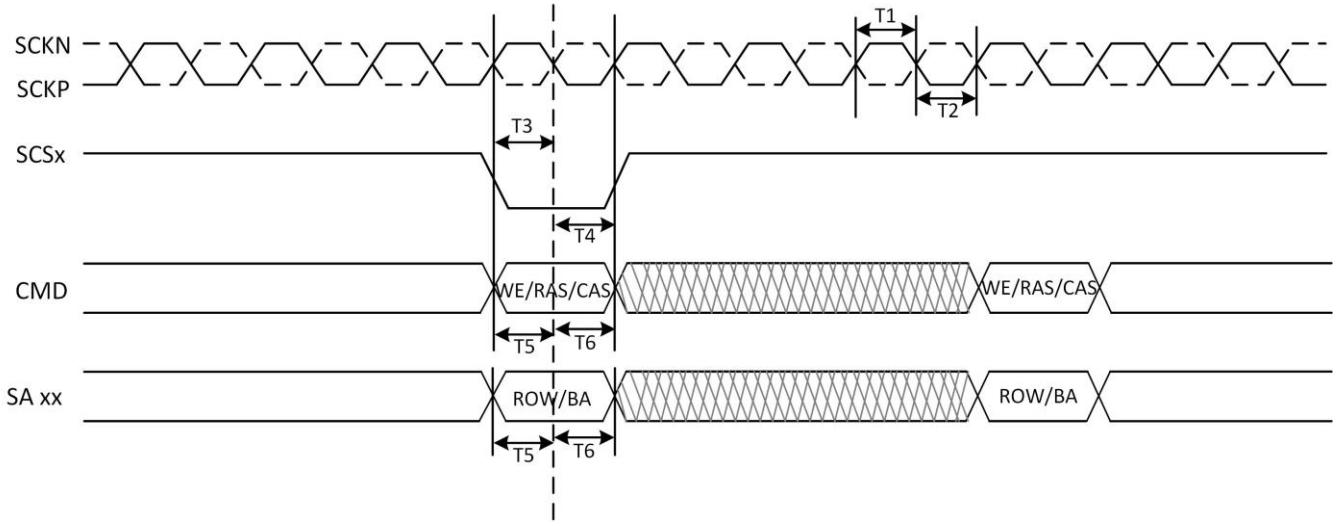


Figure 5-8. DDR4 Command and Address Timing

Table 5-17. DDR4 Timing Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T1	Clock high-level width	t_{CH}	0.48	-	0.52	tck
T2	Clock low-level width	t_{CL}	0.48	-	0.52	tck
T3	CS setup time	t_{IS}	115	-	-	ps
T4	CS hold time	t_{IH}	140	-	-	ps
T5	Command and Address setup time to CK	t_{IS}	115	-	-	ps
T6	Command and Address hold time to CK	t_{IH}	140	-	-	ps

T1~T2 are in reference to Vref level.
T3/T5 are in reference to Vih(ac) / Vil(ac) levels.(AC100)
T4/T6 are in reference to Vih(ac) / Vil(ac) levels.(DC75)

Figure 5-9 shows the DDR4 write timing diagram. The timing parameter for this diagram shows in Table 5-18.

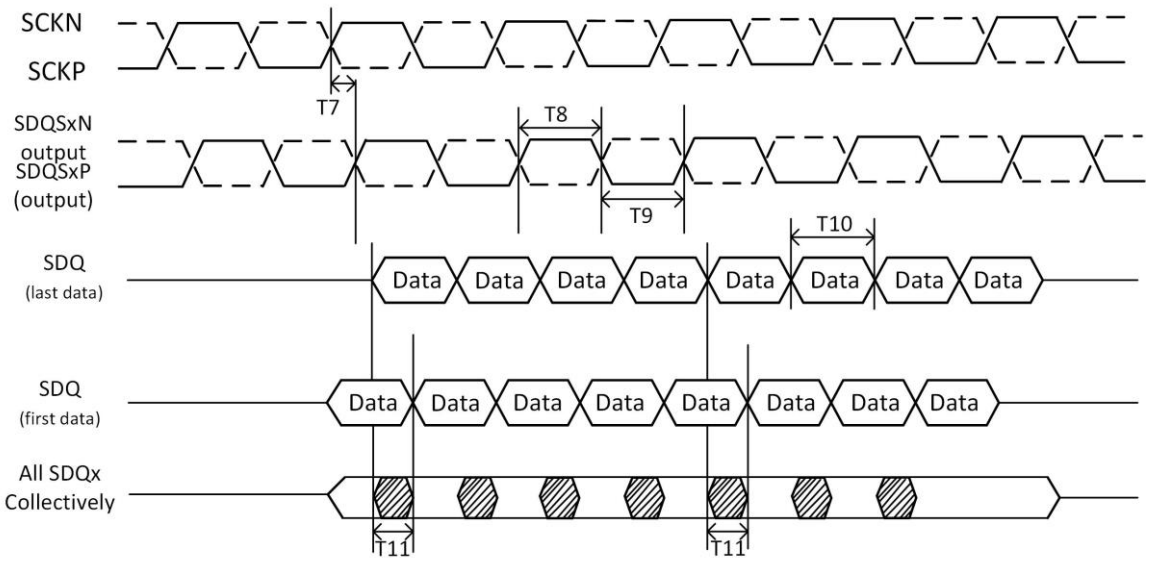


Figure 5-9. DDR4 Write Cycle

Table 5-18. DDR4 Write Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T7	SDQS rising edge to SCK rising edge	t_{DQSS}	-0.27	-	0.27	t_{CK}
T8	SDQS high level width	t_{DQSH}	0.46	-	0.54	t_{CK}
T9	SDQS low level width	t_{DQSL}	0.46	-	0.54	t_{CK}
T10	Data Valid Window per pin per UI	t_{DVWp}	0.66	-	-	t_{ui}
T11	Data Valid Window per device per UI	t_{DVWd}	0.63	-	-	t_{ui}

T7~T9 are in reference to Vref level.

T10 is Data Valid Window per pin per UI and is derived from (t_{QH} - t_{DQSQ}) of each UI on a pin of a given DRAM.

T11 is the Data Valid Window per device per UI and is derived from (t_{QH} - t_{DQSQ}) of each UI on a given DRAM.

Figure 5-10 shows the DDR4 read timing diagram. The timing parameters for this diagram shows in Table 5-19.

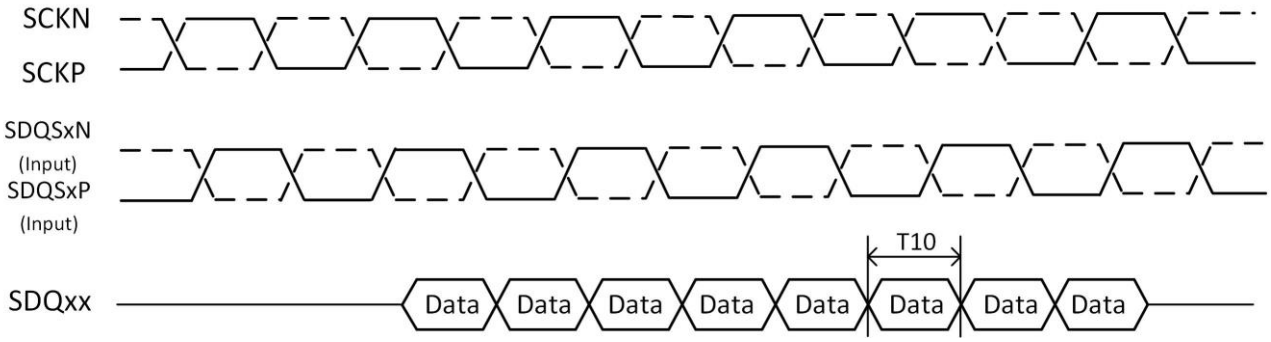


Figure 5-10. DDR4 Read Cycle

Table 5-19. DDR4 Read Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz		Unit
			Min	Max	
T10	Data Valid Window per pin per UI	t_{DVWp}	0.66	-	t_{ui}

T10 is in reference to Vref level.

5.10.1.4. LPDDR4 Parameters

Figure 5-11 shows the LPDDR4 command and address timing diagram. The timing parameters for this diagram shows in Table 5-20.

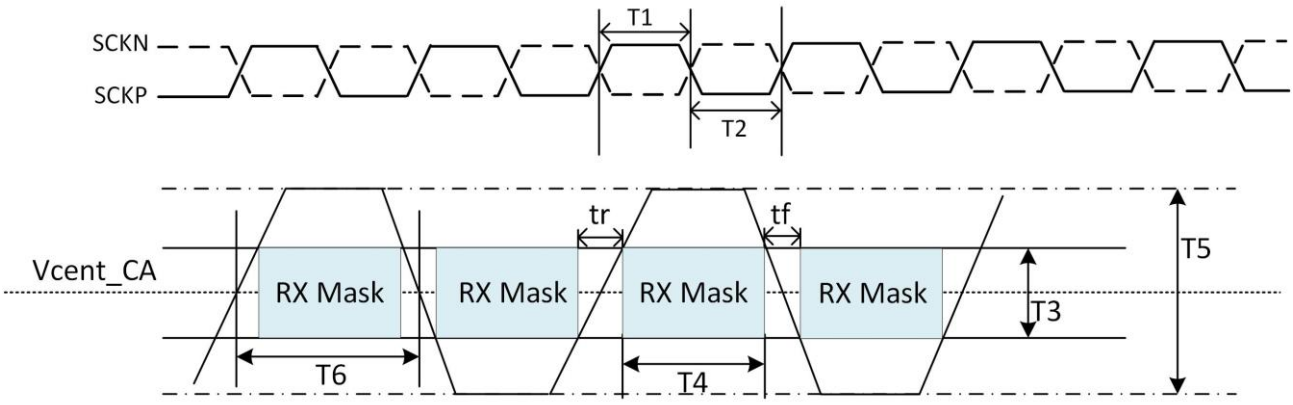


Figure 5-11. LPDDR4 Command and Address Timing Diagram

NOTE

T7 = T3/(tr or tf), signal must be monotonic within tr and tf range.

Table 5-20. LPDDR4 Command and Address Timing Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T1	Clock high pulse width	t_{CH}	0.46	-	0.54	t_{CK}
T2	Clock low pulse width	t_{CL}	0.46	-	0.54	t_{CK}
T3	Rx Mask voltage - p-p	V_{cIVW}	-	-	175	mV
T4	Rx timing window	T_{cIVW}	-	-	0.3	UI
T5	CA AC input pulse amplitude pk-pk	V_{IHL_AC}	210	-	-	mV
T6	CA input pulse width	T_{cIPW}	0.55	-	-	UI
T7	Input Slew Rate over VcIVW	SR_{IN_cIVW}	1	-	7	V/ns

Figure 5-12 shows the LPDDR4 write timing diagram. The timing parameters for this diagram shows in Table 5-21.

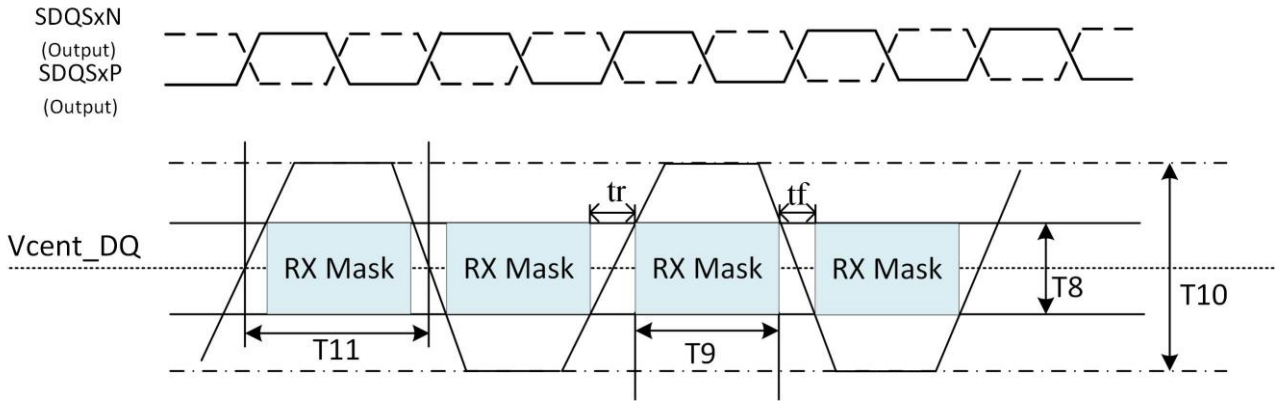


Figure 5-12. LPDDR4 Write Cycle

NOTE

T12 = T8/(tr or tf), signal must be monotonic within tr and tf range.

Table 5-21. LPDDR4 Write Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T8	Rx Mask voltage - p-p total	V_{dIVW_total}	-	-	140	mV
T9	Rx timing window total (At VdIVW voltage levels)	T_{dIVW_total}	-	-	0.22	UI
T10	DQ AC input pulse amplitude pk-pk	V_{IHL_AC}	180	-	-	mV
T11	Input pulse width (At Vcent_DQ)	$T_{dIPW\ DQ}$	0.45	-	-	UI
T12	Input Slew Rate over VdIVW_total	SR_{IN_dIVW}	1	-	7	V/ns

Figure 5-13 shows the LPDDR4 read timing diagram. The timing parameters for this diagram shows in Table 5-22.

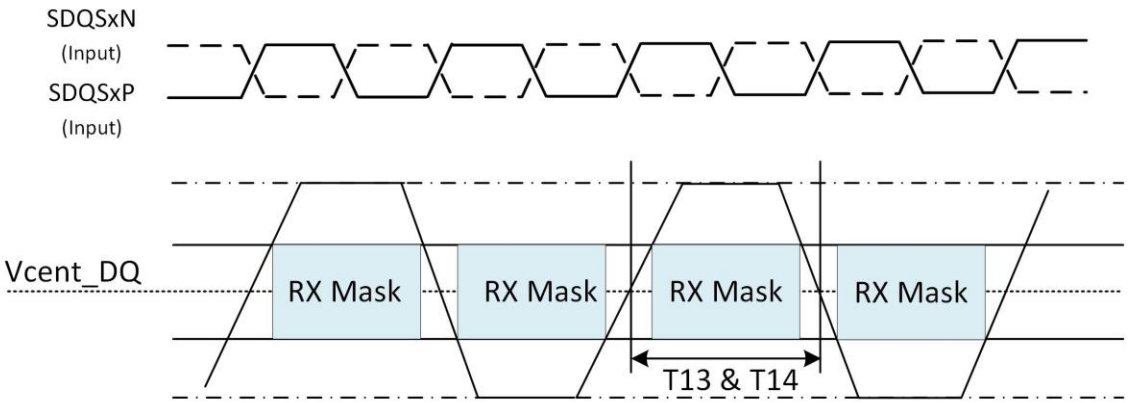


Figure 5-13. LPDDR4 Read Cycle

Table 5-22. LPDDR4 Read Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz		Unit
			Min	Max	
T13	DQ output window time total, per pin (DBI-Disabled)	t_{QW_total}	0.75	-	UI
T14	DQ output window time total, per pin (DBI-Enabled)	$t_{QW\_total\_DBI}$	0.75	-	UI

5.10.2. NAND AC Electrical Characteristics

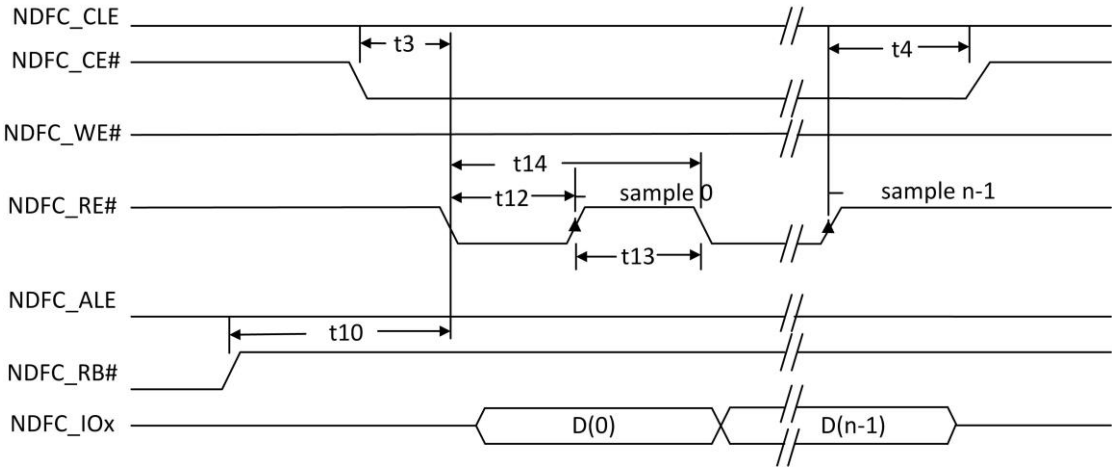


Figure 5-14. Conventional Serial Access Cycle Timing (SAM0)

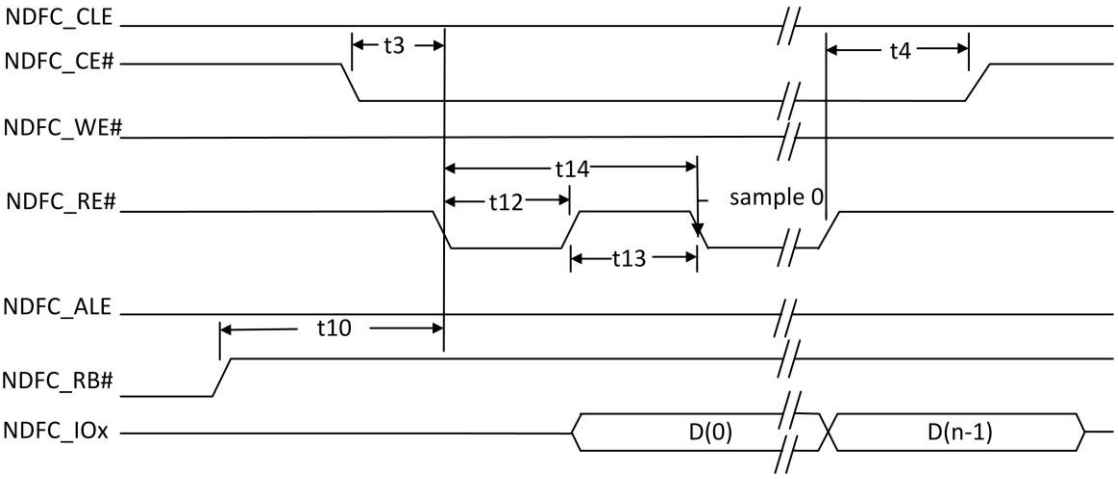


Figure 5-15. EDO Type Serial Access after Read Cycle Timing (SAM1)

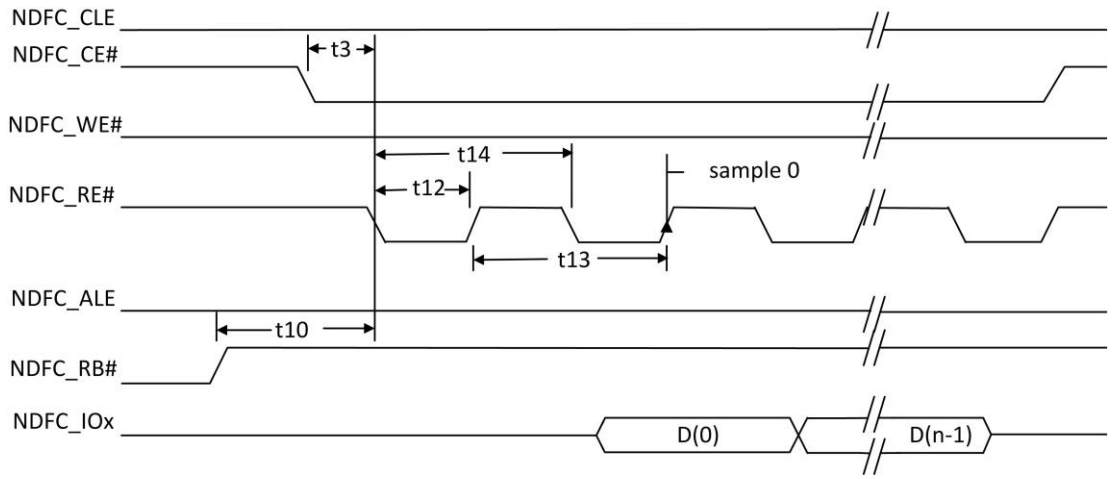


Figure 5-16. Extending EDO Type Serial Access Mode Timing (SAM2)

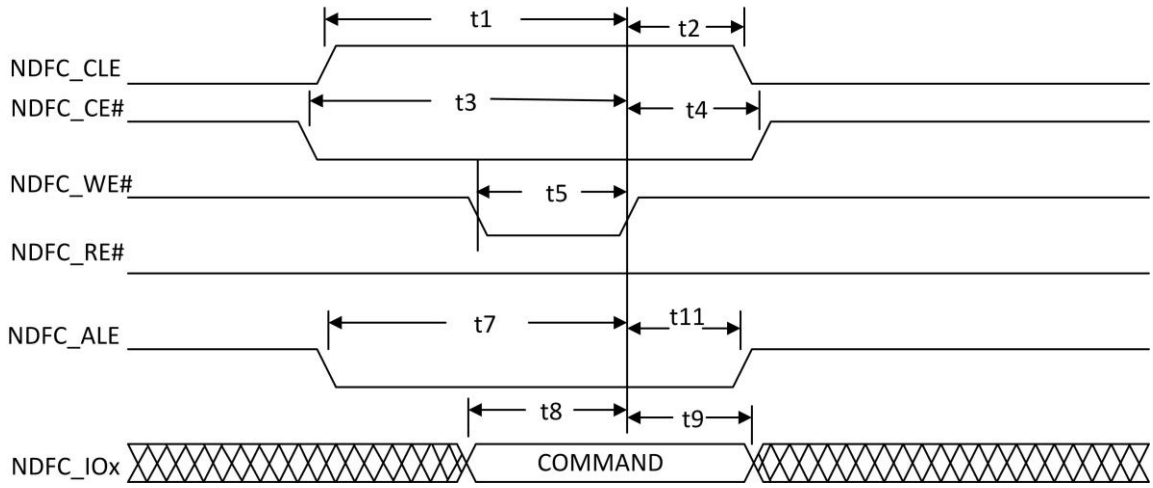


Figure 5-17. Command Latch Cycle Timing

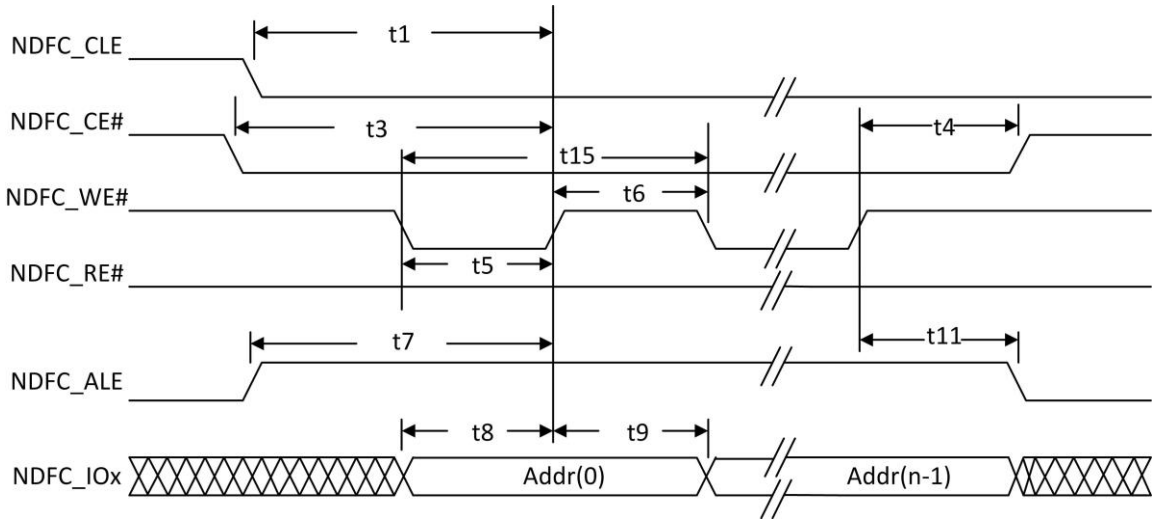


Figure 5-18. Address Latch Cycle Timing

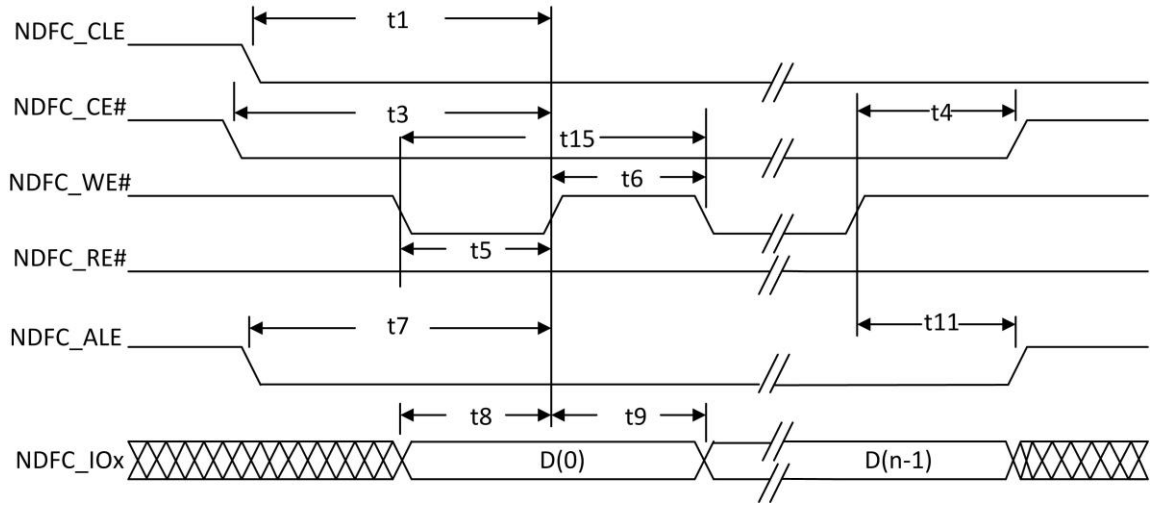


Figure 5-19. Write Data to Flash Cycle Timing

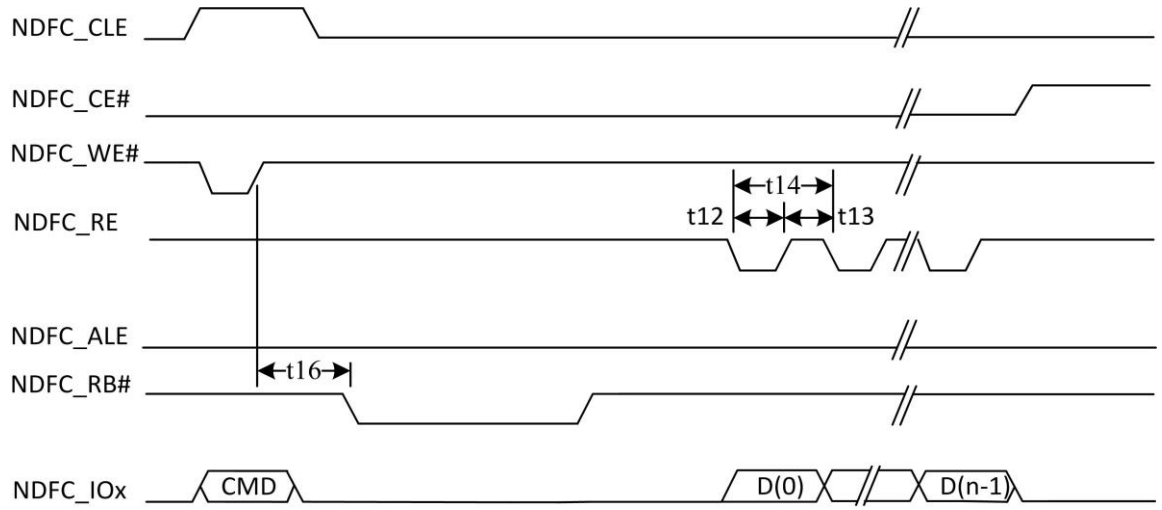


Figure 5-20. Waiting R/B# Ready Timing

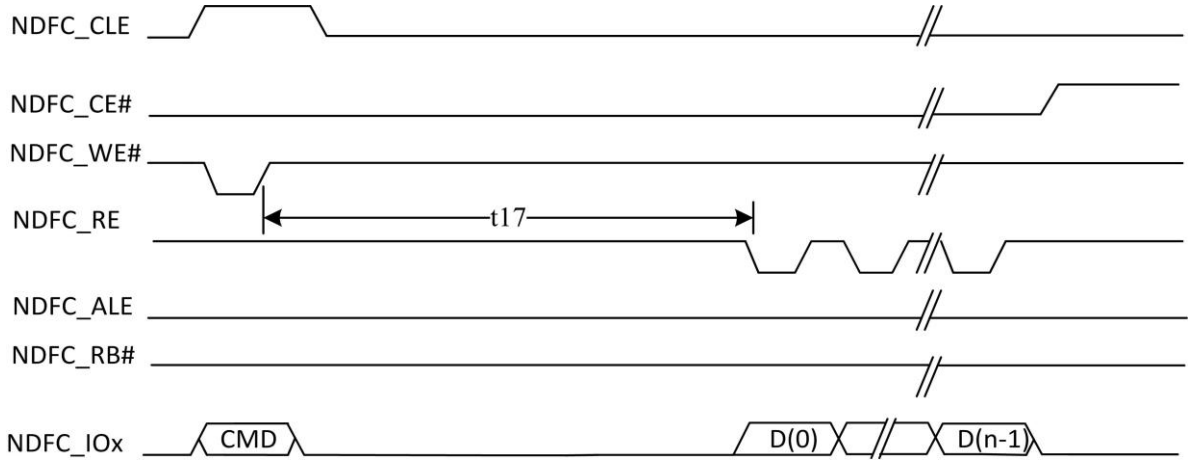


Figure 5-21. WE# High to RE# Low Timing

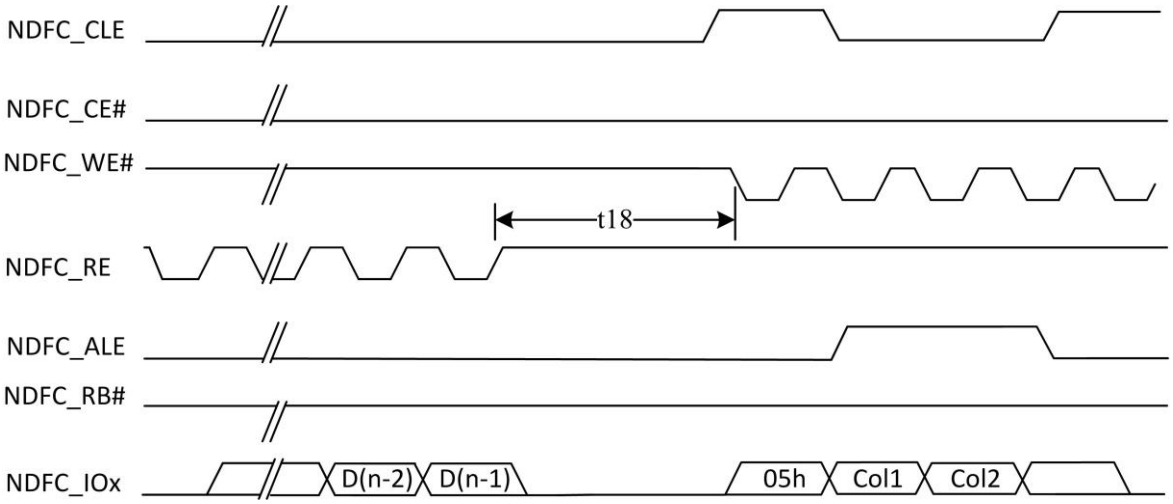


Figure 5-22. RE# High to WE# Low Timing

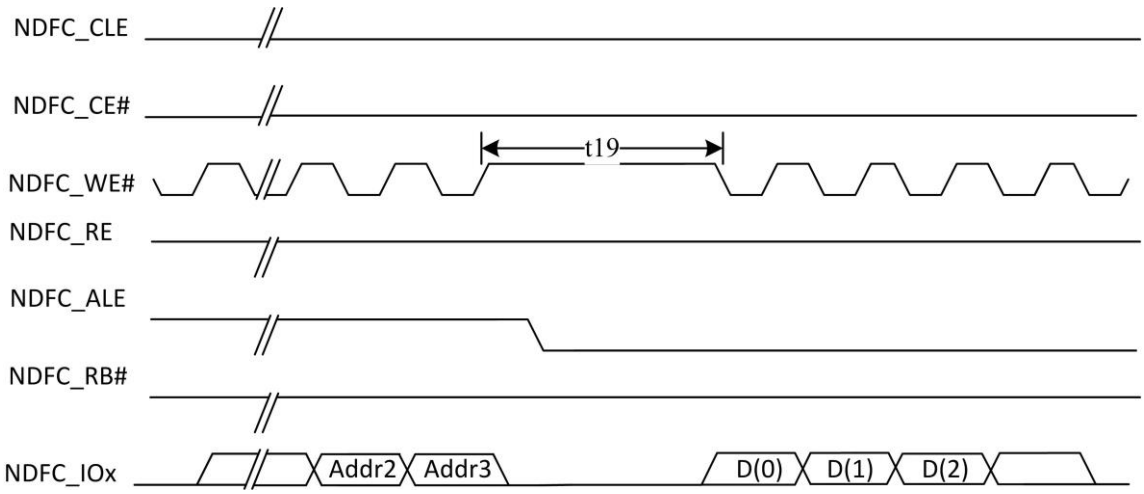


Figure 5-23. Address to Data Loading Timing

Table 5-23. NAND Timing Constants

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T(1)	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns
NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB(2)	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR(3)	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW(4)	ns
Address to Data Loading time	t19	T_ADL(5)	ns
(1):T is the cycle of internal clock. **(2),(3),(4),(5): This values is configurable in nand flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 0*2T/6*2T/14*2T/22*2T, the value of T_RHW could be 4*2T/12*2T/20*2T/28*2T, the value of T_ADL could be 0*2T/6*2T/14*2T/22*2T.**			

5.10.3. SMHC AC Electrical Characteristics

5.10.3.1. SMHC0/SMHC1

(1) SDR Mode(<100MHz)

The contents of this section can be applied to DS, HS, SDR12, SDR25, SDR50, SDR104 (<100MHz) speed mode.

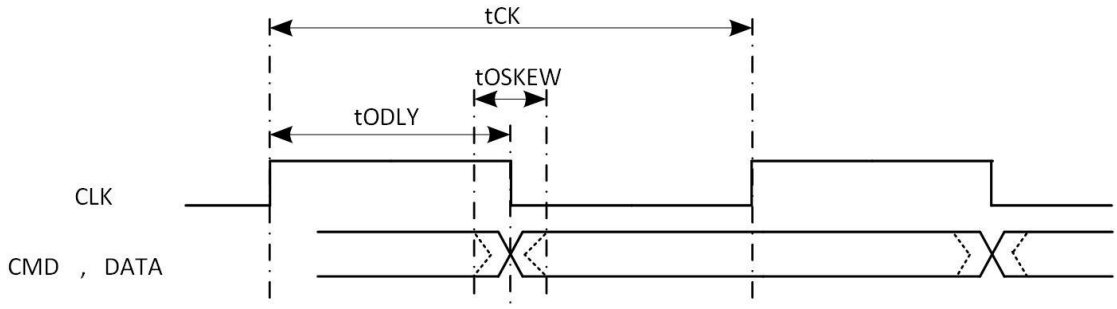


Figure 5-24. SMHC0/1 SDR Mode Output Timing Diagram

Table 5-24. SMHC0/1 SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.625	ns
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20 ns at 50 MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**					

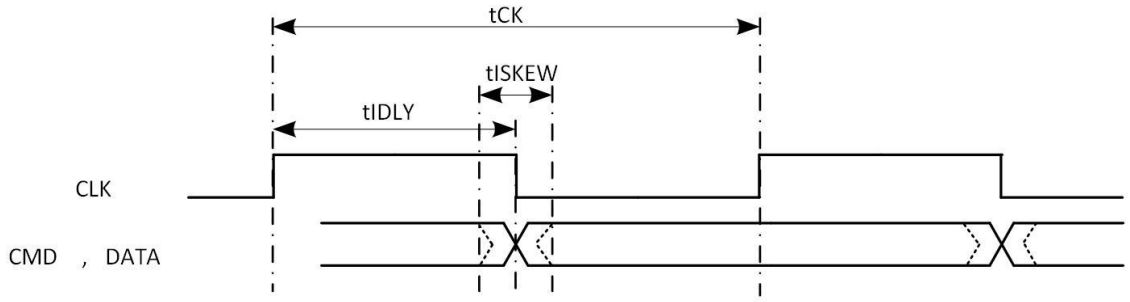


Figure 5-25. SMHC0/1 SDR Mode Input Timing Diagram

Table 5-25. SMHC0/1 SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50 MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns
NOTE (1): The driver strength level of GPIO is 2 for test.					

(2) DDR50 Mode

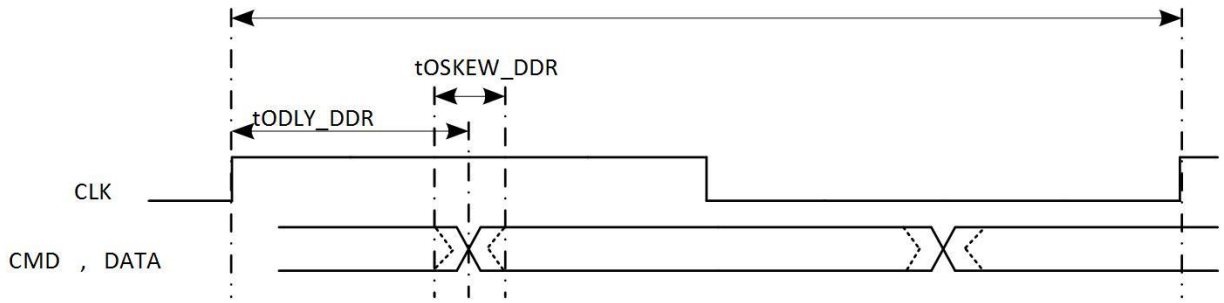


Figure 5-26. SMHC0/1 DDR50 Mode Output Timing Diagram

Table 5-26. SMHC0/1 DDR50 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW_DDR	-	-	0.884	ns
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20 ns at 50 MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**					

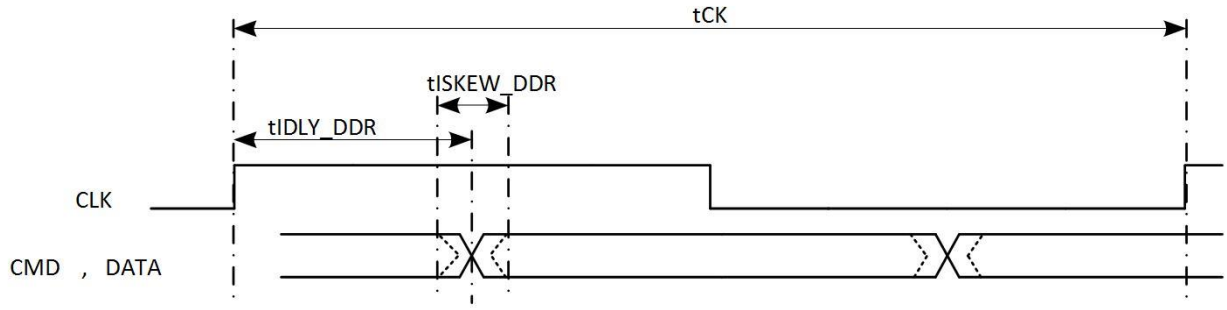


Figure 5-27. SMHC0/1 DDR50 Mode Input Timing Diagram

Table 5-27. SMHC0/1 DDR50 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-c	8.3	ns
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.858	ns
NOTE (1): The driver strength level of GPIO is 2 for test.					

(3) SDR104 Mode(>100MHz)

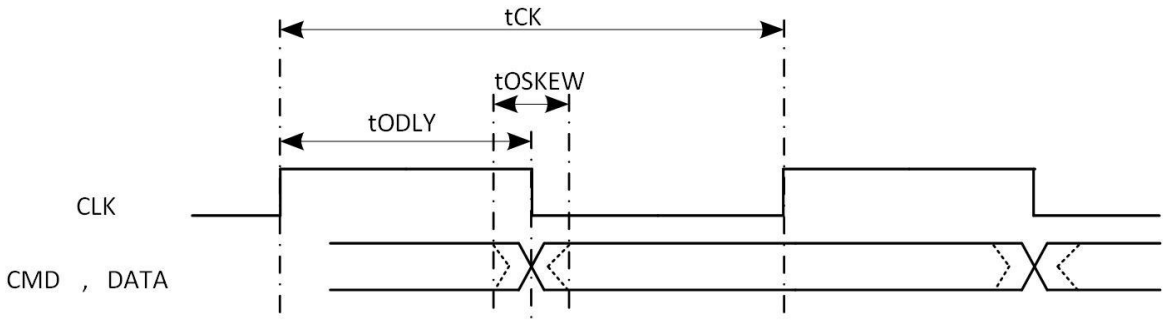


Figure 5-28. SMHC0/1 SDR104 Mode Output Timing Diagram

Table 5-28. SMHC0/1 SDR104 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	-	150	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20 ns at 50 MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**					

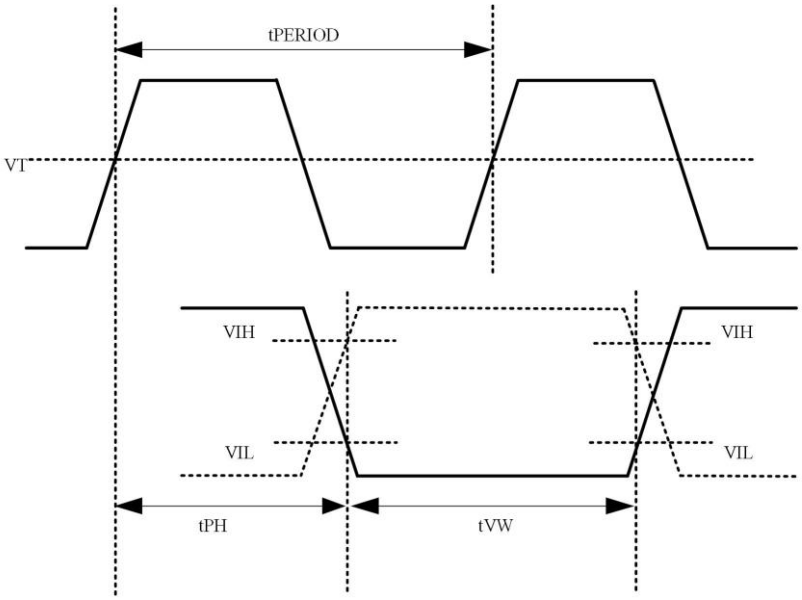


Figure 5-29. SMHC0/1 SDR104 Mode Input Timing Diagram

Table 5-29. SMHC0/1 SDR104 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10 ns at 100 MHz.						

NOTE (2): The driver strength level of GPIO is 3 for test. **NOTE (3): Temperature variation: -20°C.** **NOTE (4): Temperature variation: 90°C.**

5.10.3.2. SMHC2

(1) HS-SDR/HS-DDR Mode

NOTE

IO voltage is 1.8V or 3.3V.

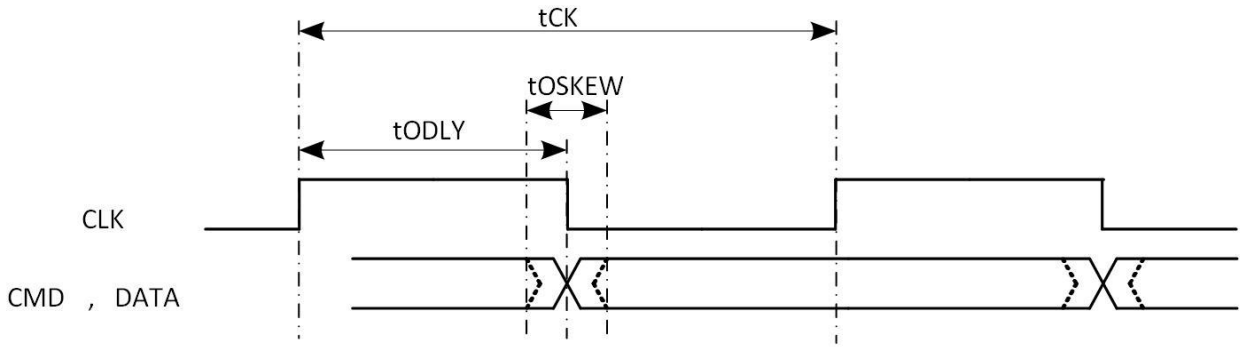


Figure 5-30. SMHC2 HS-SDR Mode Output Timing Diagram

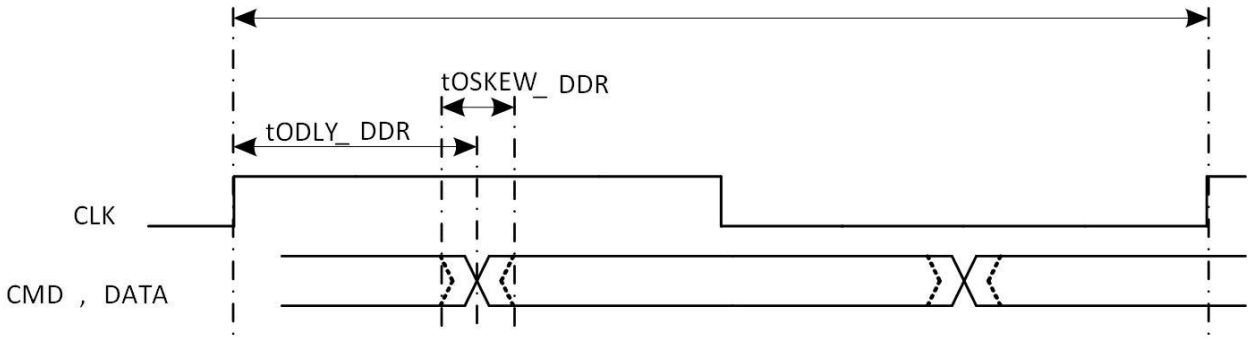


Figure 5-31. SMHC2 HS-DDR Mode Output Timing Diagram

Table 5-30. SMHC2 HS-SDR/HS-DDR Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI	
Data output delay skew time	tOSKEW	-	-	0.884	ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20 ns at 50 MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**						

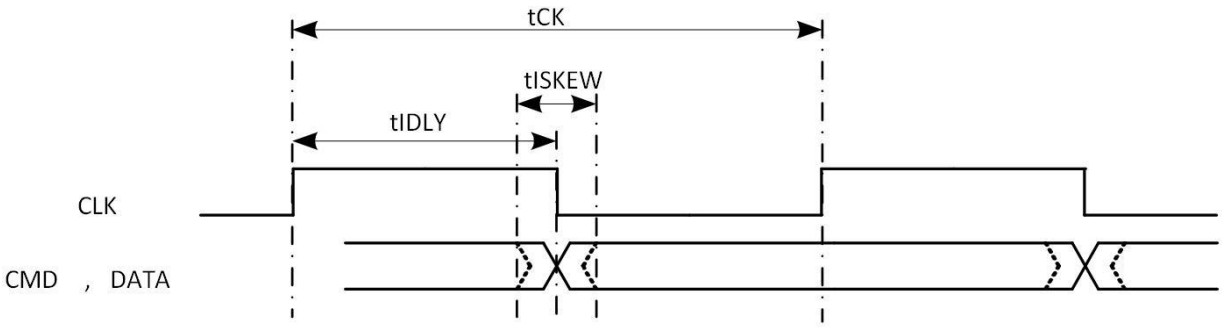


Figure 5-32. SMHC2 HS-SDR Mode Input Timing Diagram

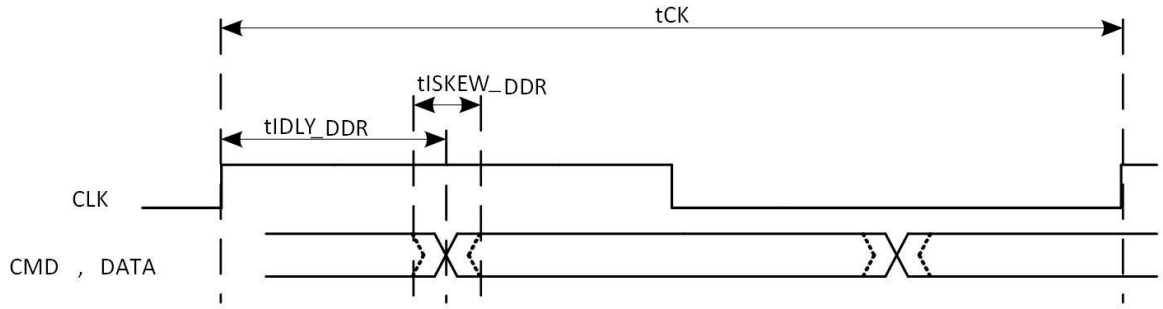


Figure 5-33. SMHC2 HS-DDR Mode Input Timing Diagram

Table 5-31. SMHC2 HS-SDR/HS-DDR Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns	
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	8.3	ns	
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.858	ns	
NOTE (1): The driver strength level of GPIO is 2 for test.						

(2) HS200 Mode

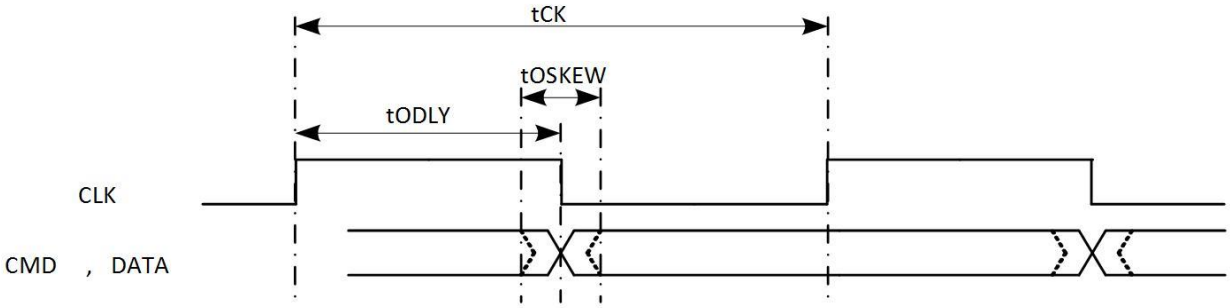


Figure 5-34. SMHC2 HS200 Mode Output Timing Diagram

Table 5-32. SMHC2 HS200 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark

CLK						
Clock frequency	tCK	-	-	150	MHz	
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-	0.884	ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10 ns at 100 MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.**						

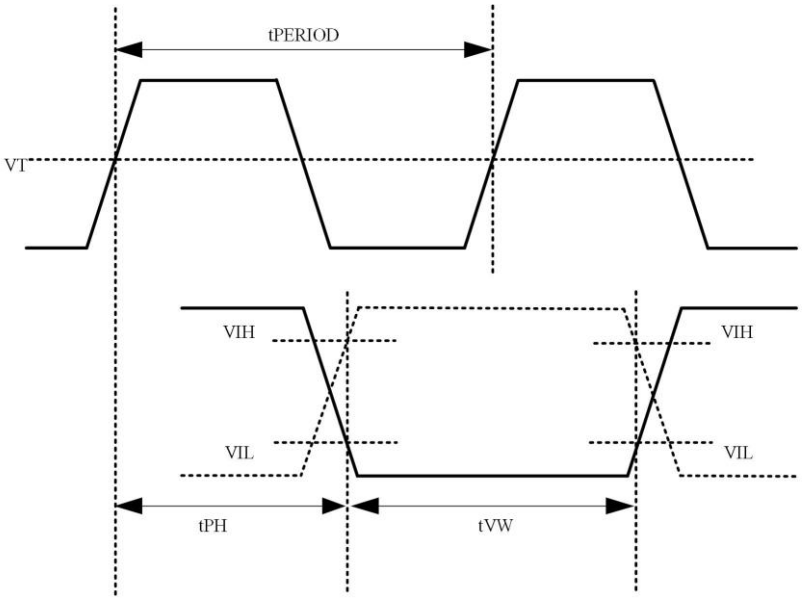


Figure 5-35. SMHC2 HS200 Mode Input Timing Diagram

Table 5-33. SMHC2 HS200 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD, DATA valid window	tVW	0.575	-	-	UI	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10 ns at 100 MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.** **NOTE (3): Temperature variation: -20°C.** **NOTE (4): Temperature variation: 90°C.**						

(3) HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

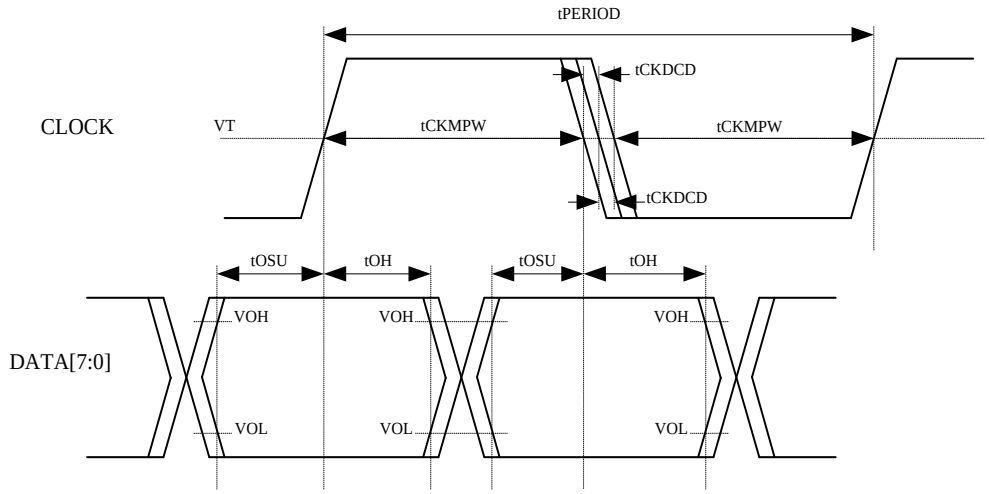


Figure 5-36. SMHC2 HS400 Mode Data Output Timing Diagram

Table 5-34. SMHC2 HS400 Mode Data Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	10	-	-	ns	Max:100MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA(referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10 ns at 100 MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.**						

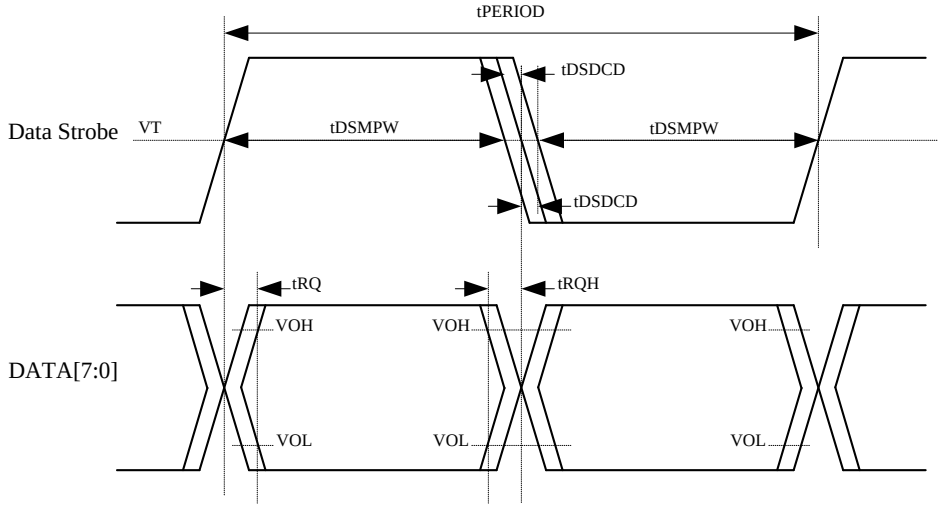


Figure 5-37. SMHC2 HS400 Mode Data Input Timing Diagram

Table 5-35. SMHC2 HS400 Mode Data Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS(Data Strobe)						
DS period	tPERIOD	10	-	-	ns	Max:100MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Output DATA(referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	

Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10 ns at 100 MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.**						

5.11. External Peripheral Electrical Characteristics

5.11.1. LCD AC Electrical Characteristics

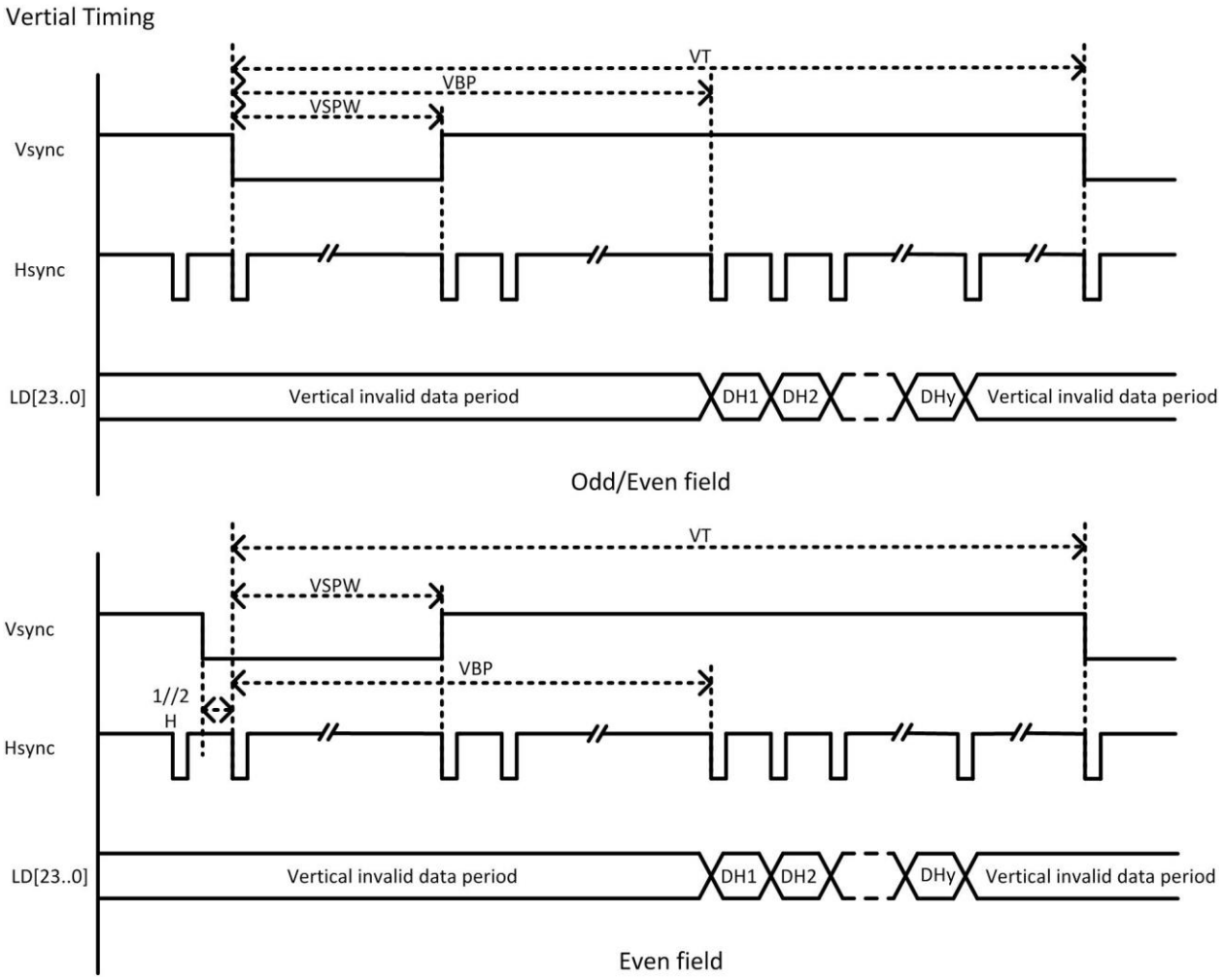


Figure 5-38. HV_IF Interface Vertical Timing

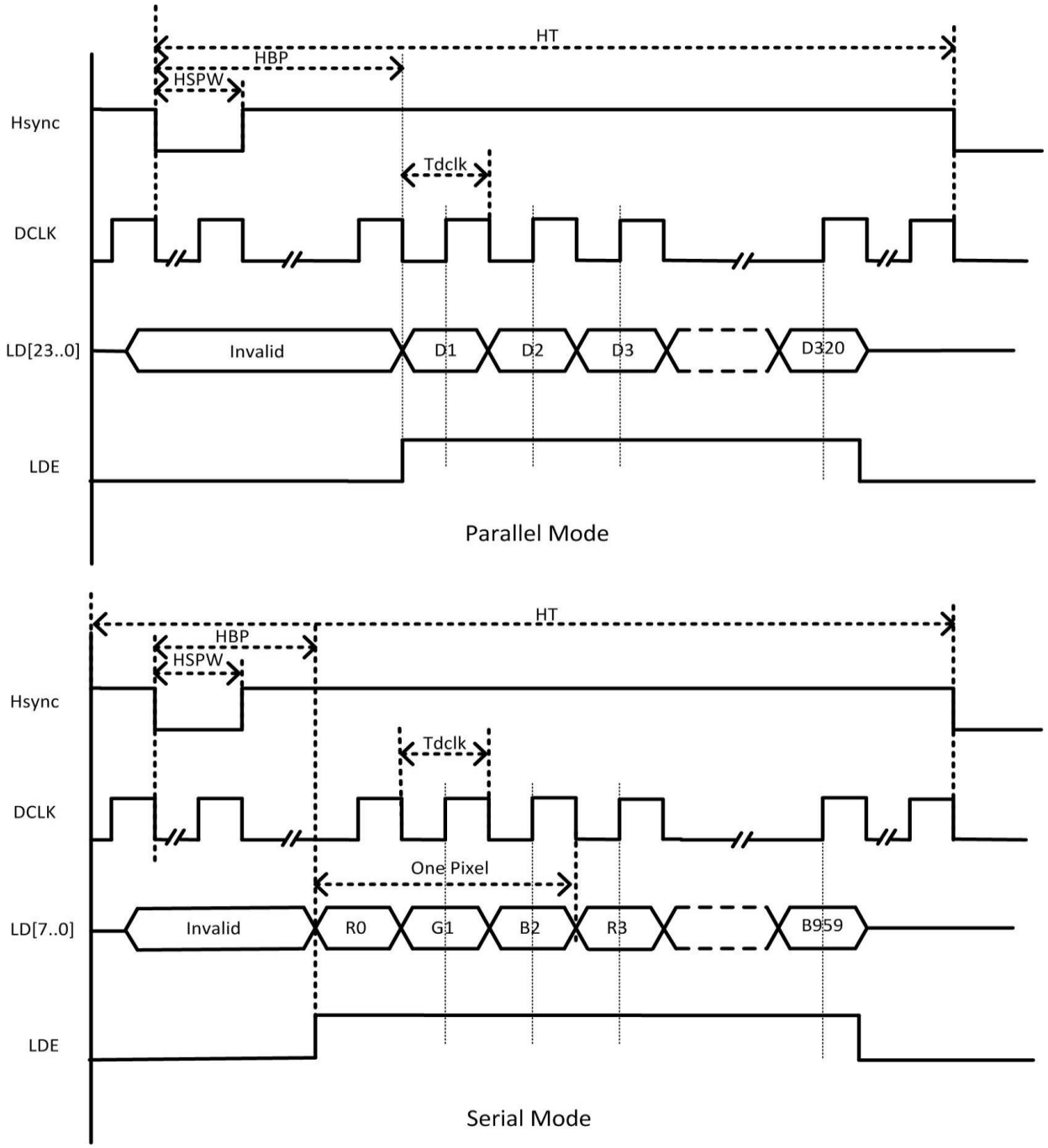


Figure 5-39. HV_IF Interface Horizontal Timing

Table 5-36. LCD HV_IF Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
Hsync period time	tHT	-	HT+1	-	tDCLK
Hsync width	tHSPW	-	HSPW+1	-	tDCLK
Hsync back porch	tHBP	-	HBP+1	-	tDCLK
Vsync period time	tVT	-	VT/2	-	tHT
Vsync width	tVSPW	-	VSPW+1	-	tHT
Vsync back porch	tVBP	-	VBP+1	-	tHT
(1) Vsync: Vertical sync, indicates one new frame. **(2) Hsync: Horizontal sync, indicate one new scan line.** **(3) DCLK: Dot clock, pixel data are sync by this clock.** **(4) LDE: LCD data enable.** **(5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.**					

5.11.2. EMAC AC Electrical Characteristics

5.11.2.1. RMII

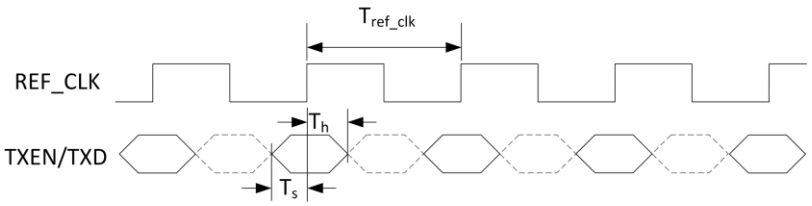


Figure 5-40. RMII Interface Transmit Timing

Table 5-37. RMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference clock period	T_{ref_clk}	-	20	-	ns
TXD/TXEN to REF_CLK setup time	Ts	4	-	-	ns
TXD/TXEN to REF_CLK hold time	Th	2	-	-	ns

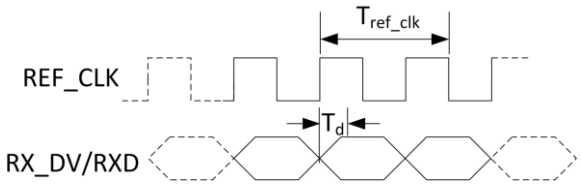


Figure 5-41. RMII Interface Receive Timing

Table 5-38. RMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference clock period	T_{ref_clk}	-	20	-	ns
REF_CLK rising edge to RX_DV/RXD	Td	-	10	12	ns

5.11.2.2. RGMII

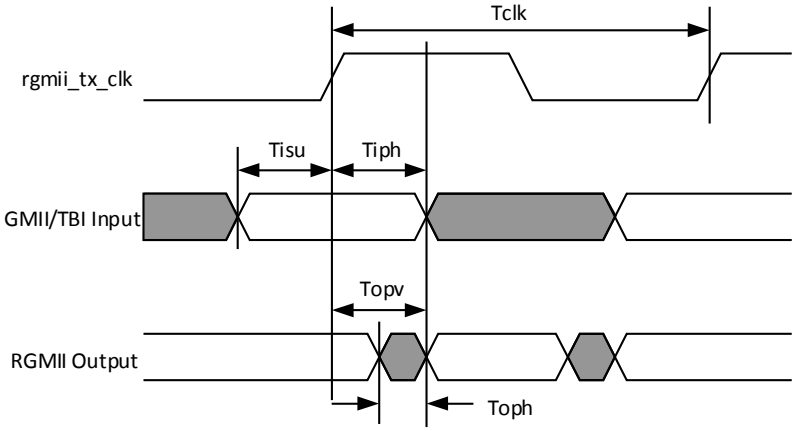


Figure 5-42. RGMII Interface Transmit Timing

Table 5-39. RGMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
rgmii_tx_clk clock period	Tclk	8	-	DC	ns
RGMII/TBI input set up prior to rgmii_tx_clk	Tisu	2.8	-	-	ns
RGMII/TBI input data hold after rgmii_tx_clk	Tiph	0.1	-	-	ns
RGMII output data valid after rgmii_tx_clk	Topv	-	-	0.85	ns
RGMII output data hold after rgmii_tx_clk	Toph	0	-	-	ns

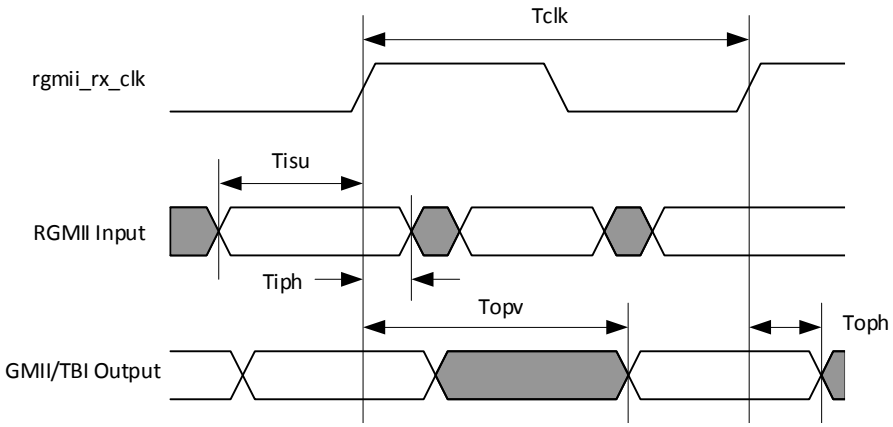


Figure 5-43. RGMII Interface Receive Timing

Table 5-40. RGMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
rgmii_rx_clk clock period	Tclk	8	-	DC	ns
RGMII input set up prior to rgmii_rx_clk	Tisu	2.6	-	-	ns
RGMII input data hold after rgmii_rx_clk	Tiph	0.8	-	-	ns
GMII/TBI input data valid after rgmii_rx_clk	Topv	-	-	5.2	ns
GMII output data hold after rgmii_rx_clk TBI output data hold after rgmii_rx_clk	Toph	0.1 0.5	-	-	ns

5.11.3. CIR-RX AC Electrical Characteristics

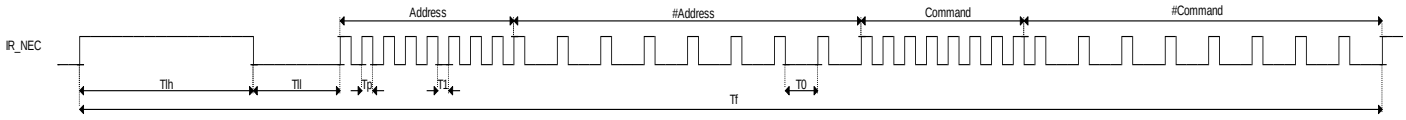


Figure 5-44. CIR-RX Timing

Table 5-41. CIR-RX Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Frame period	Tf	-	67.5	-	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	Tll	-	4.5	-	ms
Pulse time	Tp	-	560	-	us
Logical 1 low time	T1	-	1680	-	us
Logical 0 low time	T0	-	560	-	us

5.11.4. SPI AC Electrical Characteristics

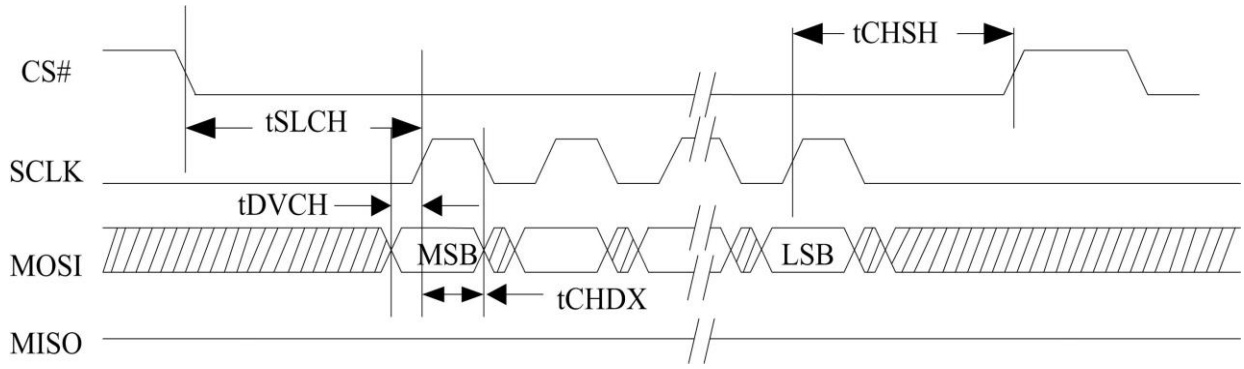


Figure 5-45. SPI MOSI Timing

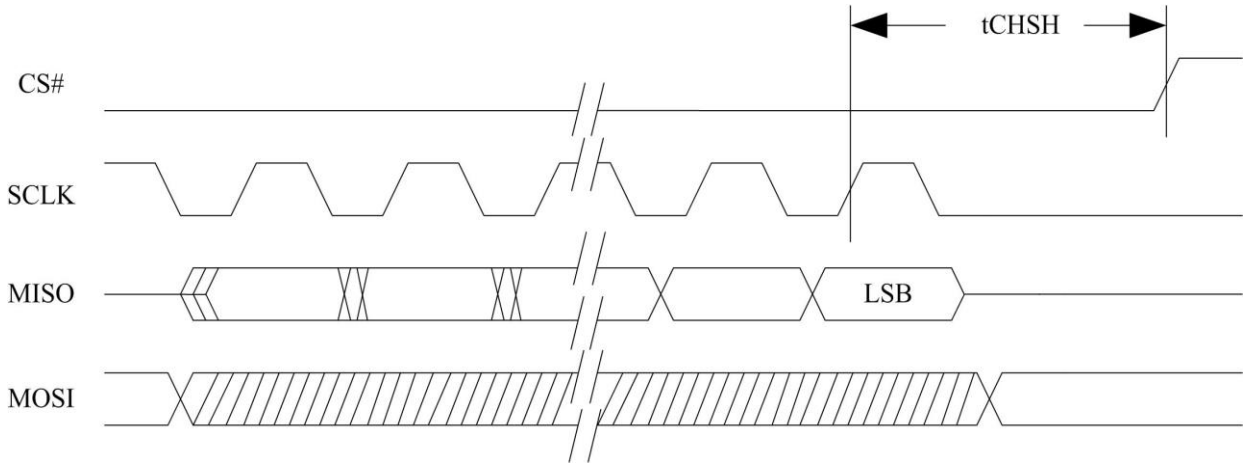


Figure 5-46. SPI MISO Timing

Table 5-42. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	tSLCH	-	2T	-	ns
CS# active hold time	tCHSH	-	2T(1)	-	ns
Data in setup time	tDVCH	-	T/2-3	-	ns
Data in hold time	tCHDX	-	T/2-3	-	ns
NOTE (1):T is the cycle of clock.					

5.11.5. UART AC Electrical Characteristics

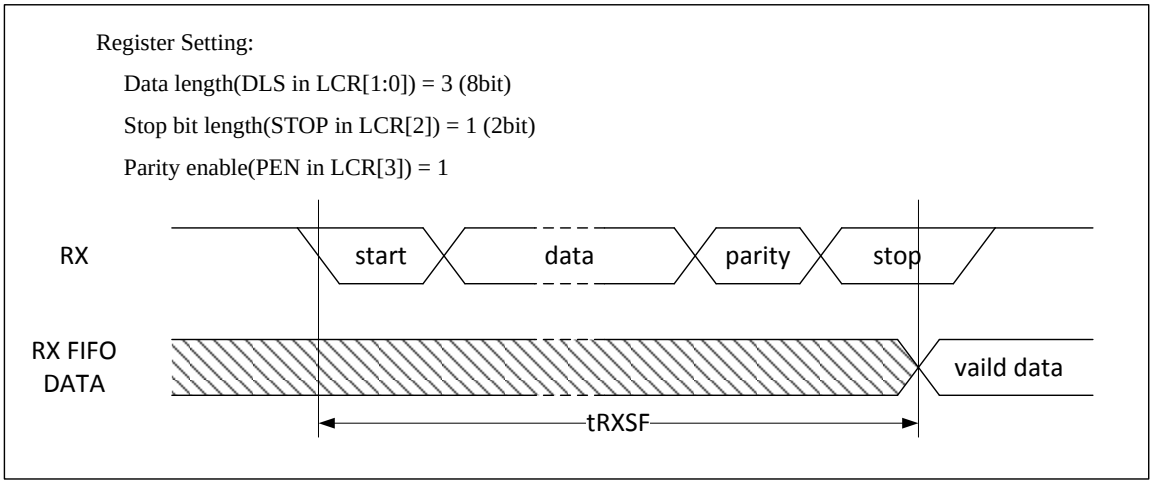


Figure 5-47. UART RX Timing

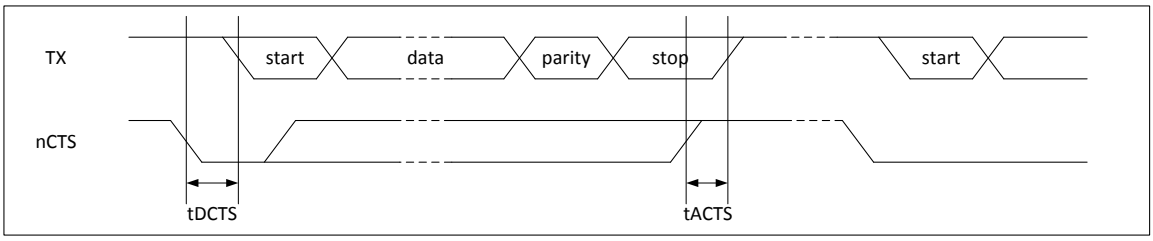


Figure 5-48. UART nCTS Timing

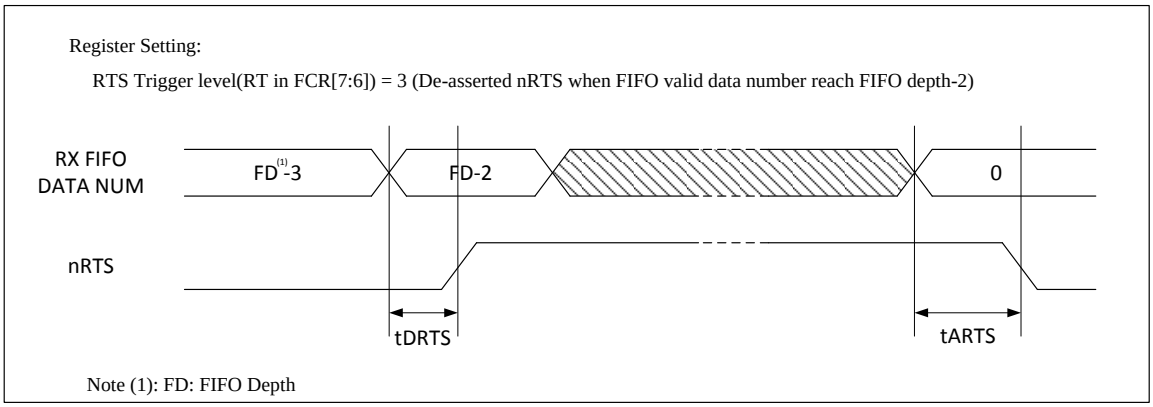


Figure 5-49. UART nRTS Timing

Table 5-43. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
NOTE (1): BRP(Baud-Rate Period).					

5.11.6. TWI AC Electrical Characteristics

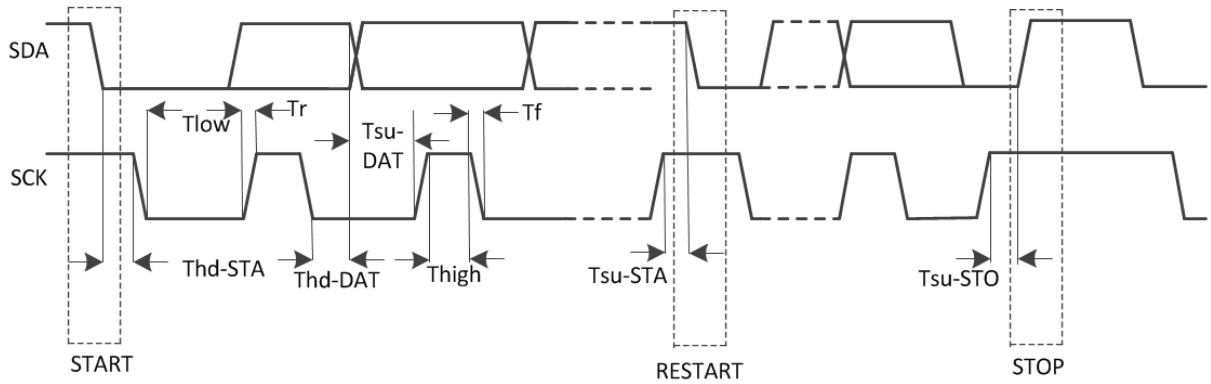


Figure 5-50. TWI Timing

Table 5-44. TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz

Setup time in Start	Tsu-STA	4.7	-	0.6	-	us
Hold time in Start	Thd-STA	4.0	-	0.6	-	us
Setup time in Data	Tsu-DAT	250	-	100	-	ns
Hold time in Data	Thd-DAT	5.0	-	-	-	ns
Setup time in Stop	Tsu-STO	4.0	-	6.0	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	ns
SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

5.11.7. I2S/PCM AC Electrical Characteristics

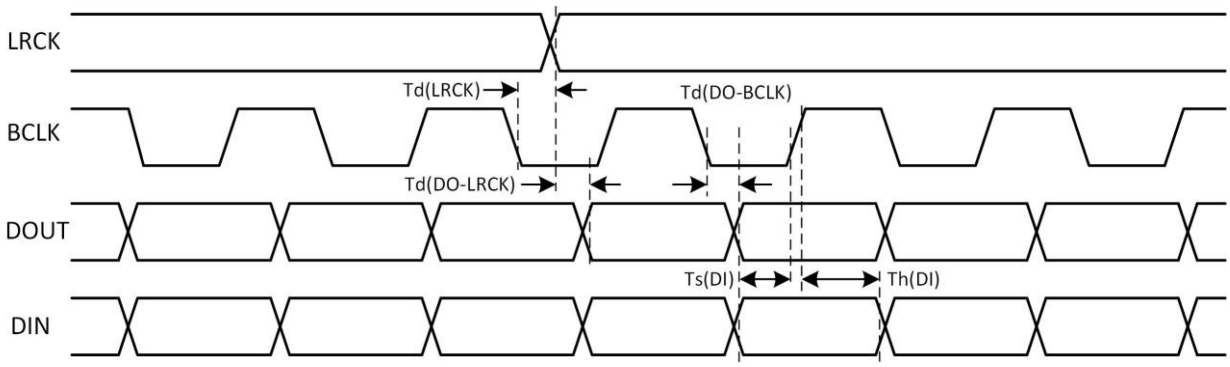


Figure 5-51. I2S/PCM Timing in Master Mode

Table 5-45. I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	8	ns
BCLK fall time	T_f	-	-	8	ns

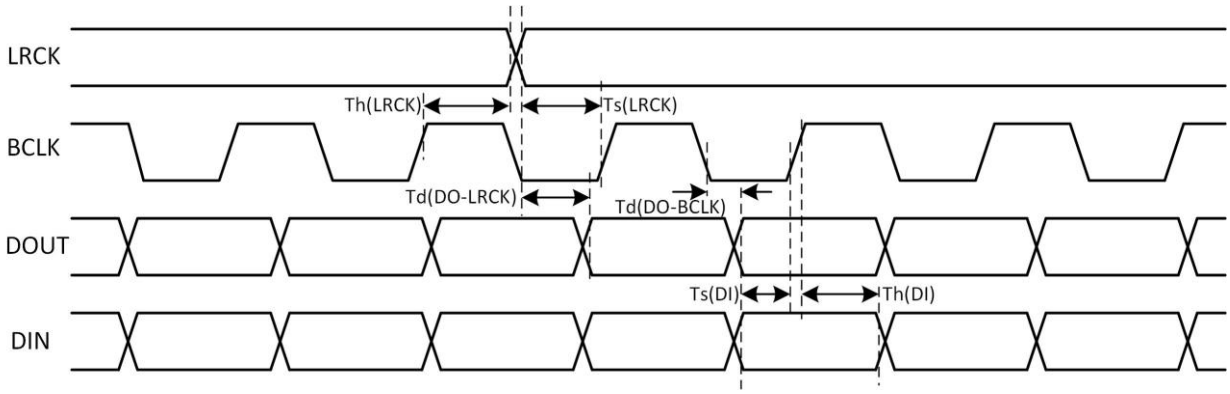


Figure 5-52. I2S/PCM Timing in Slave Mode

Table 5-46. I2S/PCM Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK setup	T_s(LRCK)	4	-	-	ns
LRCK hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns

DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	4	ns
BCLK fall time	T_f	-	-	4	ns

5.11.8. DMIC AC Electrical Characteristics

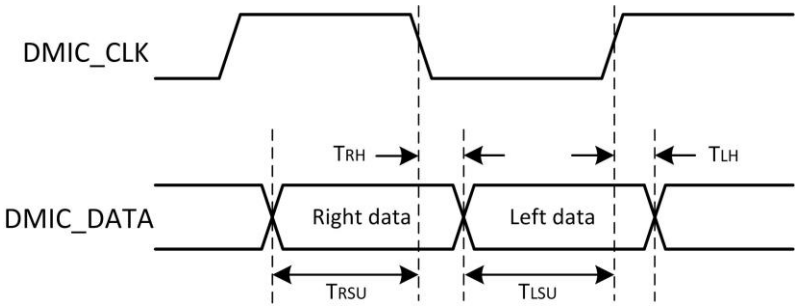


Figure 5-53. DMIC Timing

Table 5-47. DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) setup time to falling edge of DMIC_CLK	T_{RSU}	15	-	-	ns
DMIC_DATA(Right) hold time from falling edge of DMIC_CLK	T_{RH}	0	-	-	ns
DMIC_DATA(Left) setup time to rising edge of DMIC_CLK	T_{LSU}	15	-	-	ns
DMIC_DATA(Left) hold time from rising edge of DMIC_CLK	T_{LH}	0	-	-	ns

5.11.9. OWA AC Electrical Characteristics

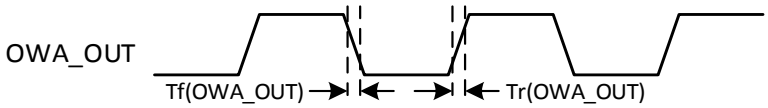


Figure 5-54. OWA Timing

Table 5-48. OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT rise time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT fall time	Tf(OWA_OUT)	-	-	8	ns

5.12. Power-On and Power-Off Sequence

5.12.1. Power-On Sequence

The description of the power on sequence is as follows.

- The consequent steps in power on sequence should not start before the previous step supplies have been stabilized within 90% to 110% of their nominal voltage, unless stated otherwise.
- No sequence requirement between power domains which are grouped as shown in the following example sequence.
- VCC_RTC starts to ramp up first. The other powers cannot be earlier than VCC_RTC.
- VDD_SYS starts to ramp up at least 8 ms later than VCC_RTC.
- VDD_SYS, VCC_DRAM, VDD18_LPDDR, and VPP_DRAM start to ramp up at the same time.
- After all of the default power outputs of the PMIC have finished powering on with a minimum delay of 6 ms, the RESET can be released.
- 24 MHz clock starts oscillating and be stable after the RESET.

Figure 5-55 shows the power on sequence for the R818 device when working with the PMIC AXP305B.

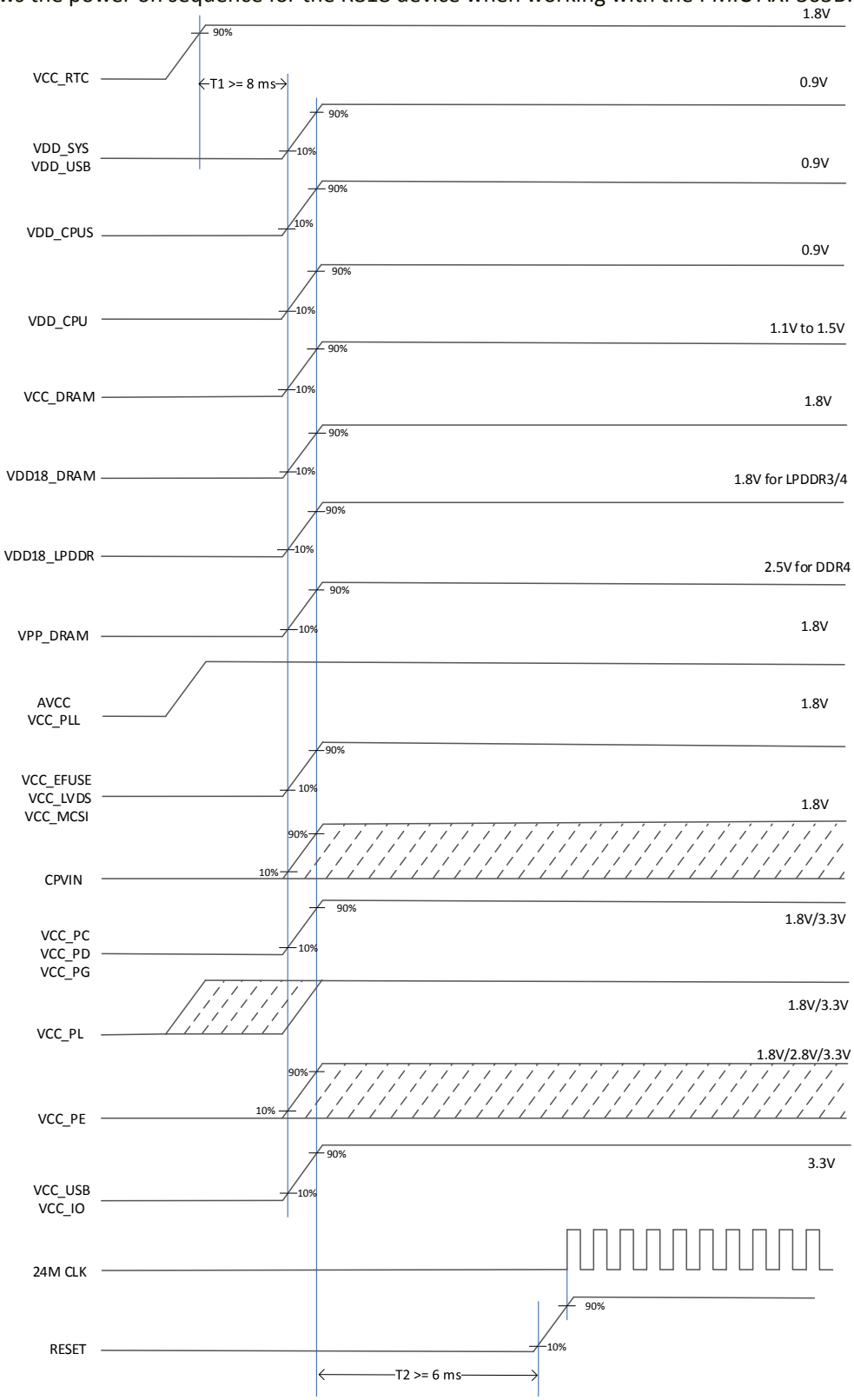


Figure 5-55. R818 Power On Sequence (with AXP305B)

Figure 5-56 shows the power on sequence for the R818 device when working with the PMIC AXP707.

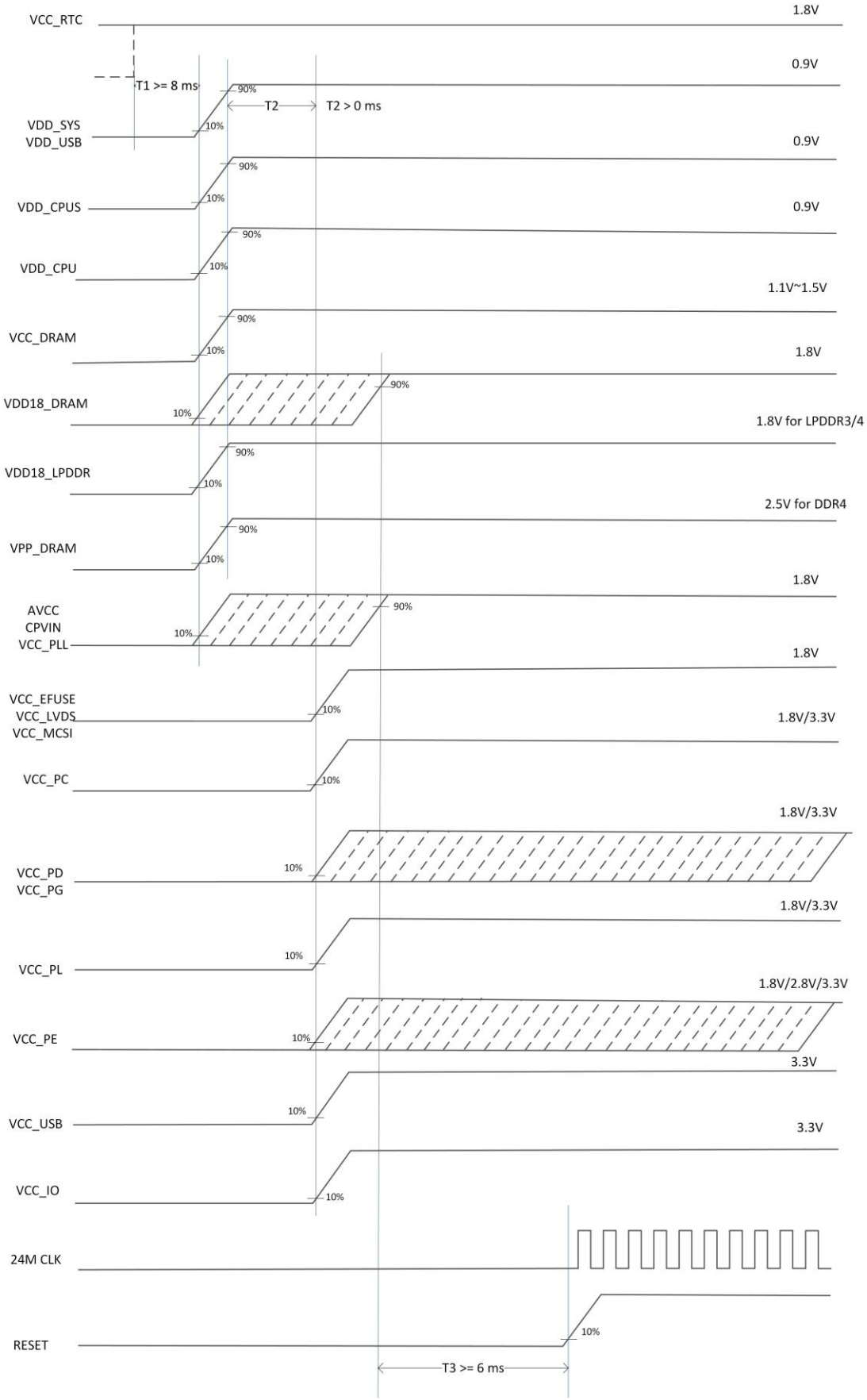


Figure 5-56. R818 Power On Sequence (with AXP707)

5.12.2. Power-Off Sequence

No special restrictions.

6. Package Thermal Characteristics

Table 6-1 shows thermal resistance characteristics for the package used on R818. The following thermal resistance characteristics in Table 6-1 is based on JEDEC JESD51 standard, because the actual system design and temperature could be different with JEDEC JESD51, the simulating result data is a reference only, please prevail in the actual application condition test.

Table 6-1. R818 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	23.45	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	6.46	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	3.01	-	°C/W

7. Pin Assignment

7.1. Pin Map

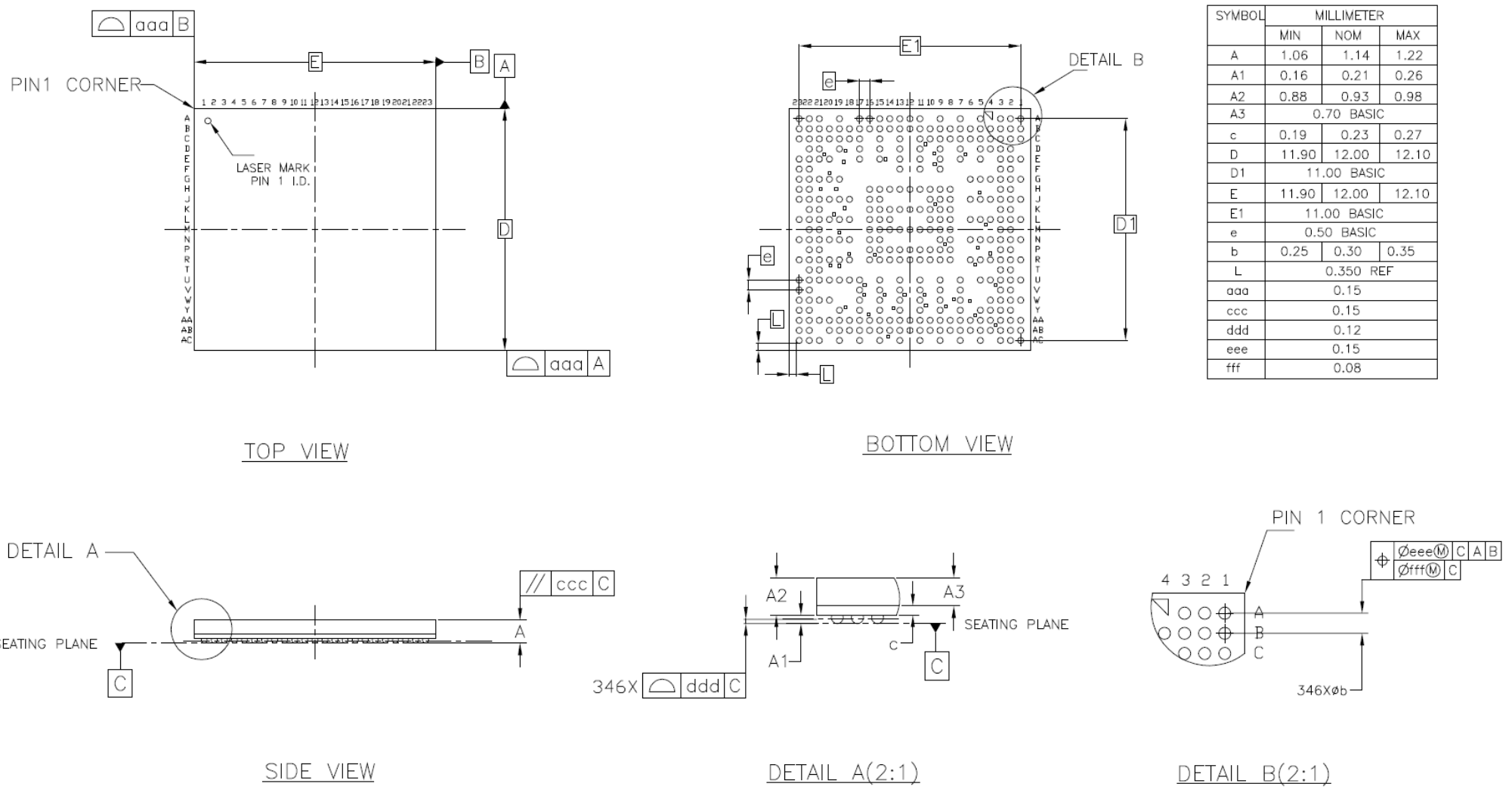
For R818, LFBGA 346 balls, 12 mm x 12 mm body, 0.3 mm ball size, and 0.5 mm ball pitch package is offered. The pin map is illustrated in Figure 7-1 for this package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	PH17	PH12		PH1		FEL		PF2		GPADC1	MICIN2P	MICIN1P	LINEOUTLP	MIC_DET	HPOUTR	HPOUTL		MCSIB_CKN		MCSIA_CKP	MCSIA_CKN	GND	A
B	PH19	PH13	PH15	PH10	PH3	PH2	JTAG_SEL	PF4	PF3	PF0	GPADC0	MICIN2N	MICIN1N	LINEOUTLN	MBIAS	HBIAS	HPOUTFB	MCSIB_D1N	MCSIB_CKP	MCSIB_D0N	MCSIA_D2N	MCSIA_D3N	MCSIA_D3P	B
C	PH14	PH18	PH16	PH7	PH5	PH4	PH0	PF5	PF1	PF6	HP_DET		CPVIN		CPVDD		GND	MCSIB_D1P	GND	MCSIB_D0P	MCSIA_D2P	MCSIA_D1N	MCSIA_D1P	C
D		PB5	PB4	PB1	PB3		PH11		PH9		AGND		AVCC		VEE		VCC_MCSI		PE3		MCSIA_D0N	MCSIA_D0P		D
E	PB8	PB7	PB6		PB0		VCC_IO		PH8		LRADC		VRA2		CPVEE		VCC_PE			PE1	PE9	PE7	PE0	E
F		PB9	PB10						PH6		BOOT_SEL		VRA1									PE6	PE8	F
G	PG2	PG4	PG3	PB2	PG11	PG12													PE5	PE2	PE4	USB0_DM	USB0_DP	G
H		PG1	PG5					GND	GND	GND	GND	VDD_SYSFB	VDD_SYS	VDD_SYS	VDD_SYS	VDD_SYS						USB1_DM	USB1_DP	H
J	PG10	PG0	GND	PG13	PG7	VCC_PG		GND	GND	GND					GND	VDD_SYS		VDD_USB	VCC_EFUSE	VCC_USB	GND	PC11	PC15	J
K		PG6	PG8					VDD_CPU	VDD_CPU	GND	GND	GND	GND	GND	GND	GND					PC14	PC10		K
L	PL8	PL7	PG9	VCC_PL	VCC_RTC	PL1		VDD_CPU	GND	GND				GND	GND	GND		VCC_PC	PC12	PC16	PC13	PC6	PC4	L
M		PL11	PL9					VDD_CPU	GND	GND	GND	GND	GND	GND	GND	GND					PC2	PC3		M
N	PL3	PL6	PL5	VDD_CPUS	PL0	VCC_PLL		VDD_CPU	GND						GND	GND		VCC_LVDS0	PC0	PC7	PC9	GND	PC5	N
P		RTC_VIO	PL2					VDD_CPUFB	GND	GND	GND	GND	GND	GND	GND	GND					PC8	PC1		P
R	DXOUT	DXIN	REFCLK_OUT	PL4	NMI	RESET		GND	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VDD18_DRAM	GND		VCC_PD	PD23	PD22	GND	PD10	PD11	R
T		X32KIN	X32KOUT																		PD12	PD13		T
U	DXLDO_OUT	WREQIN	X32KFOUT	PL10	GND		SDQM0		GND		SDQM3		SA4		SA3		SRST	PD21	PD20	PD17	PD16	PD14	PD15	U
V		GND	GND				SDQ1		SDQ26		SDQ31		GND		GND		GND					PD0	PD1	V
W	SDQ4	SDQ6	SDQ7	SDQ5			SDQ3		SDQ25		SDQ29		SA5		SBA0		SA7			PD19	PD18	PD2	PD3	W
Y		SDQS0P	SDQS0N	GND	SDQ2		SDQ0		SDQ27		SDQ24		SA6		SBA1		SA12		SZQ			PD6	PD7	Y
AA	SDQ8	SDQ15	SDQ14	SDQ13	SDQM1	SDQ22	GND	SDQ18	SDQM2	SDQS3N	GND	SA2	GND	SCKP	SCKE1	SCKE0	SA0	GND	SA9	SACT	SODT0	PD4	PD5	AA
AB	SDQ10	SDQS1P	SDQ11	SDQ9	SDQ21	SDQ23	SDQS2P	SDQ19	SDQ17	SDQS3P	SDQ30	SA15	SA1	SCKN	SA16	SA13	SBG0	SA8	SCS1	SBG1		PD8	PD9	AB
AC	GND	SDQS1N	SDQ12		SDQ20		SDQS2N		SDQ16		SDQ28		SA14		SCS0		SA10		SA11		SODT1	GND	GND	AC

Figure 7-1. R818 Pin Map

7.2. Package Dimension

Figure 7-2 shows the top, bottom, and side views of R818 package dimension.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.06	1.14	1.22
A1	0.16	0.21	0.26
A2	0.88	0.93	0.98
A3	0.70 BASIC		
c	0.19	0.23	0.27
D	11.90	12.00	12.10
D1	11.00 BASIC		
E	11.90	12.00	12.10
E1	11.00 BASIC		
e	0.50 BASIC		
b	0.25	0.30	0.35
L	0.350 REF		
aaa	0.15		
ccc	0.15		
ddd	0.12		
eee	0.15		
fff	0.08		

Figure 7-2. R818 Package Dimension

8. Carrier, Storage and Baking Information

8.1. Carrier

8.1.1. Matrix Tray Information

Table 8-1 shows the R818 matrix tray carrier information.

Table 8-1. Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315 mm x 136 mm x 7.62 mm	168 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion(Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right:12 mm x 180 mm x 85 mm Front-Back:12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

HIC:

Desiccant:

RoHS symbol:

Product label:

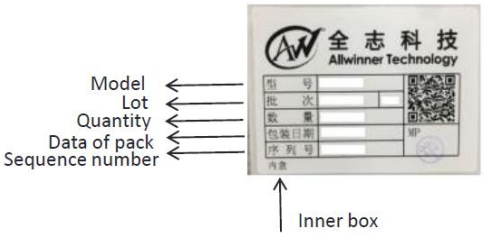


Table 8-2 shows the R818 packing quantity.

Table 8-2. Packing Quantity Information

Sample	Size(mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
R818	12 x 12	168	10	1680	6	10080

Figure 8-1 shows tray dimension drawing of the R818.

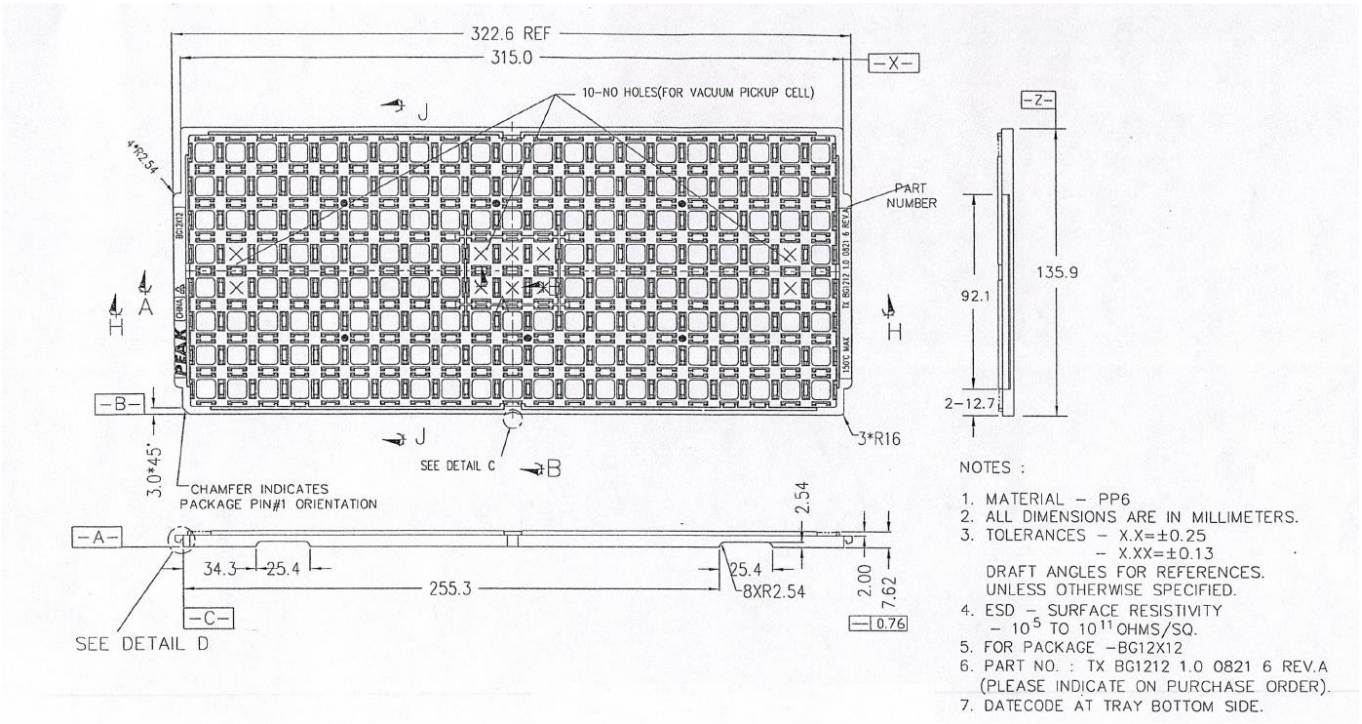


Figure 8-1. Tray Dimension Drawing

8.2. Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

8.2.1. Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL is defined in Table 8-3.

Table 8-3. MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label(TOL)	≤30°C / 60%RH

NOTE

The R818 device samples are classified as MSL3.

8.2.2. Bagged Storage Conditions

The shelf life of the R818 device samples is defined in Table 8-4.

Table 8-4. Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH

Shelf life	12 months

8.2.3. Out-of-bag Duration

It is defined by the device MSL rating, the out-of-bag duration of the R818 are as follows.

Table 8-5. Out-of-bag Duration

Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Moisture sensitive level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

8.3. Baking

It is not necessary to bake the R818 if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake the R818 if any conditions specified in Section 8.2.2 and Section 8.2.3 have been exceeded.

It is necessary to bake the R818 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the sample baking should not exceed 3 times, and the tray baking should not exceed 1 time, with a distortion risk.

9. Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, please contact with Allwinner FAE.

The appropriate reflow conditions are defined in Figure 9-1 and Table 9-1.

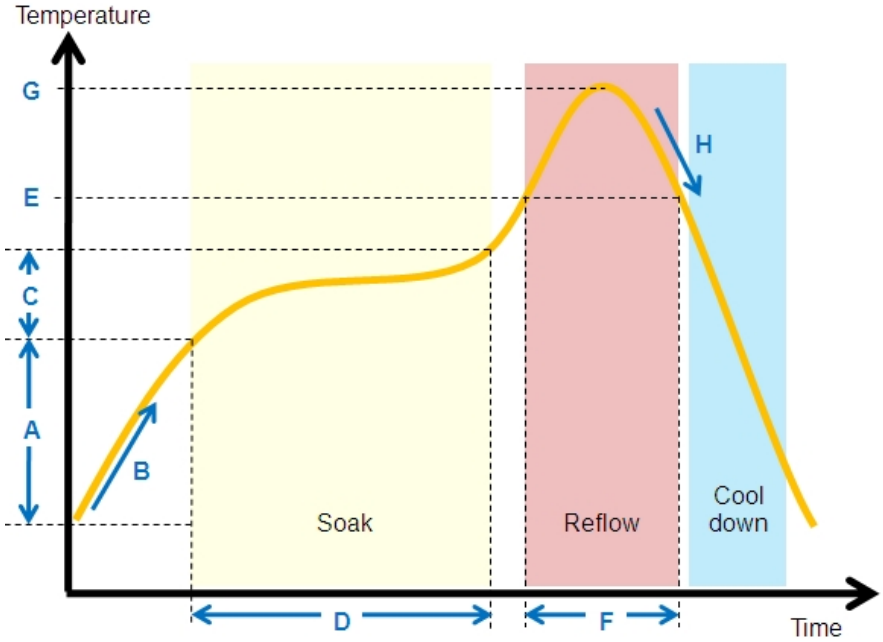


Figure 9-1. Lead-free Reflow Profile

Table 9-1. Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

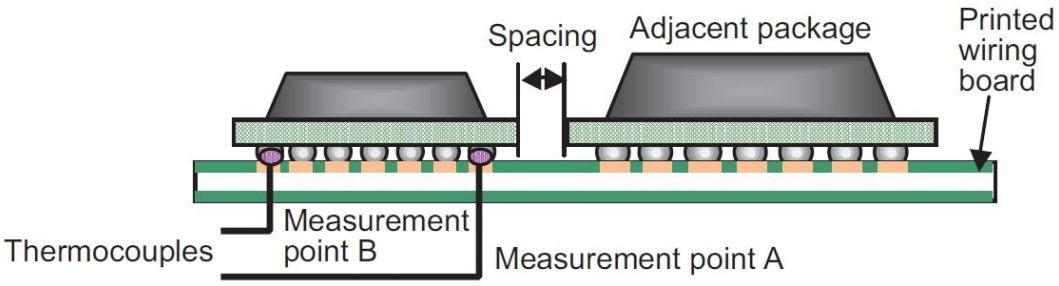


Figure 9-2. Measuring the Reflow Soldering Process

NOTE

To measure the temperature of QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10. FT and IQC Test

10.1. FT Test

FT test includes two parts, module verification and linux system testing. For module verification, it verifies the logic function of each module; for linux system testing, it mainly tests CPU, DDR, memory test and linpack, etc. The linux system testing can cover areas where module verification does not cover, with the goal of increasing coverage as much as possible.

10.2. IQC Test

IQC test system is used for sampling inspection before delivery, it is the final test for chip shipment before delivery to the customer. IQC test system includes QA test and QC test.

10.2.1. QA Test

QA test is a testing for each function module of chip based on Android system, which can judge whether chip can reach production standard by system total running results, single module testing fluency.

10.2.2. QC Test

QC test is used to test each module code booting from Nand flash, and run schedule by using PC control code, then read the return value of each module testing. If the return value is PASS, then continue to perform the next module testing; or else stop testing and remind the testing module FAIL.

11. Part Marking

Figure 11-1 shows the R818 marking.

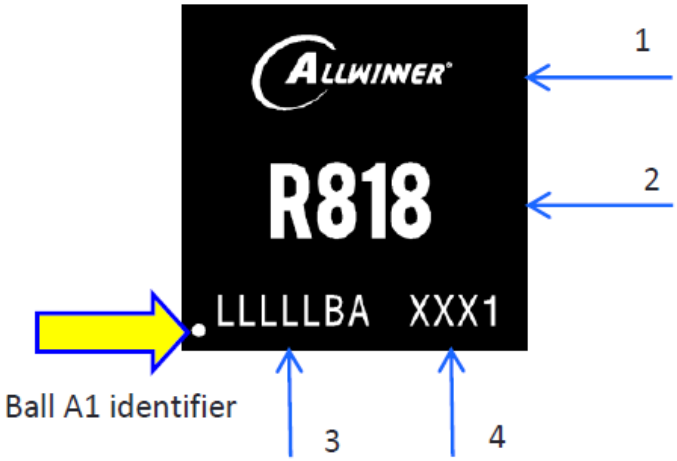


Figure 11-1. R818 Marking

Table 11-1 describes the R818 marking definitions.

Table 11-1. R818 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	R818	Product name	Fixed
3	LLLLLBA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

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