







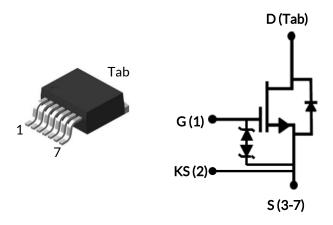








JJ4SC075011B7S



Part Number	Package	Marking
UJ4SC075011B7S	D ² PAK-7L	UJ4SC075011B7S







750V-11m Ω SiC FET

Rev. A, January 2022

Description

The UJ4SC075011B7S is a 750V, $11m\Omega$ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D²PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance R_{DS(on)}: 11mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 274nC
- ◆ Low body diode V_{FSD}: 1.1V
- ◆ Low gate charge: Q_G =75nC
- ◆ Threshold voltage V_{G(th)}: 4.5V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected, HBM class 2
- D²PAK-7L package for faster switching, clean gate waveforms

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating















Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Cata	V _{GS}	DC	-20 to +20	V
Gate-source voltage		AC (f > 1Hz)	-25 to +25	V
Continuous drain current ¹	1	T _C = 25°C	104	Α
Continuous drain current	I _D	T _C = 100°C	75	Α
Pulsed drain current ²	I _{DM}	T _C = 25°C	300	Α
Single pulsed avalanche energy ³	E _{AS}	$L=15mH$, $I_{AS}=4.5A$	151	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \leq 500V$	100	V/ns
Power dissipation	P _{tot}	T _C = 25°C	357	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 1	245	°C

- 1. Limited by $T_{J,max}$
- 2. Pulse width t_p limited by $T_{J,max}$
- 3. Starting $T_J = 25^{\circ}C$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Тур	Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.33	0.42	°C/W













Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions		Units		
rai ametei			Min	Тур	Max	UIIILS
Drain-source breakdown voltage	BV _{DS}	V_{GS} =0V, I_D =1mA	750			V
Total drain leakage current		V _{DS} =750V, V _{GS} =0V, T _J =25°C		3.5	60	
	I _{DSS}	V _{DS} =750V, V _{GS} =0V, T _J =175°C		45	45	μΑ
Total gate leakage current	I _{GSS}	V _{DS} =0V, T _J =25°C, V _{GS} =-20V / +20V		2	±20	μА
Drain-source on-resistance	R _{DS(on)}	V_{GS} =12V, I_{D} =60A, T_{J} =25°C		11	14.2	
		V _{GS} =12V, I _D =60A, T _J =125°C		18.4		mΩ
		V _{GS} =12V, I _D =60A, T _J =175°C		24.2		
Gate threshold voltage	$V_{G(th)}$	V_{DS} =5V, I_{D} =10mA	3.5	4.5	5.5	V
Gate resistance	R _G	f=1MHz, open drain		2.3		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions		Units		
Par ameter			Min	Тур	Max	Units
Diode continuous forward current ¹	I _S	T _C < 35°C			104	Α
Diode pulse current ²	I _{S,pulse}	T _C =25°C			300	Α
Forward voltage	V_{FSD}	V _{GS} =0V, I _F =30A, T _J =25°C		1.1	1.24	V
		V _{GS} =0V, I _F =30A, T _J =175°C		1.2		- v
Reverse recovery charge	Q _{rr}	V_R =400V, I_F =60A, V_{GS} =0V, R_{G_EXT} =30 Ω		274		nC
Reverse recovery time	t _{rr}	di/dt=2500A/μs, T _J =25°C		18.5		ns
Reverse recovery charge	Q _{rr}	V_R =400V, I_F =60A, V_{GS} =0V, R_{G_EXT} =30 Ω		290		nC
Reverse recovery time	t _{rr}	di/dt=2500A/μs, Τ _J =150°C		20		ns















Typical Performance - Dynamic

Parameter	Symbol Test	Took Conditions	Value			
		Test Conditions	Min	Тур	Max	Units
Input capacitance	C_{iss}	V _{DS} =400V, V _{GS} =0V		3245		
Output capacitance	C_{oss}	f=100kHz		178		pF
Reverse transfer capacitance	C_{rss}	f=100kHz		1.2		
Effective output capacitance, energy related	$C_{oss(er)}$	V _{DS} =0V to 400V, V _{GS} =0V		225		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS} =0V to 400V, V_{GS} =0V		470		pF
C _{OSS} stored energy	E _{oss}	V _{DS} =400V, V _{GS} =0V		18		μЈ
Total gate charge	Q_{G}	V _{DS} =400V, I _D =60A,		75		
Gate-drain charge	Q_{GD}	$V_{DS} = -0V \text{ to } 15V$		13		nC
Gate-source charge	Q_{GS}	VGS - 0 V to 13 V		22		
Turn-on delay time	$t_{d(on)}$			17.6		- ns
Rise time	t _r	Notes 4 and 5, V _{DS} =400V, I _D =60A, Gate		22.4		
Turn-off delay time	t _{d(off)}	v_{DS} =400V, I_D =60A, Gate Driver =0V to +15V,		65		
Fall time	t _f	Turn-on $R_{G,EXT}=1\Omega$,		12.8		
Turn-on energy including R _S energy	E _{ON}	Turn-off $R_{G,EXT}$ =5 Ω , inductive Load, FWD:		173		 μJ
Turn-off energy including R _S energy	E _{OFF}	same device with $V_{GS} = 0V$		132		
Total switching energy	E _{TOTAL}	and $R_G = 5\Omega$, RC snubber: $R_S = 5\Omega$ and $C_S = 440$ pF, $T_1 = 25$ °C		305		
Snubber R _S energy during turn-on	E _{RS_ON}			11		
Snubber R _S energy during turn-off	E _{RS_OFF}			37		
Turn-on delay time	t _{d(on)}			18		ns
Rise time	t _r	Notes 4 and 5,		25		
Turn-off delay time	t _{d(off)}	$V_{DS}\!=\!400V, I_{D}\!=\!60A, Gate$ $Driver=\!0V\ to +\!15V,$ $Turn-on\ R_{G,EXT}\!=\!1\Omega,$ $Turn-off\ R_{G,EXT}\!=\!5\Omega,$ inductive Load, FWD: same device with $V_{GS}\!=\!0V$ and $R_{G}\!=\!5\Omega, RC\ snubber:$ $R_{S}\!=\!5\Omega\ and\ C_{S}\!=\!440pF,$ $T_{J}\!=\!150^{\circ}C$		68		
Fall time	t _f			13.6		
Turn-on energy including R _S energy	E _{ON}			203		
Turn-off energy including R _S energy	E _{OFF}			145		
Total switching energy	E _{TOTAL}			348		μJ
Snubber R _S energy during turn-on	E _{RS_ON}			11		
Snubber R _S energy during turn-off	E _{RS_OFF}			37		

^{4.} Measured with the switching test circuit in Figure 26.

^{5.} In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.





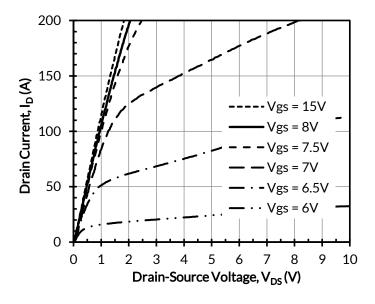








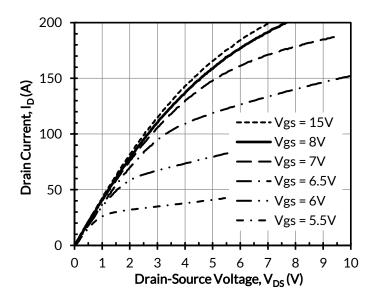




200 150 Drain Current, I_D (A) Vgs = 15V 100 Vgs = 8V Vgs = 7.5V - Vgs = 7V 50 **-** Vgs = 6.5V Vgs = 6V 0 10 0 1 2 5 Drain-Source Voltage, $V_{DS}(V)$

Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250 μ s

Figure 2. Typical output characteristics at $T_J = 25$ °C, $tp < 250\mu s$



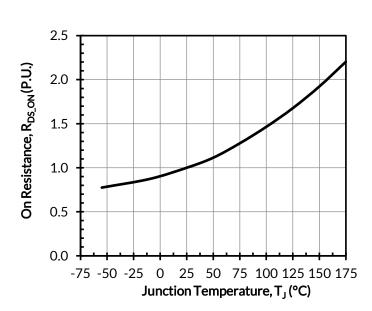


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250 μ s

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 60A



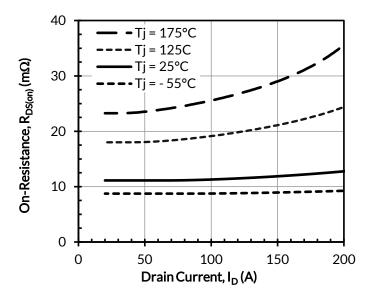












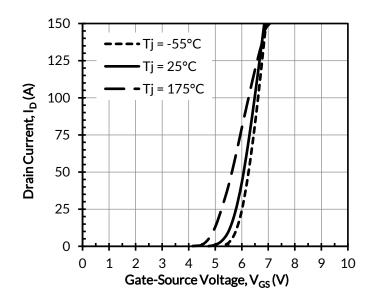
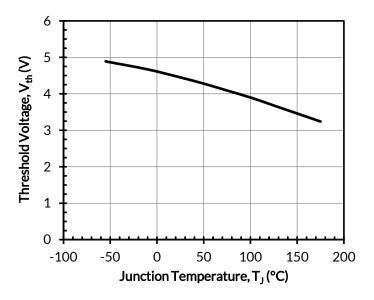


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V



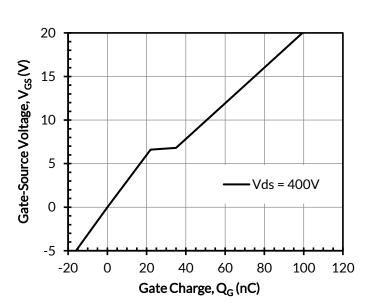


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 10mA

Figure 8. Typical gate charge at $I_D = 60A$





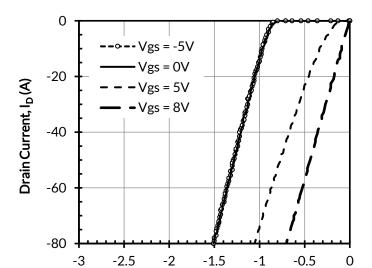
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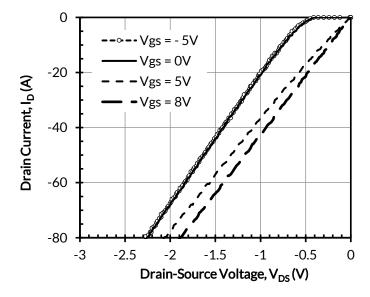


-- Vgs = - 5V Vgs = 0V -20 **-** Vgs = 5V Drain Current, I_D (A) **-** Vgs = 8V -40 -60 -80 -3 -2.5 -2 -1.5 -1 -0.5 0 Drain-Source Voltage, V_{DS} (V)

Figure 9. 3rd quadrant characteristics at $T_J = -55$ °C

Drain-Source Voltage, V_{DS} (V)

Figure 10. 3rd quadrant characteristics at T_J = 25°C



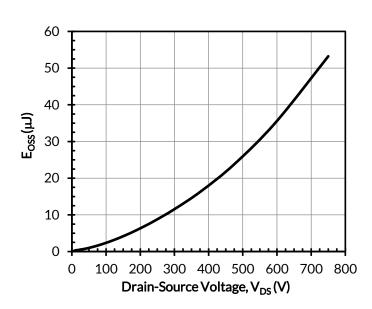


Figure 11. 3rd quadrant characteristics at $T_J = 175$ °C

Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0V$



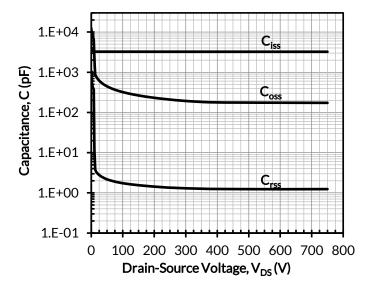








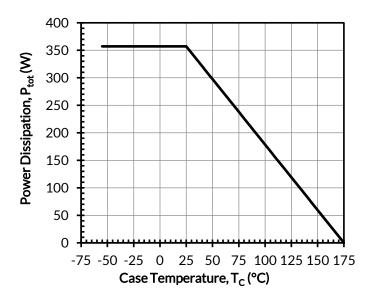




120 100 100 80 40 20 -75 -50 -25 0 25 50 75 100 125 150 175 Case Temperature, T_c (°C)

Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 14. DC drain current derating



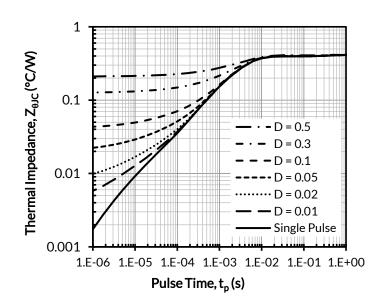


Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance













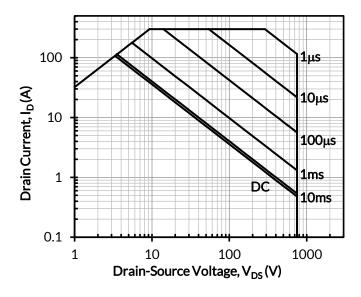


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

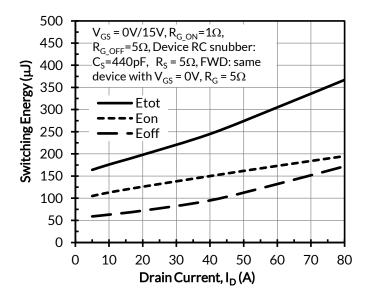


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

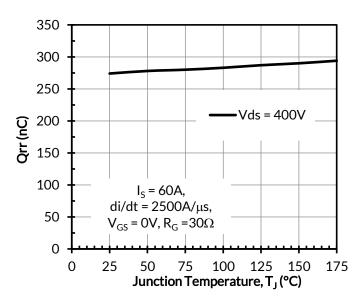


Figure 18. Reverse recovery charge Qrr vs. junction temperature

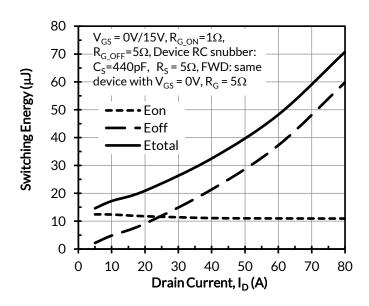


Figure 20. RC snubber energy loss vs. drain current at $V_{DS} = 400V$ and $T_J = 25$ °C



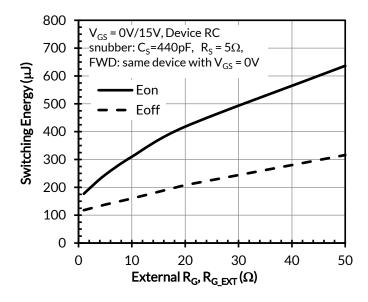








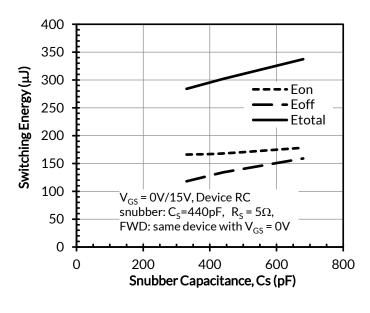




50 V_{GS} = 0V/15V, Device RC snubber: C_S = 440pF, R_S = 5 Ω , 40 FWD: same device with $V_{GS} = 0V$ Snubber R_s Energy (µJ) 30 Rs_Eon Rs_Eoff 20 10 0 10 20 30 40 50 0 External R_G , $R_{G,EXT}(\Omega)$

Figure 21. Clamped inductive switching energy vs. $R_{G,EXT}$ at V_{DS} = 400V, I_D = 60A, and T_J = 25°C

Figure 22. RC snubber energy losses vs. $R_{G,EXT}$ at V_{DS} = 400V, I_D = 60A, and T_J = 25°C



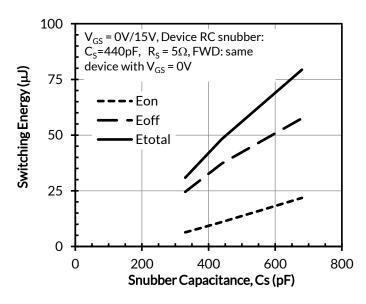


Figure 23. Clamped inductive switching energy vs. Snubber Capacitance Cs at V_{DS} = 400V, I_{D} = 60A, and T_{J} = 25°C

Figure 24. RC snubber energy loss vs. Snubber Capacitance Cs at V_{DS} = 400V, I_D = 60A, and T_J = 25°C





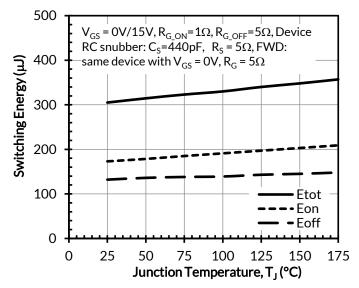












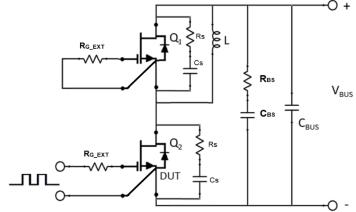


Figure 25. Clamped inductive switching energies vs. junction temperature T_J at V_{DS} = 400V, and I_D = 60A

Figure 26. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ($R_{BS} = 1\Omega$, C_{BS} =100nF) is used to reduce the power loop high frequency oscillations.













Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode. Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

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