

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

## SSM3K44MFV

High Speed Switching Applications

Analog Switch Applications

- AEC-Q101 qualified (Note 1)
- Compact package suitable for high-density mounting
- Low ON-resistance :  $R_{DS(ON)} = 4.0 \Omega$  (max) (@ $V_{GS} = 4 V$ )  
:  $R_{DS(ON)} = 7.0 \Omega$  (max) (@ $V_{GS} = 2.5 V$ )

Note 1: For detail information, please contact to our sales.

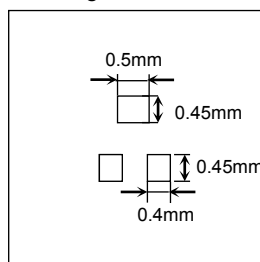
### Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	30	V
Gate-source voltage		$V_{GSS}$	$\pm 20$	V
Drain current	DC	$I_D$	100	mA
	Pulse	$I_{DP}$	200	
Drain power dissipation (Ta = 25°C)		$P_D$ (Note 1)	150	mW
Channel temperature		$T_{ch}$	150	°C
Storage temperature		$T_{stg}$	-55 to 150	°C

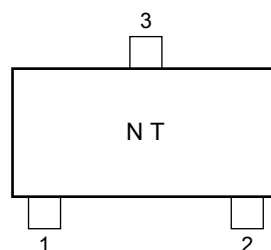
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

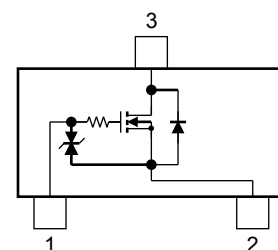
Note 1: Total rating, mounted on FR4 board (25.4 mm × 25.4 mm × 1.6 mm)



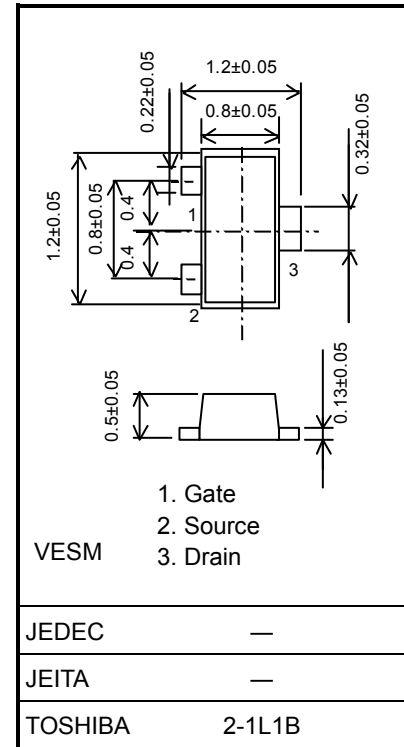
### Marking



### Equivalent Circuit



Unit: mm



Weight: 1.5 mg (typ.)

### Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

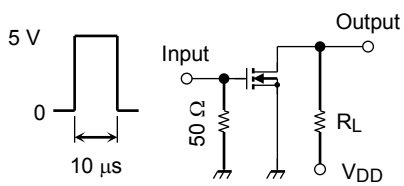
Start of commercial production  
2009-12

## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Gate leakage current	IGSS	VGS = ±14 V, VDS = 0 V	—	—	±1	μA	
Drain-source breakdown voltage	V (BR) DSS	ID = 0.1 mA, VGS = 0 V	30	—	—	V	
Drain cut-off current	IDSS	VDS = 30 V, VGS = 0 V	—	—	1	μA	
Gate threshold voltage	Vth	VDS = 3 V, ID = 0.1 mA	0.8	—	1.5	V	
Forward transfer admittance	Yfs	VDS = 3 V, ID = 10 mA	25	—	—	mS	
Drain-Source on-resistance	RDS (ON)	ID = 10 mA, VGS = 4 V	—	2.2	4.0	Ω	
		ID = 10 mA, VGS = 2.5 V	—	4.0	7.0		
Input capacitance	Ciss	VDS = 3 V, VGS = 0 V, f = 1 MHz	—	8.5	—	pF	
Reverse transfer capacitance	Crss		—	5.3	—		
Output capacitance	Coss		—	9.4	—		
Switching time	Turn-on time	t <sub>on</sub>	VDD = 5 V, ID = 10 mA, VGS = 0 to 5 V	—	50	—	ns
	Turn-off time	t <sub>off</sub>		—	200	—	

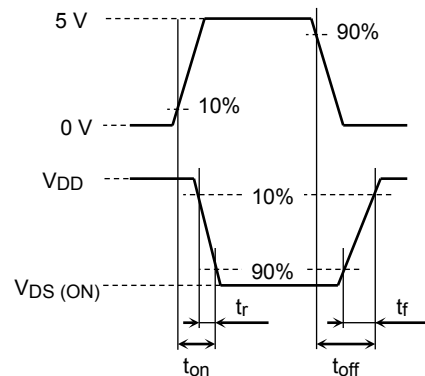
## Switching Time Test Circuit

### (a) Test circuit



V<sub>DD</sub> = 5 V  
 Duty ≤ 1%  
 Input: t<sub>r</sub>, t<sub>f</sub> < 5 ns  
 (Z<sub>out</sub> = 50 Ω)  
 Common Source  
 Ta = 25°C

### (b) VIN



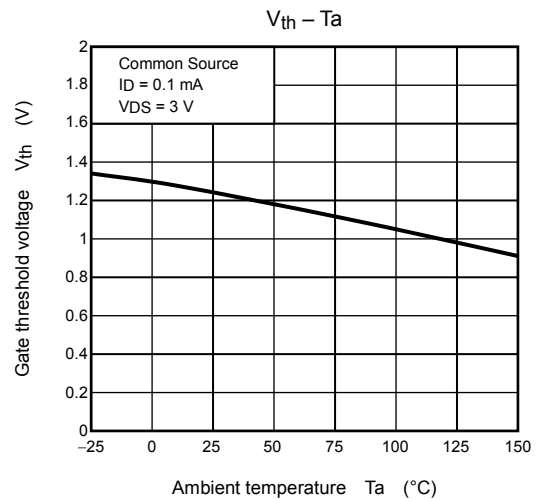
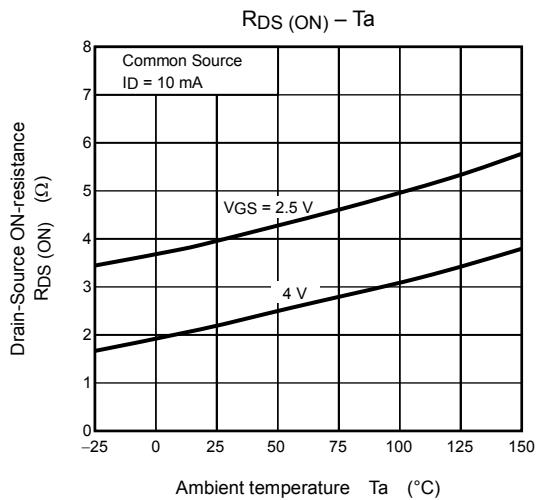
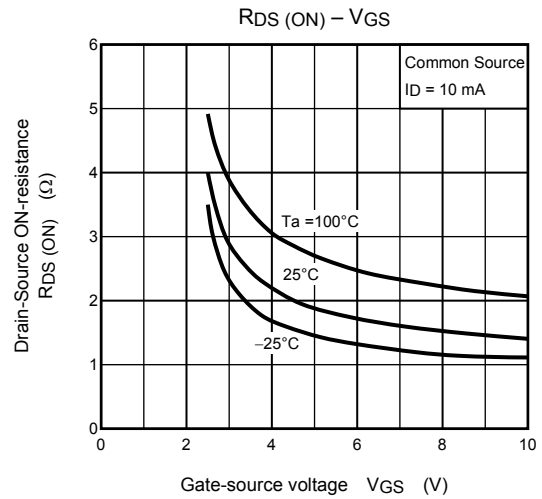
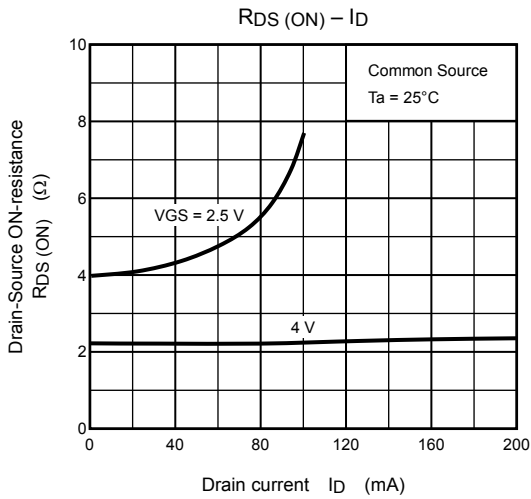
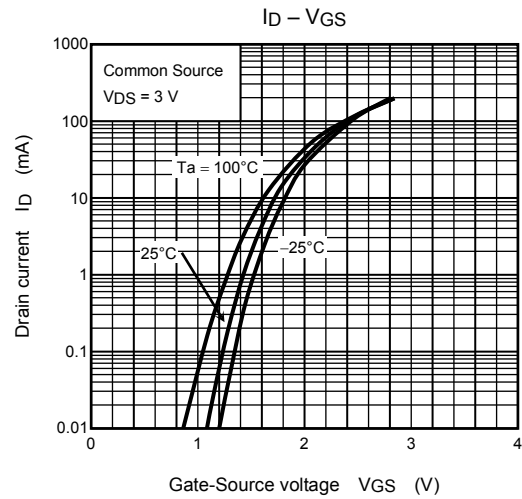
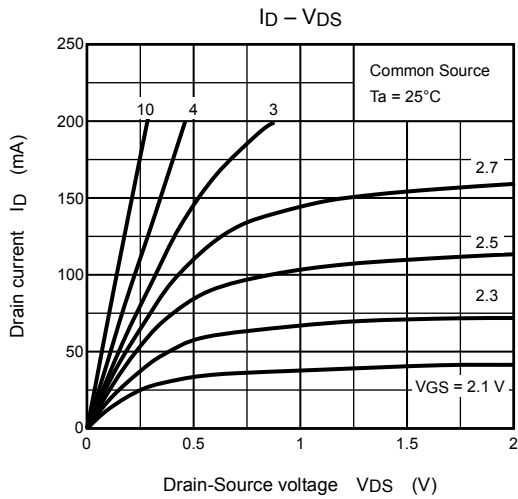
### (c) VOUT

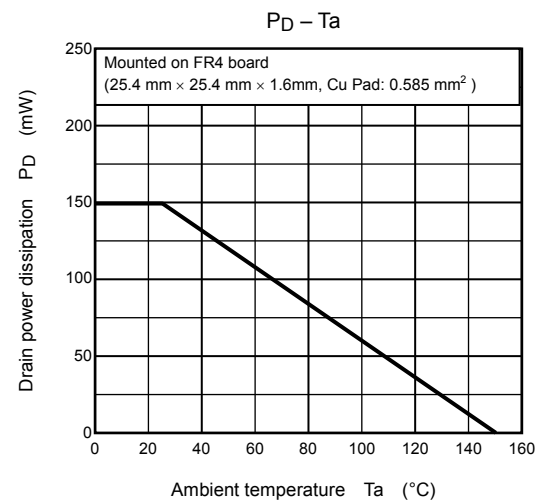
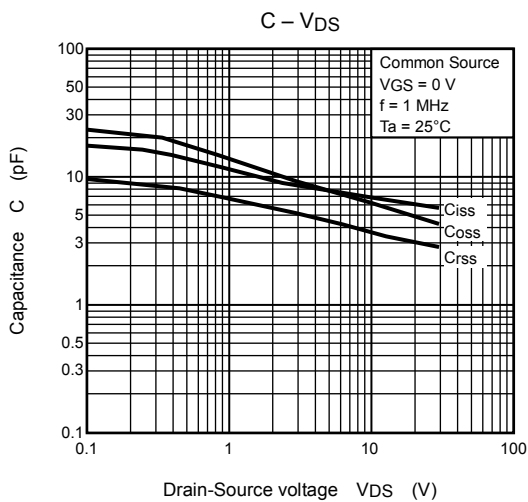
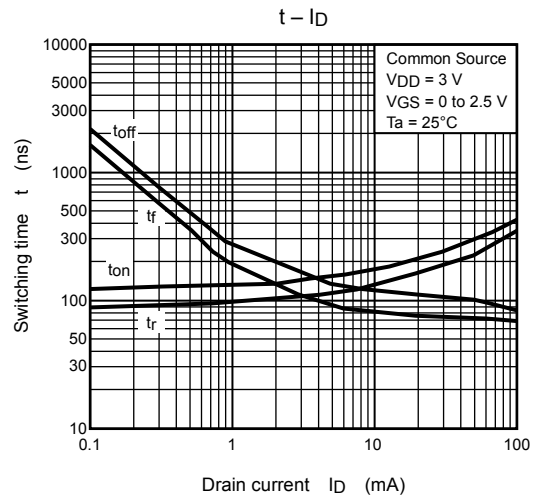
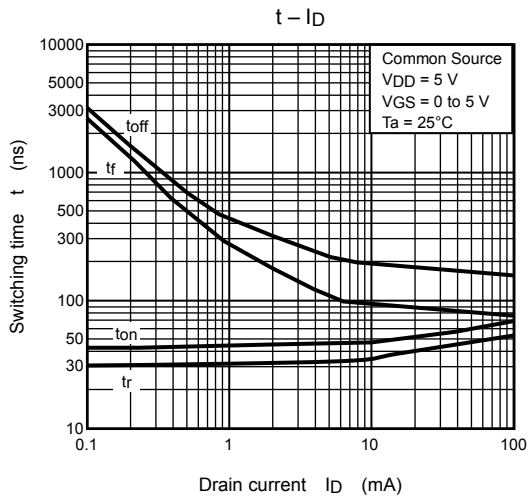
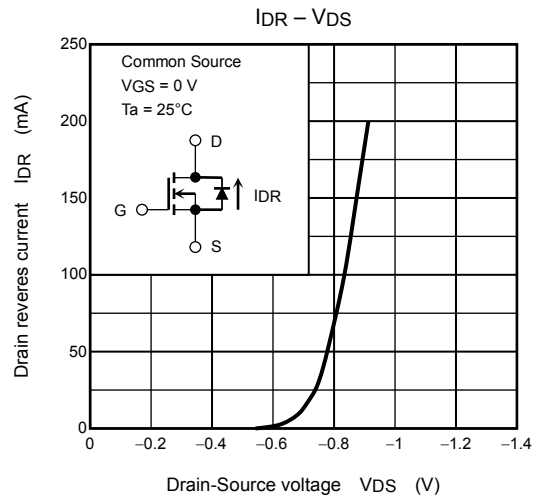
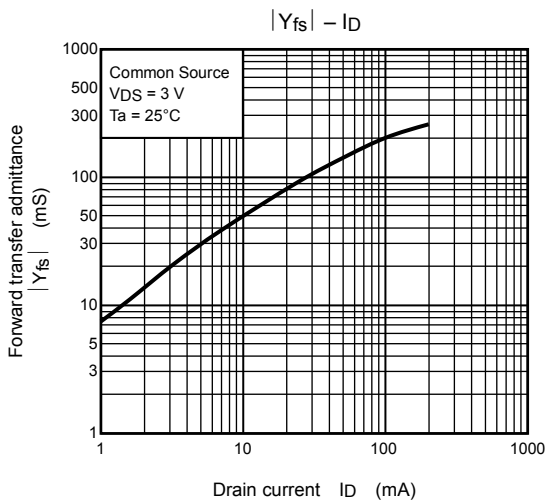
## Precaution

V<sub>th</sub> can be expressed as the voltage between gate and source when the low operating current value is ID = 100 μA for this product. For normal switching operation, VGS (on) requires a higher voltage than V<sub>th</sub> and VGS (off) requires a lower voltage than V<sub>th</sub>.

(The relationship can be established as follows: VGS (off) < V<sub>th</sub> < VGS (on) )

Please take this into consideration when using the device.





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