Digital Attenuator, 5-Bit, Serial / Parallel Control
0.1 - 30 GHz, 31 Attenuation Range

MAAD-011035
Rev. V2

Features

- 5-Bit, 1 dB LSB, 31 dB Range
- Integrated CMOS Driver
- Parallel or Serial (P/S) Control
- Low DC Power Consumption
- Attenuation Accuracy:
  +/-(0.4 + 7% of attenuation setting) dB
- Lead-Free 4 mm 24-Lead PQFN Package
- RoHS* Compliant

Applications

- Test Equipment (instrumentation)
- Communications (commercial and military) :
  Cellular Infrastructure
  Radars
  Radios (MMW)
- General Purpose

Description

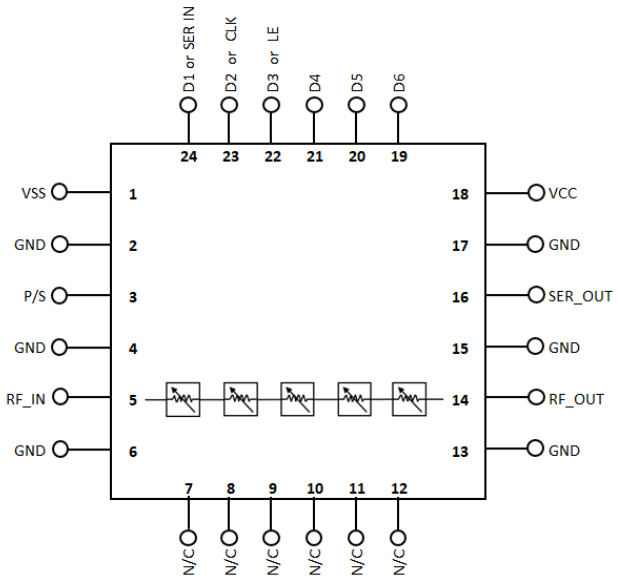
The MAAD-011035 is a wide band 5-bit, 1 dB step GaAs pHEMT MMIC digital attenuator in a lead-free 4 mm 24 lead PQFN surface mount plastic package. This device is ideally suited for use where high accuracy, very low power consumption, and low intermodulation products are required.

This attenuator is controlled with either a SPI compatible serial interface or a 5 bit parallel word.

Ordering Information

Part Number	Package
MAAD-011035-TR0500	500 piece reel
MAAD-011035-001SMB	Sample Board

Functional Schematic



Pin Configuration[1,2]

Pin #	Function
1	VSS
2, 4, 6, 13, 15, 17	GND
3	P/S
7 - 12	N/C
5	RF IN
14	RF OUT
16	SER OUT
18	VCC
19	D6
20	D5
21	D4
22	D3 or LE
23	D2 or CLK
24	D1 or SER IN

1. MACOM recommends grounding all N/C (no connection) pins
2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications:

Freq. = 0.1 - 30 GHz, T_A = 25°C, Z_0 = 50 Ω, V_{CC} = +5 V, V_{SS} = -5 V, P_{IN} = 0 dBm

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Reference Insertion Loss[3]	0.1 - 18.0 GHz 18.0 - 26.5 GHz 26.5 - 30.0 GHz	dB	—	3.4 4.8 5.2	4.4 — 6.2
RMS Attenuation Error[4]	0.1 - 30.0 GHz (RMS, mean)	dB	—	0.4	—
Attenuation Accuracy	Relative to Insertion Loss (0.1 - 30 GHz)	± (0.4 + 7% of attenuation setting) typ.			
Return Loss (IN & OUT)[3]	All states	dB	—	-12	—
Input P0.1dB	Reference State (beyond 1 GHz)	dBm	—	21	—
IIP_3	2-Tone, 10 dBm/tone, 1 MHz Spacing Reference State (beyond 1 GHz)	dBm	—	42	—
T_{RISE}, T_{FALL}	10% to 90% RF, 90% to 10% RF	ns	—	15	—
V_{CC}	—	V	+3.0	—	+5.5
I_{CC}	—	µA	—	5	—
V_{SS}	—	V	-5.5	-5.0	-3.0
I_{SS}	—	mA	—	-0.1	—
V_H V_L	HIGH level control voltage LOW level control voltage	V	0.7 X V_{CC} 0.0	—	V_{CC} 0.3 X V_{CC}
ESD	HBM	V	—	Class1A	—

3. Test frequencies = 1 GHz, 18 GHz, and 30 GHz.
4. RMS calculation, mean:

$$\textit{RMS ERROR, mean} = \sqrt{\frac{1}{n}\sum (Er_i - Er_{Ave})^2}$$

Truth Table[5]

D6	D5	D4	D3	D2	D1	Attenuation (dB)
0	0	0	0	0	0	Reference IL
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	1	0	0	4
0	0	1	0	0	0	8
0	1	0	0	0	0	16
0	1	1	1	1	1	31

5. "0" = CMOS Low "1" = COMS High (see specifications table)

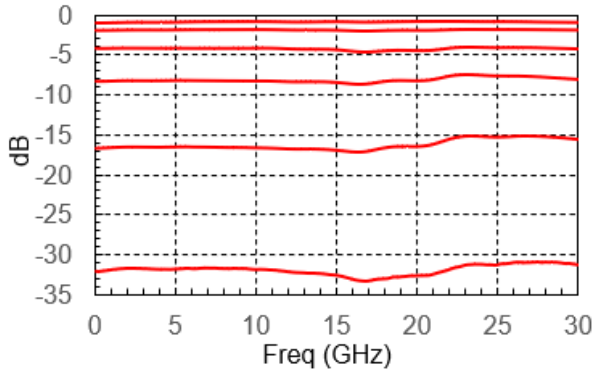
Absolute Maximum Ratings[6,7]

Parameter	Absolute Maximum
Input Power	31 dBm
V_{CC} Voltage	6 V
Control Voltage	-0.5 V ≤ V_C ≤ 5.5 V
Junction Temperature	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

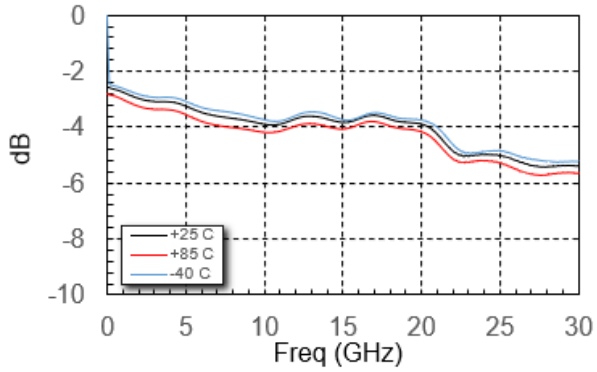
6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.

Typical RF Performance Plots, @ +25°C

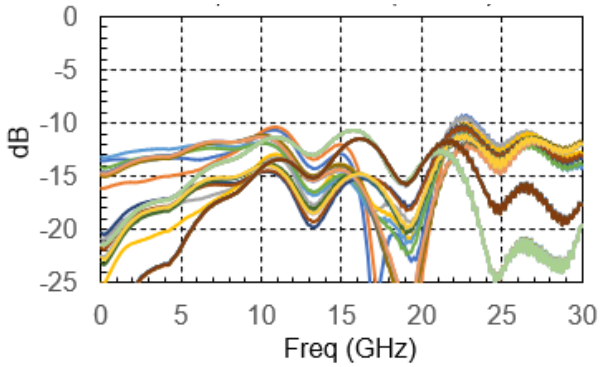
Relative Attenuation



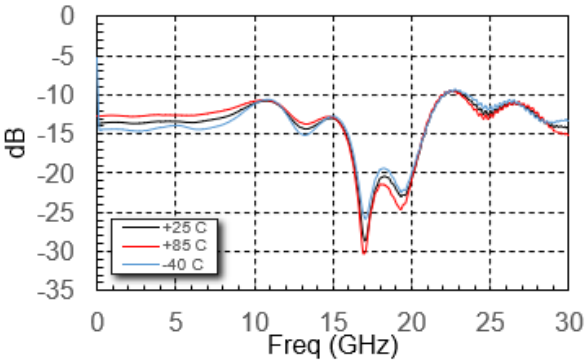
Insertion Loss vs. Temperature



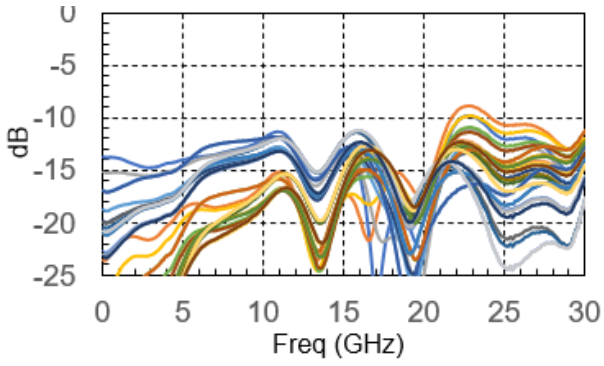
Input Return Loss (all states)



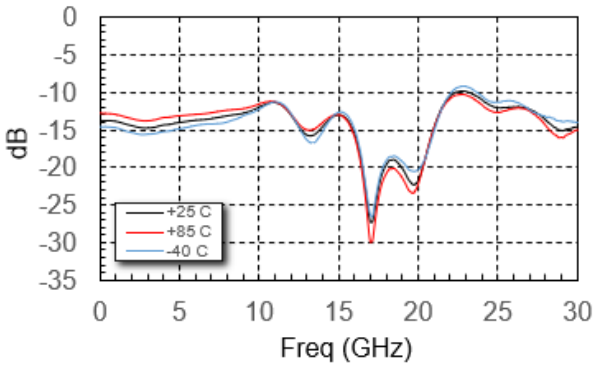
Input Return Loss vs. Temperature



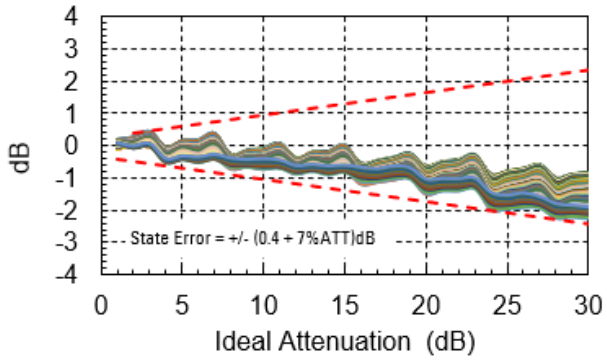
Output Return Loss (all states)



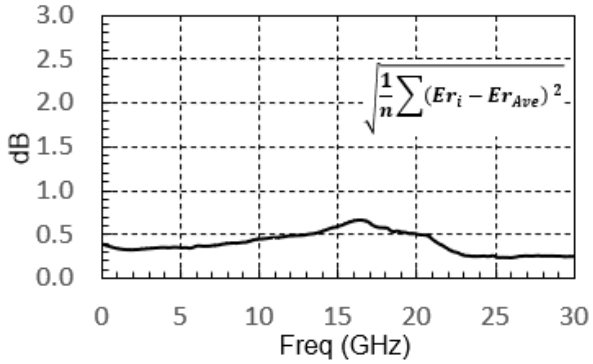
Output Return Loss vs. Temperature



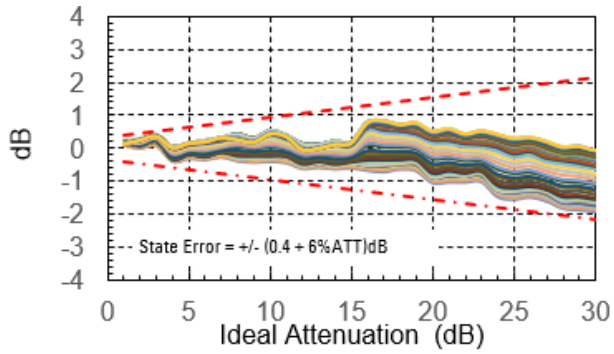
BIT Error vs. Attenuation State
0.1 - 18 GHz, @ +25°C



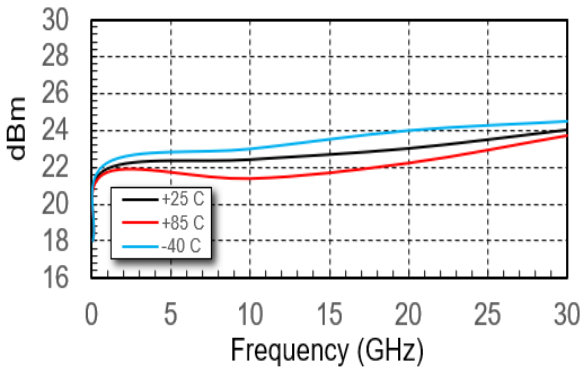
RMS Error vs. Frequency (mean)



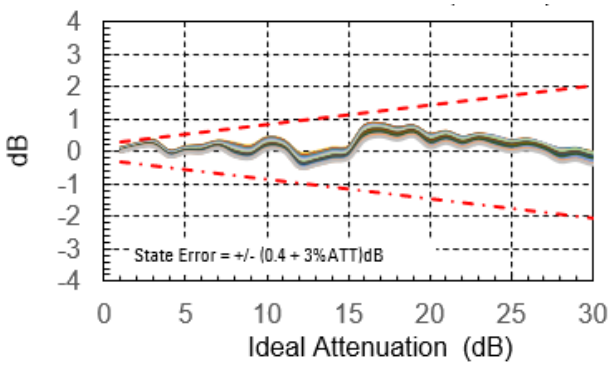
BIT Error vs. Attenuation State
18 - 26.5 GHz, @ +25°C



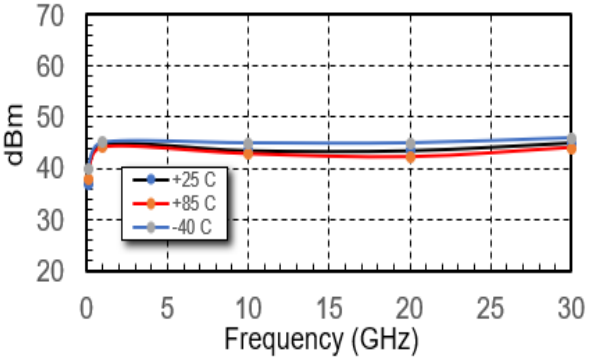
Input 0.1dB Compression over Temp



BIT Error vs. Attenuation State
26.5 - 30GHz, @ +25°C



Input IP3 over Temperature



Modes of Operation
Serial and Direct Parallel

Mode Truth Table[8,9,10]

P/S	LE	Mode
1	X	Serial
0	N/A	Direct Parallel

8. There is a dummy bit (D6), that must be sent in the serial mode. This is because this 5 bit digital attenuator uses the same driver as the 6 bit digital attenuator
9. In the parallel mode: D6 should be tied to ground or to V_{CC}.
10. In the serial mode: D4, D5, and D6 should be tied to ground or to V_{CC}.

Direct Parallel Mode

The parallel mode is enabled when P/S is set low. In the direct parallel mode, the digital attenuator is controlled by the parallel control inputs directly. When P/S is set low, pins 22, 23,and 24 have the D3, D2, and D1 function.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

Serial Mode

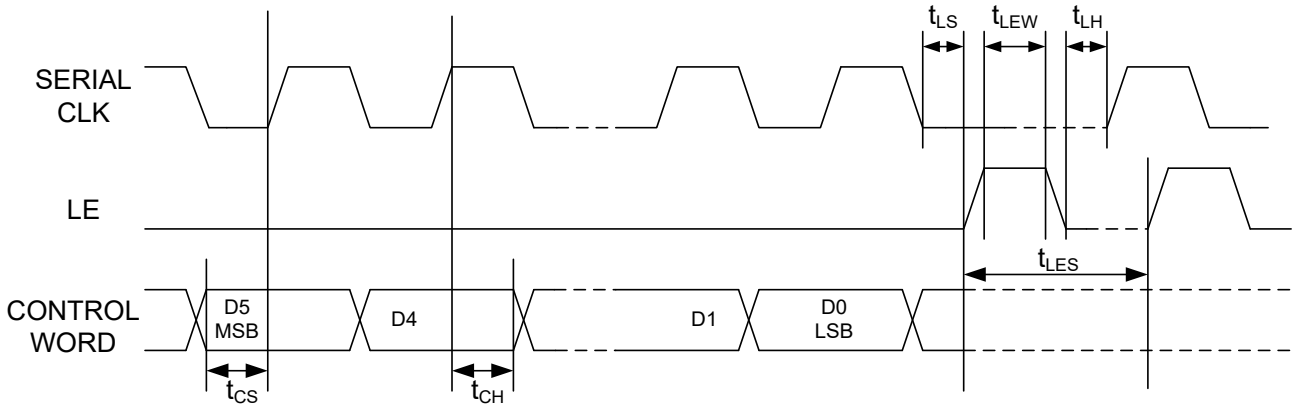
The serial control interface (SER IN, CLK, LE, SER OUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with the MSB first. After shifting in the 6 bit word, a rising edge on LE will set the digital attenuator to the desired state. While LE is high the CLK is masked to protect the data while implementing the change. SEROUT is SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled. When P/S is set high, pins 22, 23, and 24 have the LE, CLK, and SER IN function.

In serial mode operation, the outputs will stay constant while LE is kept low.

Functionality
Modes of Operation: Serial and Direct Parallel

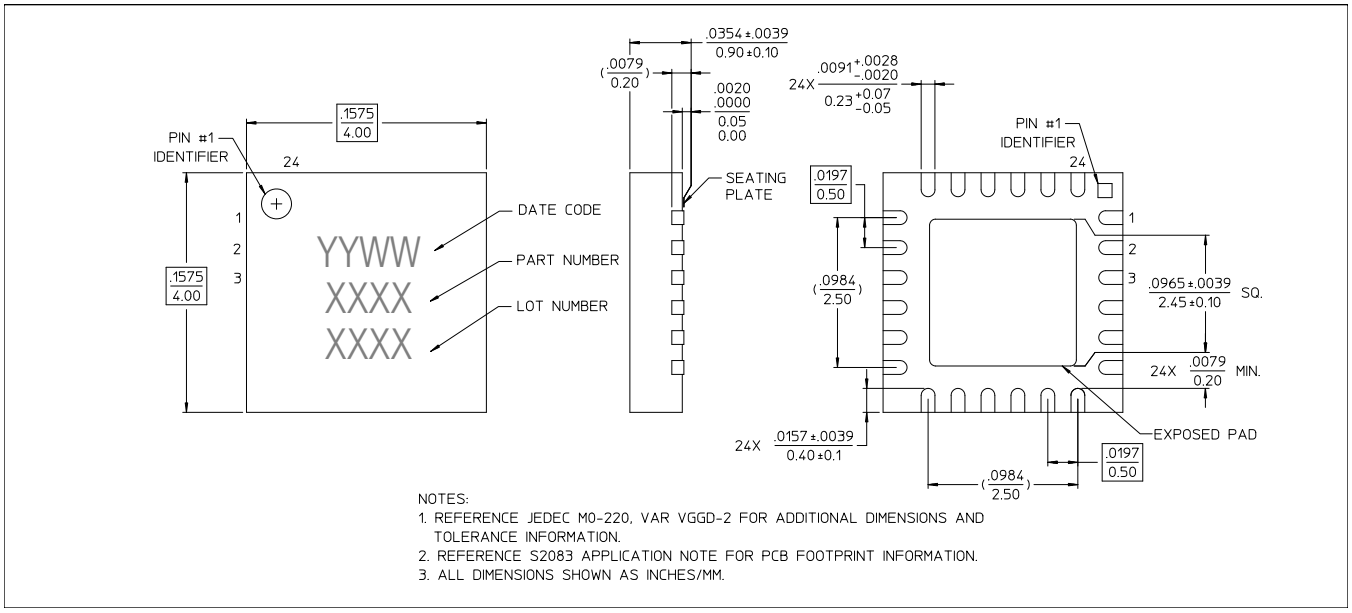
Serial Input Interface Timing Diagram



Serial Interface Timing Characteristics

Symbol	Parameter	Units
t_{SCK}	Min. Serial Clock Period	ns
t_{CS}	Min. Control Set-up Time	ns
t_{CH}	Min. Control Hold Time	ns
t_{LS}	Min. LE Set-up Time	ns
t_{LEW}	Min. LE Pulse Width	ns
t_{LH}	Min. Serial Clock Hold Time from LE	ns
t_{LES}	Min. LE Pulse Spacing	ns

Lead Free 4 mm 24-Lead PQFN †



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.