



PJL9403

30V P-Channel Enhancement Mode MOSFET

Voltage

-30 V

Current

-3.6A

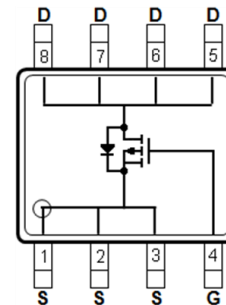
Features

- $R_{DS(ON)}$, $V_{GS}@-10V$, $I_D@-3.6A < 72m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-2.4A < 96m\Omega$
- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: SOP-8 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams

SOP-8



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	V_{DS}	-30	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	-3.6	A
		$T_A=70^\circ\text{C}$	-2.4	
Pulsed Drain Current ^(Note 1)	I_{DM}	-14.4		
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2.1	W
		$T_A=70^\circ\text{C}$	1.3	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$	
Typical Thermal Resistance	$R_{\theta JA}$	59.5	$^\circ\text{C/W}$	
- Junction to Ambient ^(Note 5)				



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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.37	-2.1	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-3.6A$	-	59	72	m Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-2.4A$	-	76	96	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-3.6A,$ $V_{GS}=-10V$ (Note 1,2)	-	10	-	nC
Gate-Source Charge	Q_{gs}		-	1.1	-	
Gate-Drain Charge	Q_{gd}		-	1.7	-	
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	417	-	pF
Output Capacitance	C_{oss}		-	50	-	
Reverse Transfer Capacitance	C_{rss}		-	36	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-3.6A,$ $V_{GS}=-10V,$ $R_G=6\Omega$ (Note 1,2)	-	3.2	-	ns
Turn-On Rise Time	t_r		-	33	-	
Turn-Off Delay Time	$t_{d(off)}$		-	119	-	
Turn-Off Fall Time	t_f		-	68	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-3.6	A
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$	-	-0.77	-1.2	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

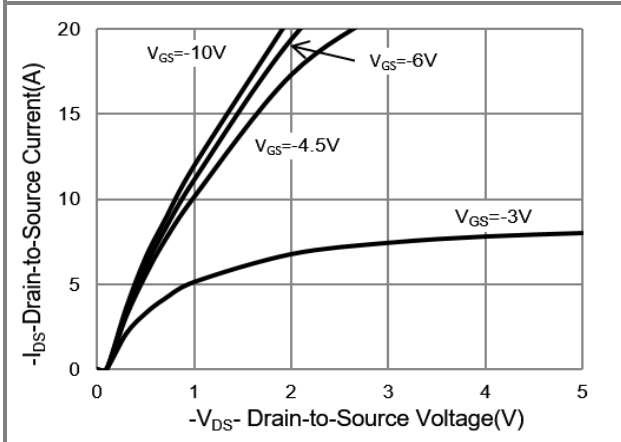


Fig.1 On-Region Characteristics

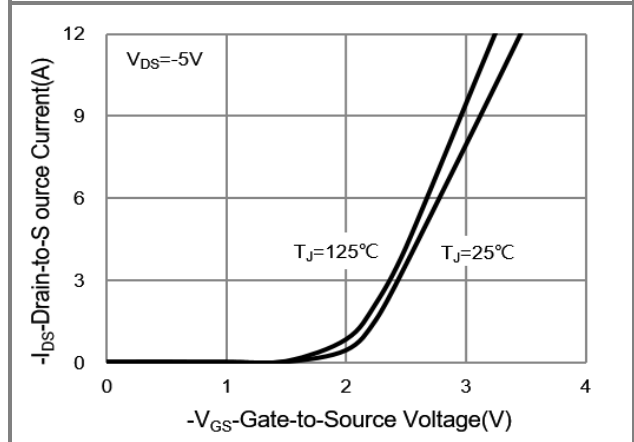


Fig.2 Transfer Characteristics

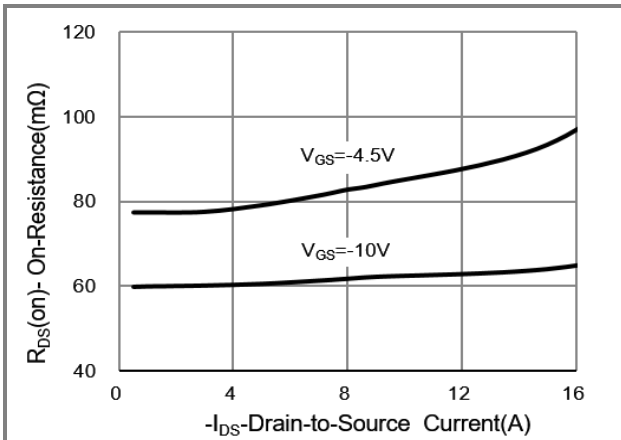


Fig.3 On-Resistance vs. Drain Current

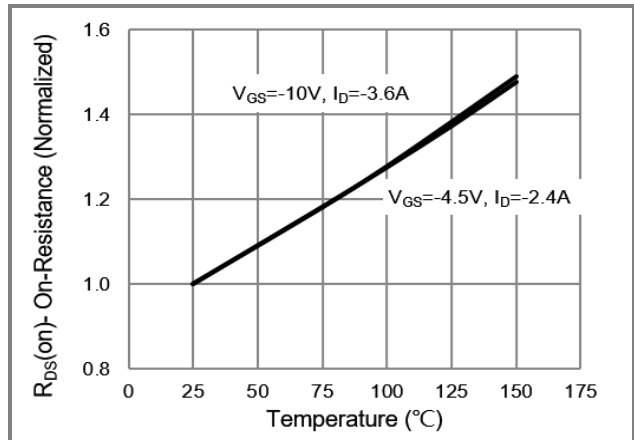


Fig.4 On-Resistance vs. Junction temperature

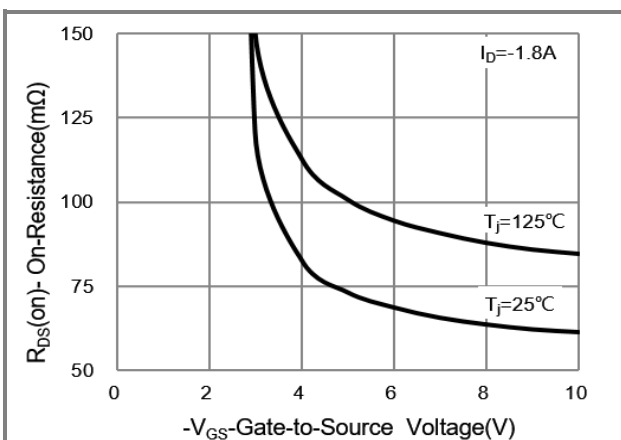


Fig.5 On-Resistance Variation with V_{GS}

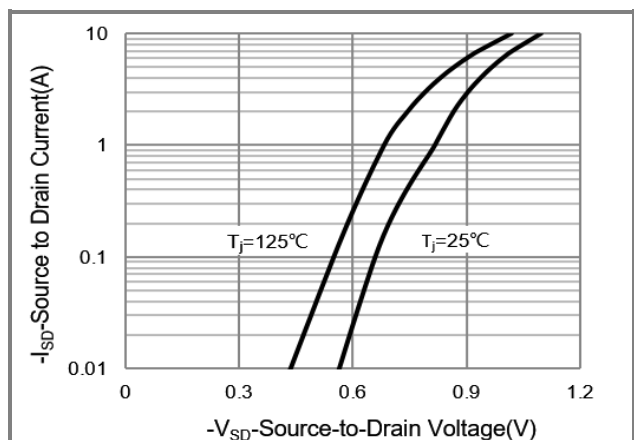


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

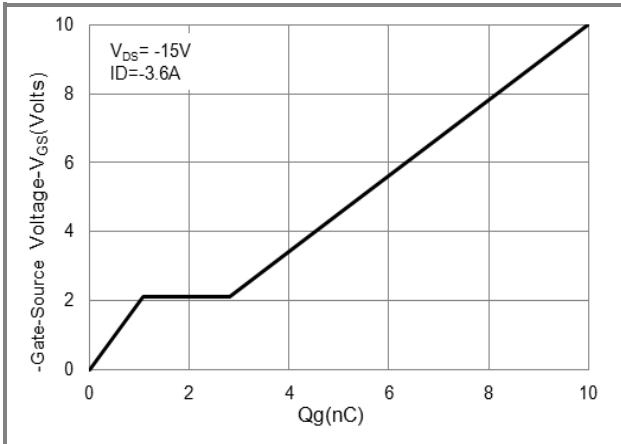


Fig.7 Gate-Charge Characteristics

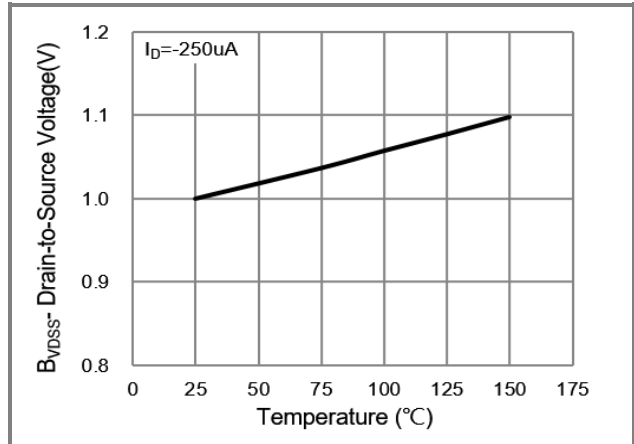


Fig.8 Breakdown Voltage Variation vs. Temperature

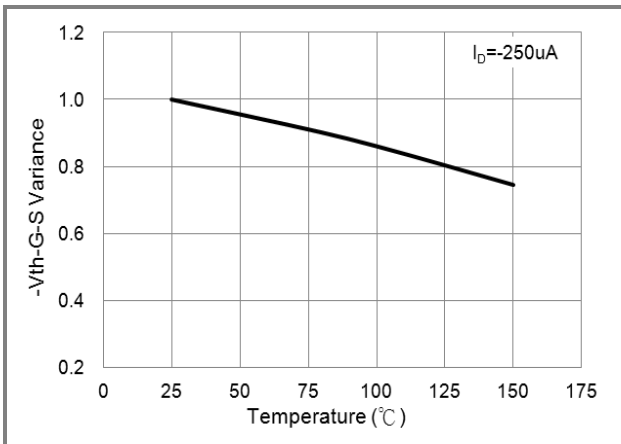


Fig.9 Threshold Voltage Variation with Temperature

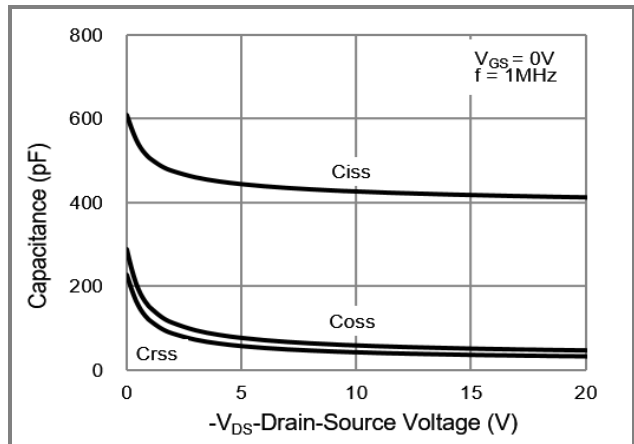


Fig.10 Capacitance vs. Drain-Source Voltage

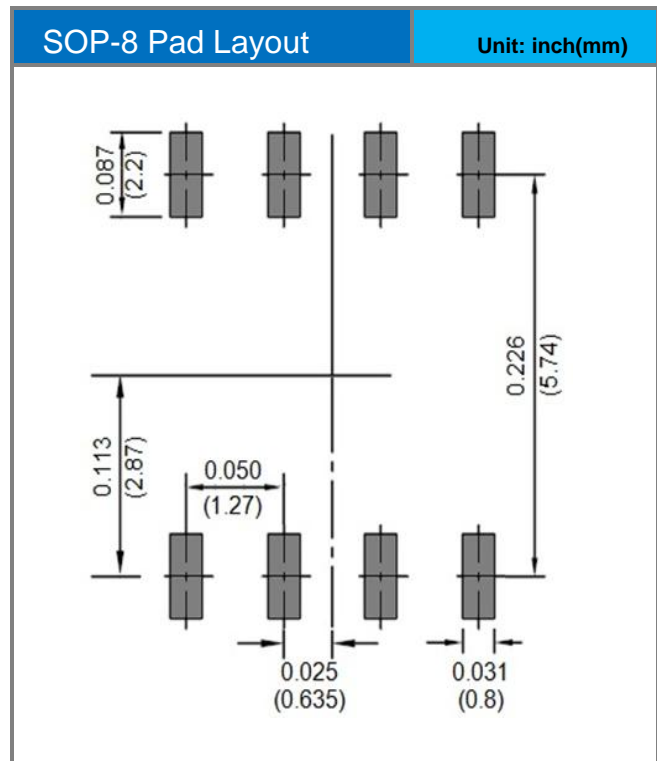
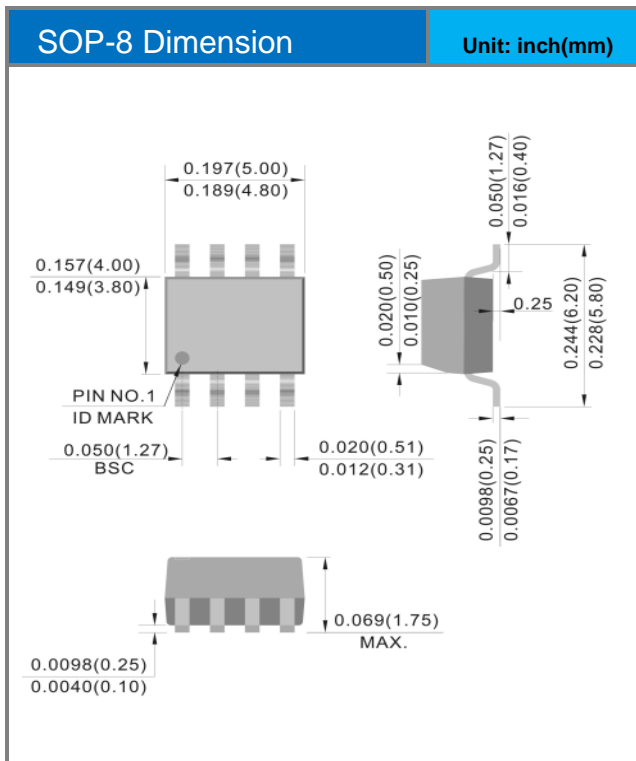


PJL9403

Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJL9403_R2_00001	SOP-8	2.5K pcs / 13" reel	L9403	Halogen free

Packaging Information & Mounting Pad Layout





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