

1T 8051
8-bit Microcontroller

NuMicro[®] Family
ML51/ML54/ML56 Series
Product Brief

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TABLE OF CONTENTS

1 GENERAL DESCRIPTION 6

2 FEATURES 7

3 PART INFORMATION 12

 3.1 ML51/ML54/ML56 Series Package Type..... 12

 3.2 ML51/ML54/ML56 Series Selection Guide..... 13

 3.2.1 ML51 Series13

 3.2.2 ML54 Series16

 3.2.3 ML56 Series17

4 PIN CONFIGURATION 18

 4.1 Pin Configuration..... 18

 4.1.1 ML51/ML54/ML56 Series Pin Diagram18

 4.1.2 ML51/ML54/ML56 Series Multi Function Pin Diagram26

 4.2 Pin Description..... 66

 4.2.1 ML51/ML54/ML56 Series Pin Mapping66

 4.2.2 ML51/ML54/ML56 Series Pin Function Description68

5 BLOCK DIAGRAM..... 73

 5.1 ML51 Series Full Function Block 73

6 UTILITIES 74

 6.1 Programmer and Debugger 74

 6.2 Development Environment..... 74

 6.3 Development Board 74

7 PACKAGE DIMENSIONS 75

 7.1 LQFP 64L (7x7x1.4 mm Footprint 2.0 mm)..... 75

 7.2 LQFP 48-pin (7x7x1.4 mm Footprint 2.0mm) 76

 7.3 LQFP 44-pin (10x10x1.4mm)..... 77

 7.4 QFN 32-pin (4.0 x 4.0 x 0.8 mm) 78

 7.5 LQFP 32-pin (7.0 x 7.0 x 1.4 mm)..... 79

 7.6 TSSOP 28-pin (4.4 x 9.7 x 1.0 mm) 80

 7.7 SOP 28-pin (300mil)..... 81

 7.8 TSSOP 20-pin (4.4 x 6.5 x 0.9 mm) 82

 7.9 SOP 20-pin (300 mil) 83

 7.10 QFN 20-pin (3.0 x 3.0 x 0.8 mm) 84

 7.11 TSSOP 14-pin (4.4 x 5.0 x 0.9 mm)..... 85

 7.12 MSOP 10-pin (3.0 x 3.0 x 0.85 mm)..... 86

8 REVISION HISTORY87

LIST OF FIGURES

Figure 4.1-1 ML51SD1AE Pin Assignment..... 18

Figure 4.1-2 ML54SD1AE / ML56SD1AE Pin Assignment..... 19

Figure 4.1-3 ML51LD1AE Pin Assignment 20

Figure 4.1-4 ML54LD1AE / ML56LD1AE Pin Assignment..... 20

Figure 4.1-5 ML54MD1AE / ML56MD1AE Pin Assignment..... 21

Figure 4.1-6 ML51TD1AE / ML51TC0AE / ML51TB9AE Pin Assignment..... 21

Figure 4.1-7 ML51PC0AE / ML51PB9AE Pin Assignment 22

Figure 4.1-8 ML51EC0AE / ML51EB9AE Pin Assignment 22

Figure 4.1-9 ML51UC0AE / ML51UB9AE Pin Assignment..... 23

Figure 4.1-10 ML51FB9AE Pin Assignment 23

Figure 4.1-11 ML51OB9AE Pin Assignment..... 24

Figure 4.1-12 ML51XB9AE Pin Assignment..... 24

Figure 4.1-13 ML51DB9AE Pin Assignment..... 25

Figure 4.1-14 ML51BB9AE Pin Assignment 25

Figure 4.1-15 ML51SD1AE Multi-Function Pin assignment 26

Figure 4.1-16 ML54SD1AE Multi-Function Pin assignment 29

Figure 4.1-17 ML56SD1AE Multi-Function Pin assignment 32

Figure 4.1-18 ML51LD1AE Multi-Function Pin assignment..... 35

Figure 4.1-19 ML54LD1AE Multi-Function Pin assignment..... 38

Figure 4.1-20 ML56LD1AE Multi-Function Pin assignment..... 41

Figure 4.1-21 ML54MD1AE Multi-Function Pin assignment..... 44

Figure 4.1-22 ML56MD1AE Multi-Function Pin assignment..... 47

Figure 4.1-23 ML51TD1AE Multi-Function Pin assignment..... 50

Figure 4.1-24 ML51TC0AE / ML51TB9AE Multi-Function Pin Assignment..... 52

Figure 4.1-25 ML51PC0AE / ML51PB9AE Multi-Function Pin Assignment 54

Figure 4.1-26 ML51EC0AE / ML51EB9AE Multi-Function Pin Assignment 56

Figure 4.1-27 ML51UC0AE / ML51UB9AE Multi Function Pin Assignment 58

Figure 4.1-28 ML51FB9AE Multi Function Pin Assignment..... 60

Figure 4.1-29 ML51OB9AE Multi Function Pin Assignment 61

Figure 4.1-30 ML51XB9AE Multi Function Pin Assignment 62

Figure 4.1-31 ML51DB9AE Multi Function Pin Assignment 64

Figure 4.1-32 ML51BB9AE Pin Assignment 65

Figure 5.1-1 Functional Block Diagram..... 73

Figure 7.1-1 LQFP 64L Package Dimension 75

Figure 7.2-1 LQFP48 Package Dimension 76

Figure 7.3-1 LFP44 Package Dimension 77

Figure 7.4-1 QFN-32 Package Dimension 78

Figure 7.5-1 LQFP-32 Package Dimension 79

Figure 7.6-1 TSSOP-28 Package Dimension 80

Figure 7.7-1 SOP-28 Package Dimension 81

Figure 7.8-1 TSSOP-20 Package Dimension 82

Figure 7.9-1 SOP-20 Package Dimension 83

Figure 7.10-1 QFN-20 Package Dimension 84

Figure 7.11-1 TSSOP-14 Package Dimension 85

Figure 7.12 -1 MSOP-10 Package Dimension 86

1 GENERAL DESCRIPTION

The NuMicro®ML51/ML54/ML56 series is a Flash embedded 1T 8051-based microcontroller. The instruction set of the ML51 series is fully compatible with the standard 80C51 with enhanced performance; This series is a three-to-one single microcontrollers, intergrated with up to 14 channels of capacitive touch and LCD driver.

The ML51/ML54/ML56 series is 1T 8051 core based low-power microcontrollers running at less 80µA/MHz in normal run mode, and power down current is below 1µA. It Provides operating frequency up to 24 MHz. 16KB and 32KB Flash of ML51 series voltage range supports 1.8V to 5.5V, and 64KB Flash of ML51 series supports 1.8 to 3.6V voltage range.

The ML51/ML54/ML56 series microcontroller provides 3 power modes to reduce power consumption –Low power run mode, Low power Idle mode, and Power-down mode. In Low power run mode, the power consumption can be down to 15 uA at 38.4 kHz LIRC. In Low power idle mode, CPU processing is suspended by holding the Program Counter. No program code is fetched and run in low power idle mode if the power consumption does not exceed 13 uA. Power-down mode stops the whole system clock for minimum power consumption with the leakage current less than 1 uA. The system clock of the ML51 series can also be slowed down by software clock divider, which allows for flexibility between execution performance and power consumption.

The ML51/ML54/ML56 series provides rich peripherals including 256 bytes of SRAM, 4 Kbytes of auxiliary RAM (XRAM), up to 56 general purpose I/O, two 16-bit Timers/Counters 0/1, one 16-bit Timer2 with three-channel input capture module, one Watchdog Timer (WDT), one Self Wake-up Timer (WKT), one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, two ISO7816 Smartcard interface, two SPI, two I2C, six enhanced PWM output channels with dead zone control, six PWM output channels with three individual configurable period, two analog comparators, eight-channel shared pin interrupt for all I/O ports, and one 12-bit ADC at 500 ksp/s.

All series contains up to 64 Kbytes Flash, called APROM designed for programming. Flash supports In-Application-Programming (IAP) function, which supports on-chip firmware upgrade. Partial flash can be configured as Data Flash programmed by IAP and read by IAP or MOVC instruction. The ML51/ML54/ML56 series includes an additional configurable up to 4/3/2/1 Kbytes Flash area called LDROM, in which the Boot Code normally resides for carrying out the In-System-Programming (ISP). To facilitate mass production programming and verification, the Flash is allowed to be programmed and read electronically by parallel Writer/Programmer or In-Circuit-Programming (ICP) with Nu-Link. Once programmed and verified, the programmed code can be protected by the Flash lock mechanism from being read out by external programming tool.

Through the high performance and low power features of ML51/ML54/ML56 series, this series benefits for low-power, battery powered devices, general purpose, home appliances, and motor control system.

Series	V _{DD} Voltage	LCD Driver	Touch Key
ML51 32/16KB Flash Series	1.8 ~ 5.5 V	-	-
ML51 64KB Flash Series	1.8 ~3.6 V	-	-
ML54 Series	1.8 ~3.6 V	✓	-
ML56 Series	1.8 ~3.6 V	✓	✓

2 FEATURES

Core and System

- | | |
|-------------|---|
| 8051 | <ul style="list-style-type: none"> Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller. Instruction set fully compatible with MCS-51. 4-priority-level interrupts capability. Dual Data Pointers (DPTRs). |
|-------------|---|

- | | |
|-----------------------------|--|
| Power on Reset (POR) | <ul style="list-style-type: none"> POR with 1.55V threshold voltage level |
|-----------------------------|--|

- | | |
|---------------------------------|--|
| Brown-out Detector (BOD) | <ul style="list-style-type: none"> 7-level selection, with brown-out interrupt and reset option. (4.4V / 3.7V / 3.0V / 2.7V / 2.4V / 2.0V / 1.8V) |
|---------------------------------|--|

- | | |
|--------------------------------|--|
| Low Voltage Reset (LVR) | <ul style="list-style-type: none"> LVR with 1.63V threshold voltage level |
|--------------------------------|--|

- | | |
|-----------------|---|
| Security | <ul style="list-style-type: none"> 96-bit Unique ID (UID) 128-bit Unique Customer ID (UCID) 128-bytes security protection memory SPROM |
|-----------------|---|

Memories

- | | |
|--------------|--|
| Flash | <ul style="list-style-type: none"> Up to 64 KBytes of APROM for User Code. 4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP) Flash Memory accumulated with pages of 128 Bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be use as Data Flash An additional 128 bytes security protection memory SPROM Code lock for security by CONFIG |
|--------------|--|

- | | |
|-------------|--|
| SRAM | <ul style="list-style-type: none"> 256 Bytes on-chip RAM. Additional 4 KBytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction. |
|-------------|--|

- | | |
|--------------|--|
| PDMA: | <ul style="list-style-type: none"> Three modes: peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer. Source address and destination address must be word alignment in all modes. Memory-to-memory mode: transfer length must be word alignment. |
|--------------|--|

Clocks

- | | |
|------------------------------|--|
| External Clock Source | <ul style="list-style-type: none"> 4~24 MHz High-speed external crystal oscillator (HXT) for precise timing operation |
|------------------------------|--|

	<ul style="list-style-type: none"> 32.768 kHz High-speed external crystal oscillator (LXT) for RTC operation
Internal Clock Source	<ul style="list-style-type: none"> Default 24 MHz high-speed internal oscillator (HIRC) trimmed to $\pm 1\%$ (accuracy at 25 °C, 3.3 V), $\pm 2\%$ in -20~105°C. 38.4 kHz low-speed internal oscillator (LIRC) calibrating to $\pm 2\%$ by software from high-speed internal oscillator
Timers	
16-bit Timer	<ul style="list-style-type: none"> Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051. One 16-bit Timer 2 with three-channel input capture module and 9 input pin can be selected. One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs.
Watchdog	<ul style="list-style-type: none"> 6-bit free running up counter for WDT time-out interval. Selectable time-out interval is 1.66 ms ~ 3413.12 ms since WDT_CLK = 38.4 kHz (LIRC). Able to wake up from Power-down or Idle mode Interrupt or reset selectable on watchdog time-out
Wake-up Timer	<ul style="list-style-type: none"> 16-bit free running up counter for time-out interval. Clock sources from LIRC Able self Wake-up wake up from Power-down or Idle mode, and auto reload count value. Supports Interrupt
PWM	<ul style="list-style-type: none"> Up To 12 output pins can be selected Supports maximum clock source frequency up to 24 MHz Supports up to Three PWM modules, each module provides 6 output channels. Supports independent mode for PWM output Supports complementary mode for 3 complementary paired PWM output channels Dead-time insertion with 8-bit resolution Supports 16-bit resolution PWM counter Supports mask function and tri-state enable for each PWM pin Supports brake function Supports trigger ADC on the following events
RTC	<ul style="list-style-type: none"> Supports real time counter and calendar counter for RTC time and calendar check. Supports alarm time and calendar settings

- Supports alarm time and calendar mask enable settings.
- Selectable 12-hour or 24-hour time scale setting.
- Supports Leap Year indication setting.
- Supports Day of the Week counter setting.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Support clock source selectable from LXT or LIRC.

Analog Interfaces

Analog-to-Digital Converter (ADC)

- Analog input voltage range: 0 ~ AV_{DD}.
- External or internal Voltage reference input selectable.
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 16 single-end analog input channels
- 1 internal channels, they are band-gap voltage (VBG).
- Maximum ADC peripheral clock frequency is 1 MHz.
- Up to 500 KSPS sampling rate.
- Software Write 1 to ADCS bit to trig ADC start.
- External pin (STADC) trigger
- PWM trigger.

Communication Interfaces

UART

- Supports up to 2 UARTs: UART0, UART1
- Supports 2 Smart Card configuration as UART function as UART2 and UART3.
- UART baud rate clock from HIRC or HXT.
- Full-duplex asynchronous communications
- Programmable 9th bit.
- TXD and RXD pins of UART0 exchangeable via software.

I²C

- 2 sets of I²C devices
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- 7-bit addressing mode

	<ul style="list-style-type: none"> • Standard mode (100 kbps) and Fast mode (400 kbps). • Supports 8-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows • Multiple address recognition (four slave addresses with mask option) • Supports hold time programmable
SPI	<ul style="list-style-type: none"> • 2 sets of SPI devices • Supports Master or Slave mode operation • Supports MSB first or LSB first transfer sequence • Slave mode up to 12 Mhz
ISO 7816-3	<ul style="list-style-type: none"> • Two sets ISO 7816-3 device • Supports ISO 7816-3 compliant T=0, T=1 • Supports full-duplex UART mode.
GPIO	<ul style="list-style-type: none"> • Four I/O modes: • Quasi-bidirectional mode • Push-Pull Output mode • Open-Drain Output mode • Input only with high impedance mode • Schmitt trigger input / TTL mode selectable. • Each I/O pin configured as interrupt source with edge/level trigger setting • Standard interrupt pins $\overline{INT0}$ and $\overline{INT1}$. • Supports high drive and high sink current I/O • I/O pin internal pull-up or pull-down resistor enabled in input mode. • Maximum I/O Speed is 24 MHz • Enabling the pin interrupt function will also enable the wake-up function • Supports 5V-tolerance function for • ML51 Series: ML51TD1AE/ML51LD1AE/ML51SD1AD • ML54 Series: ML54MD1AE/ML54LD1AE/ML54SD1AE • ML56 Series: ML56MD1AE/ML56LD1AE/ML56SD1AE
LCD Driver	<ul style="list-style-type: none"> • Support Internal resistor bias, capacitor bias • Support programmable internal VLCD charge pump mode • 1/2, 1/3, 1/4 bias selectable • 4 COM x 32 SEG, 6 COM x 30 SEG, 8 COM x 28 SEG • Support 2.8V to 5.5V LCD operating voltage
Touch Key	<ul style="list-style-type: none"> • Supports up to 14 touch key + 1 reference pin.

- Programmable sensitivity levels for each channel.
- Programmable scanning speed for different applications.
- Supports effect when in power down mode.
- Supports single key-scan and programmable periodic key-scan.
- Programmable interrupt options for key-scan complete with/without threshold control.

ESD & EFT

ESD

- HBM 8 kV passed for ML51 32KB/16KB Flash Series.
- HBM 7 kV passed for ML51 64KB Flash/ML54/ML56 Series.

EFT

- $> \pm 4.4$ kV

Latch-up

- 150 mA passed for ML51 32KB/16KB Flash Series.
- 200 mA passed for ML51 64KB Flash/ML54/ML56 Series.

3 PART INFORMATION

3.1 ML51/ML54/ML56 Series Package Type

Package	ML51			ML54	ML56
	ML51xB	ML51xC	ML51xD	ML54xD	ML56xD
MSOP10	ML51BB9AE				
TSSOP14	ML51DB9AE				
TSSOP20	ML51FB9AE				
SOP20	ML51OB9AE				
QFN20(3x3)	ML51XB9AE				
TSSOP28	ML51EB9AE	ML51EC0AE			
SOP28	ML51UB9AE	ML51UC0AE			
LQFP32	ML51PB9AE	ML51PC0AE			
QFN33(4x4)	ML51TB9AE	ML51TC0AE	ML51TD1AE		
LQFP44				ML54MD1AE	ML56MD1AE
LQFP48			ML51LD1AE	ML54LD1AE	ML56LD1AE
LQFP64			ML51SD1AE	ML54SD1AE	ML56SD1AE

3.2 ML51/ML54/ML56 Series Selection Guide

3.2.1 ML51 Series

ML51 16KB Flash Series

Part Number		ML51							
		BB9AE	DB9AE	FB9AE	OB9AE	XB9AE	EB9AE	UB9AE	PB9AE
Flash (KB)		16	16	16	16	16	16	16	16
SRAM (KB)		1	1	1	1	1	1	2	2
ISP ROM (KB)		4	4	4	4	4	4	4	4
SPROM (bytes)		128	128	128	128	128	128	128	128
System Frequency (MHz)		24	24	24	24	24	24	24	24
GPIO		7	11	16	16	17	24	24	28
16-bit Timer		4	4	4	4	4	4	4	4
PWM		5	6	6	6	6	6	6	6
Analog Comparator		-	-	-	-	-	-	2	2
Internal Voltage Reference		-	-	-	-	-	-	Y	Y
PDMA		2	2	2	2	2	2	2	2
RTC		-	-	-	-	-	-	-	-
LCD		-	-	-	-	-	-	-	-
Connectivity	ISO 7816-3	-	1	1	1	1	1	1	1
	UART	2	2	2	2	2	2	2	2
	SPI	-	1	1	1	1	1	1	1
	I ² C	1	2	2	2	2	2	2	2
12-bit SAR ADC		2	3	6	6	6	8	8	8
Package		MSOP10	TSSOP14	TSSOP20	SOP20	QFN20	TSSOP28	SOP28	LQFP32
Note: 1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM. 2. ISO 7816-3 configurable as standard UART function.									

ML51 32KB Flash Series

Part Number		ML51					
		EC0AE	UC0AE	PC0AE	TC0AE	TC1AE	LC1AE
Flash (KB)		32	32	32	32	32	32
SRAM (KB)		2	2	2	2	2	2
ISP ROM (KB)		4	4	4	4	4	4
SPROM (bytes)		128	128	128	128	128	128
System Frequency (MHz)		24	24	24	24	24	24
GPIO		24	24	28	28	28	43
16-bit Timer		4	4	4	4	4	4
PWM		6	6	6	6	6	6
Analog Comparator		2	2	2	2	2	2
Internal Voltage Reference		Y	Y	Y	Y	Y	Y
PDMA		2	2	2	2	2	2
RTC		-	-	-	-	-	-
LCD		-	-	-	-	-	-
Connectivity	ISO 7816-3	1	1	1	1	2	2
	UART	2	2	2	2	2	2
	SPI	2 ^[3]	2 ^[3]	2	2	2	2
	I ² C	2	2	2	2	2	2
12-bit SAR ADC		8	8	8	8	9	10
Package		TSSOP28	SOP28	LQFP32	QFN33	QFN33	LQFP48
<p>Note:</p> <ol style="list-style-type: none"> 1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM. 2. ISO 7816-3 configurable as standard UART function. 3. SPI0 and SPI1 share with same SS pin in 28pin package. 							

ML51 64KB Flash Series

Part Number		ML51		
		TD1AE	LD1AE	SD1AE
Flash (KB)		64	64	64
SRAM (KB)		4	4	4
ISP ROM (KB)		4	4	4
SPROM (bytes)		128	128	128
System Frequency (MHz)		24	24	24
GPIO		28	43	56
16-bit Timer		4	4	4
PWM		6+2+2+2	6+2+2+2	6+2+2+2
Analog Comparator		2	2	2
Internal Voltage Reference		Y	Y	Y
PDMA		4	4	4
RTC		Y	Y	Y
LCD		-	-	-
Connectivity	ISO 7816-3	2	2	2
	UART	2	2	2
	SPI	2	2	2
	I ² C	2	2	2
12-bit SAR ADC		9	10	14
Package		QFN33	LQFP48	LQFP64
<p>Note:</p> <ol style="list-style-type: none"> 1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM. 2. ISO 7816-3 configurable as standard UART function. 				

3.2.2 ML54 Series

Part Number		ML54		
		MD1AE	LD1AE	SD1AE
Flash (KB)		64	64	64
SRAM (KB)		4	4	4
ISP ROM (KB)		4	4	4
SPROM (bytes)		128	128	128
System Frequency (MHz)		24	24	24
GPIO		38	42	55
16-bit Timer		4	4	4
PWM		6+2+2+2	6+2+2+2	6+2+2+2
Analog Comparator		2	2	2
Internal Voltage Reference		Y	Y	Y
PDMA		4	4	4
RTC		Y	Y	Y
LCD		8x17	8x18	8x28
		6x19	6x20	6x30
		4x21	4x22	4x32
Connectivity	ISO 7816-3	2	2	2
	UART	2	2	2
	SPI	2	2	2
	I ² C	2	2	2
12-bit SAR ADC		10	10	14
Package		LQFP44	LQFP48	LQFP64
Note: 1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM. 2. ISO 7816-3 configurable as standard UART function.				

3.2.3 ML56 Series

Part Number		ML56		
		MD1AE	LD1AE	SD1AE
Flash (KB)		64	64	64
SRAM (KB)		4	4	4
ISP ROM (KB)		4	4	4
SPROM (bytes)		128	128	128
System Frequency (MHz)		24	24	24
GPIO		38	42	55
16-bit Timer		4	4	4
PWM		6+2+2+2	6+2+2+2	6+2+2+2
Analog Comparator		2	2	2
Internal Voltage Reference		Y	Y	Y
PDMA		4	4	4
RTC		Y	Y	Y
LCD		8x17	8x18	8x28
		6x19	6x20	6x30
		4x21	4x22	4x32
Touch Key		6+1	9+1	14+1
Connectivity	ISO 7816-3	2	2	2
	UART	2	2	2
	SPI	2	2	2
	I ² C	2	2	2
12-bit SAR ADC		10	10	14
Package		LQFP44	LQFP48	LQFP64
Note: 1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM. 2. ISO 7816-3 configurable as standard UART function. 3.Touch key should define 1 key as reference pin.				

4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuration informations in chapter 1 or by using [NuTool - PinConfigure](#). The NuTool - PinConfigure contains all Nuvoton NuMicro[®] Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1.1 ML51/ML54/ML56 Series Pin Diagram

4.1.1.1 LQFP64 Package

Corresponding Part Number: ML51SD1AE/ ML54SD1AE / ML56SD1AE

ML51SD1AE

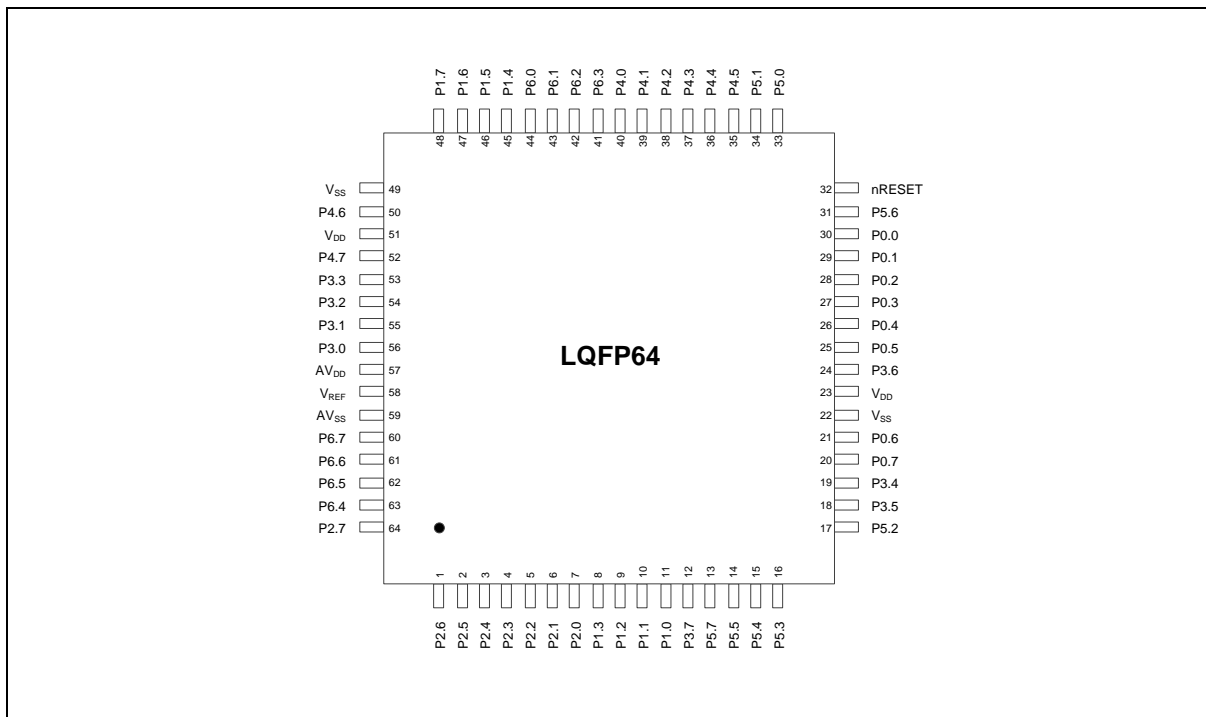


Figure 4.1-1 ML51SD1AE Pin Assignment

ML54SD1AE / ML56SD1AE

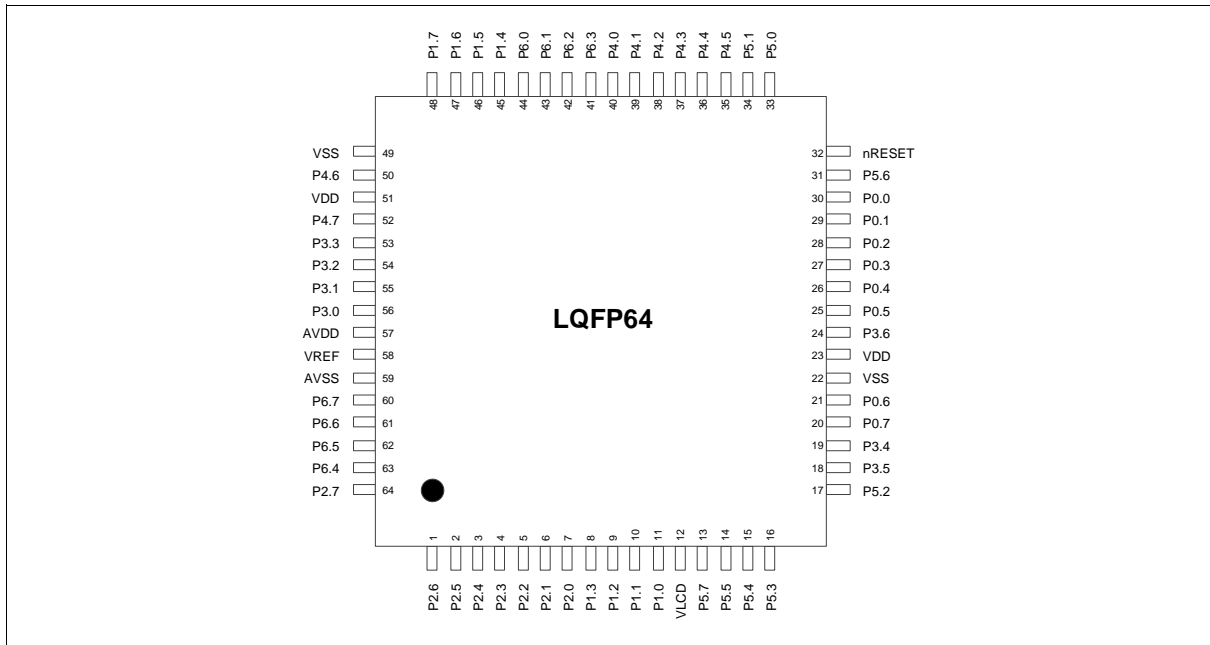


Figure 4.1-2 ML54SD1AE / ML56SD1AE Pin Assignment

4.1.1.2 LQFP48 Package

Corresponding Part Number: ML51LD1AE/ ML54LD1AE / ML56LD1AE

ML51LD1AE

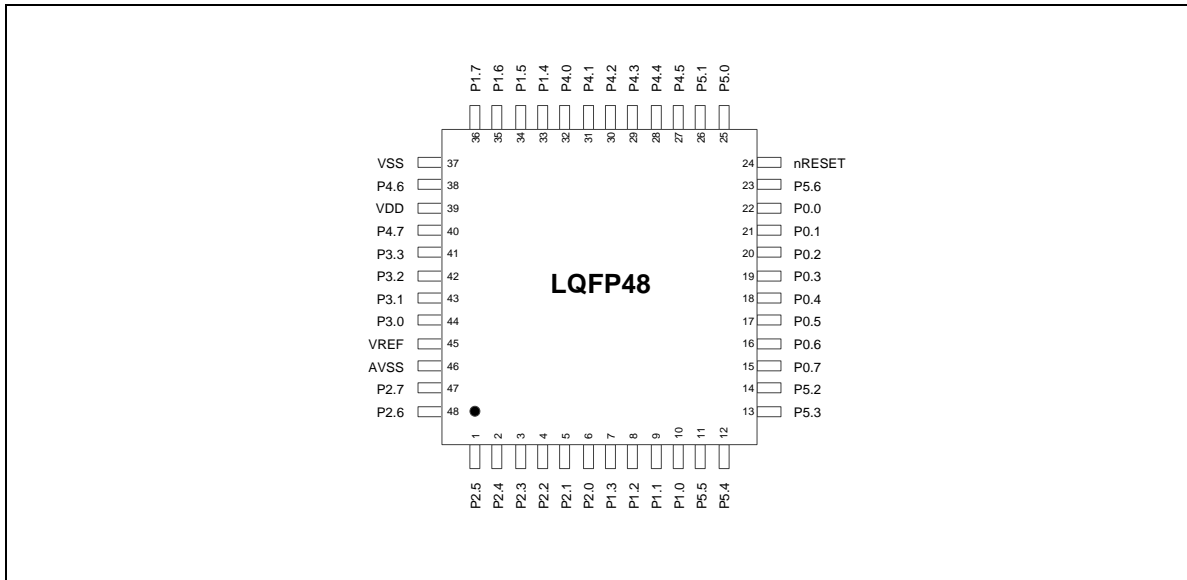


Figure 4.1-3 ML51LD1AE Pin Assignment

ML54LD1AE / ML56LD1AE

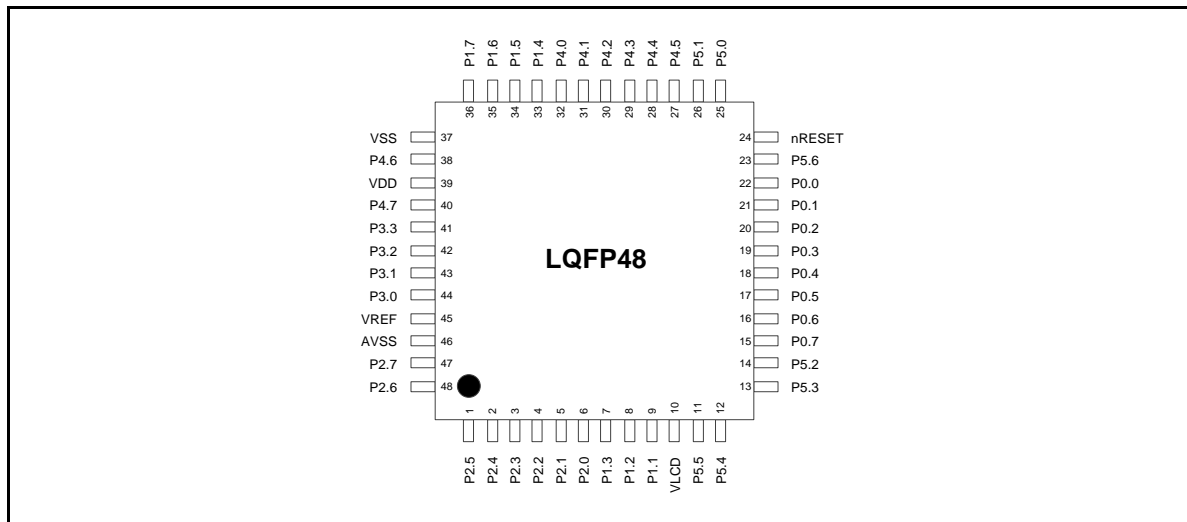


Figure 4.1-4 ML54LD1AE / ML56LD1AE Pin Assignment

4.1.1.3 LQFP44 Package

Corresponding Part Number: ML54MD1AE / ML56MD1AE

ML54MD1AE / ML56MD1AE

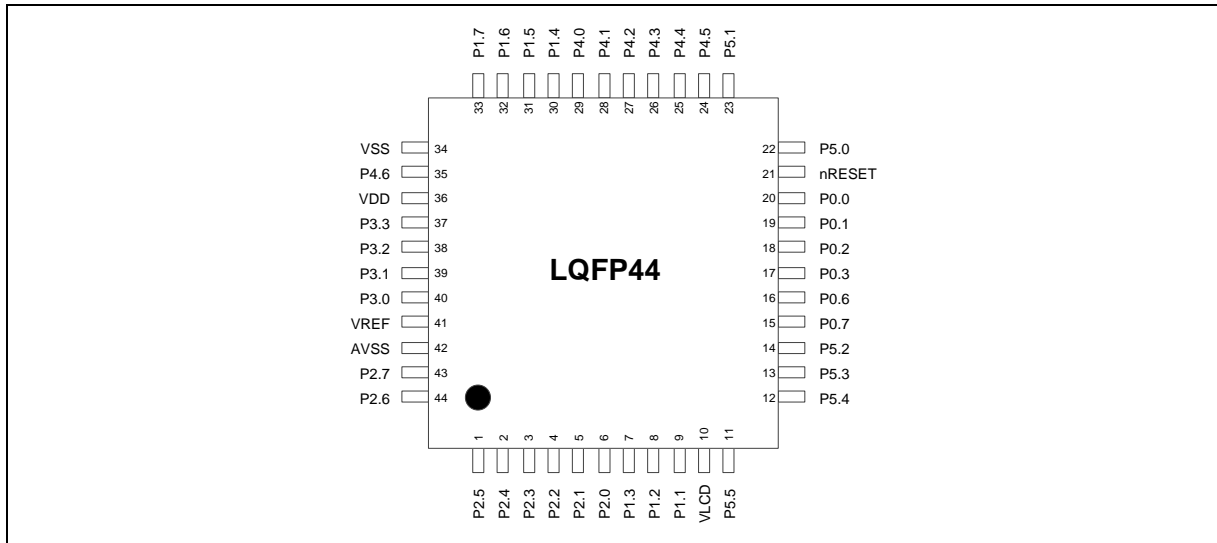


Figure 4.1-5 ML54MD1AE / ML56MD1AE Pin Assignment

4.1.1.4 QFN33 Package

Corresponding Part Number: ML51TD1AE / ML51TC0AE / ML51TB9AE

ML51TD1AE / ML51TC0AE / ML51TB9AE

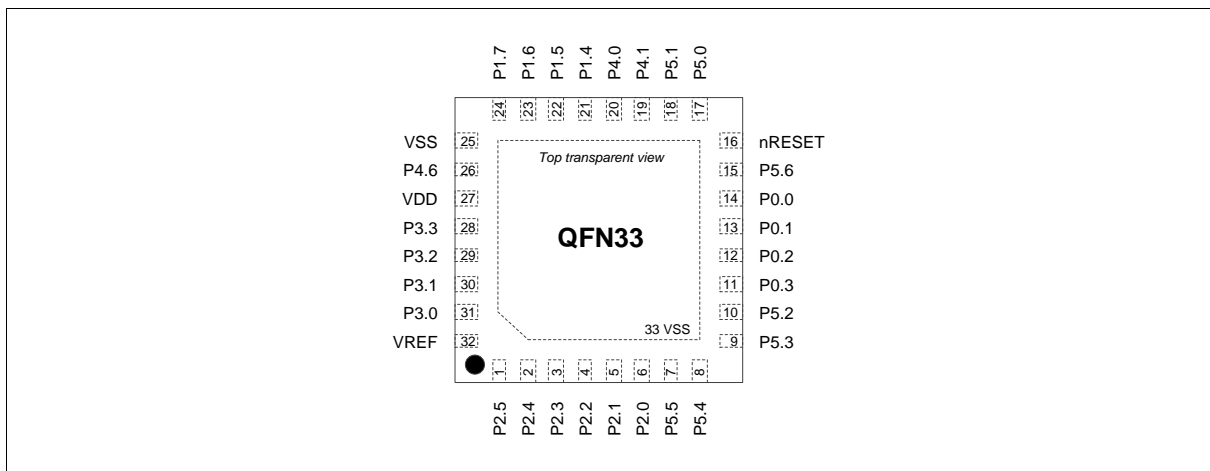


Figure 4.1-6 ML51TD1AE / ML51TC0AE / ML51TB9AE Pin Assignment

4.1.1.5 LQFP32 Package

Corresponding Part Number: ML51PC0AE / ML51PB9AE

ML51PC0AE / ML51PB9AE

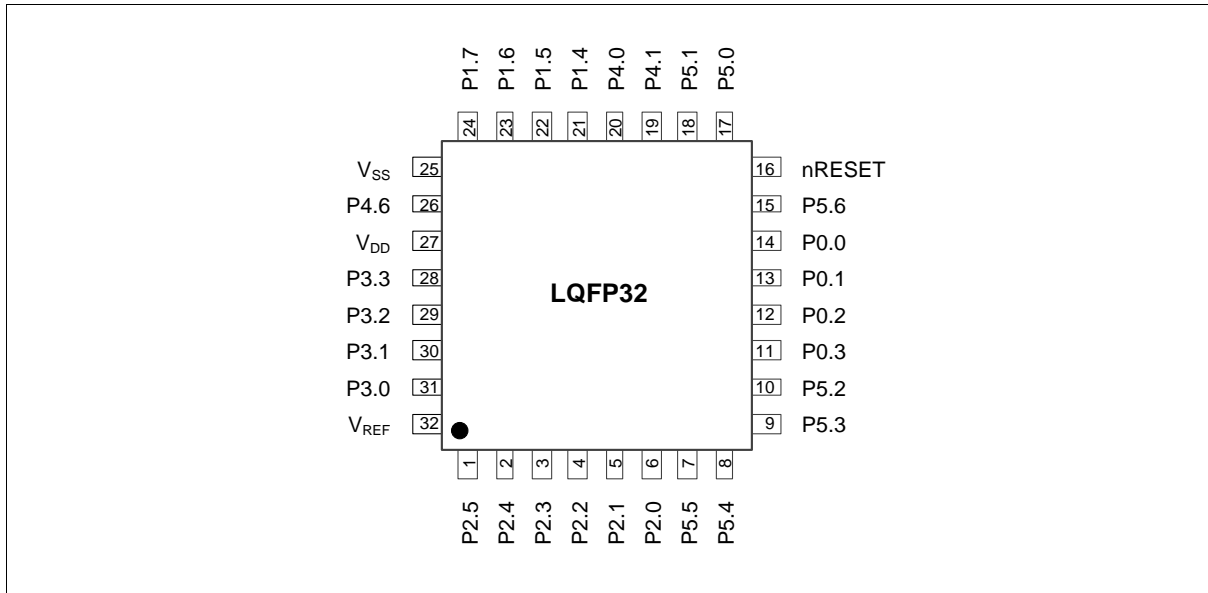


Figure 4.1-7 ML51PC0AE / ML51PB9AE Pin Assignment

4.1.1.6 TSSOP28 Package

Corresponding Part Number: ML51EC0AE / ML51EB9AE

ML51EC0AE / ML51EB9AE

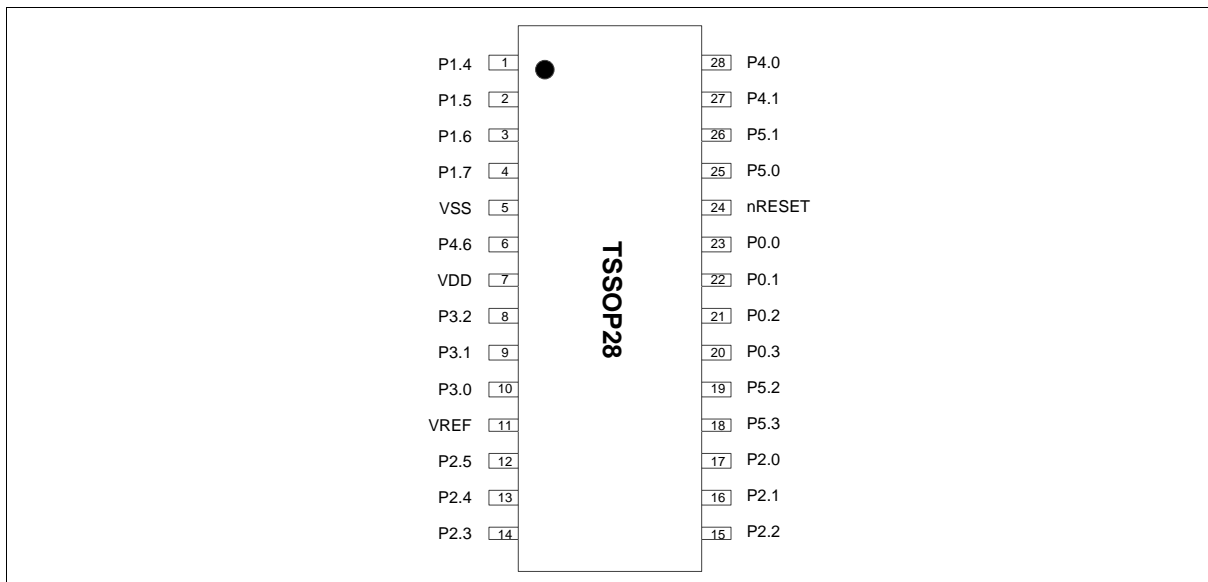


Figure 4.1-8 ML51EC0AE / ML51EB9AE Pin Assignment

4.1.1.7 SOP28 Package

Corresponding Part Number: ML51UC0AE / ML51UB9AE

ML51UC0AE / ML51UB9AE

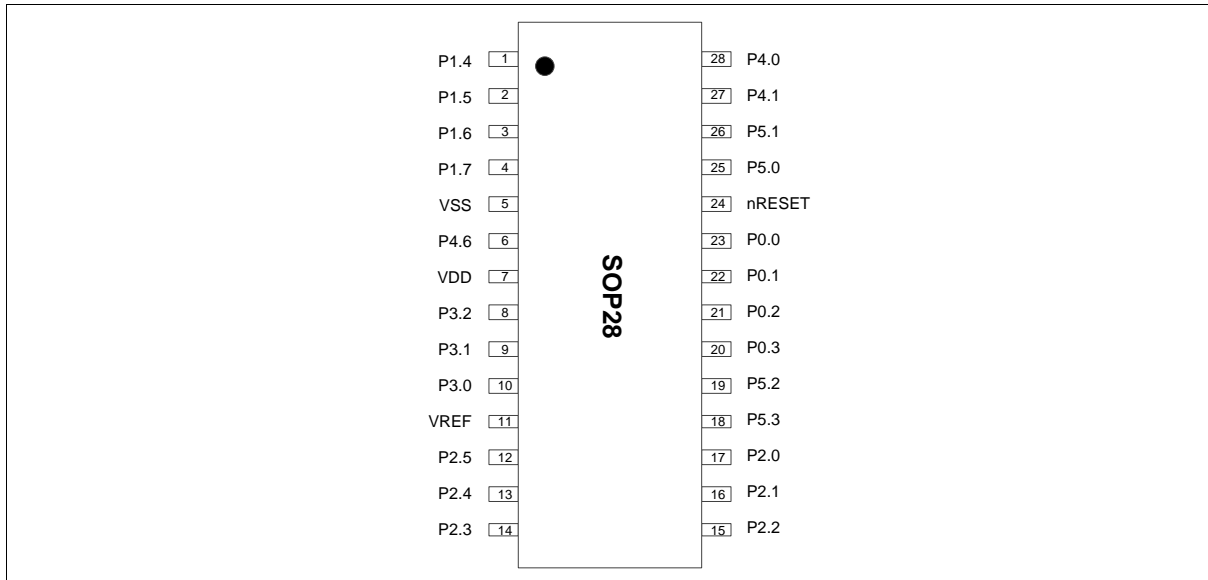


Figure 4.1-9 ML51UC0AE / ML51UB9AE Pin Assignment

4.1.1.8 TSSOP20 Package

Corresponding Part Number: ML51FB9AE

ML51FB9AE

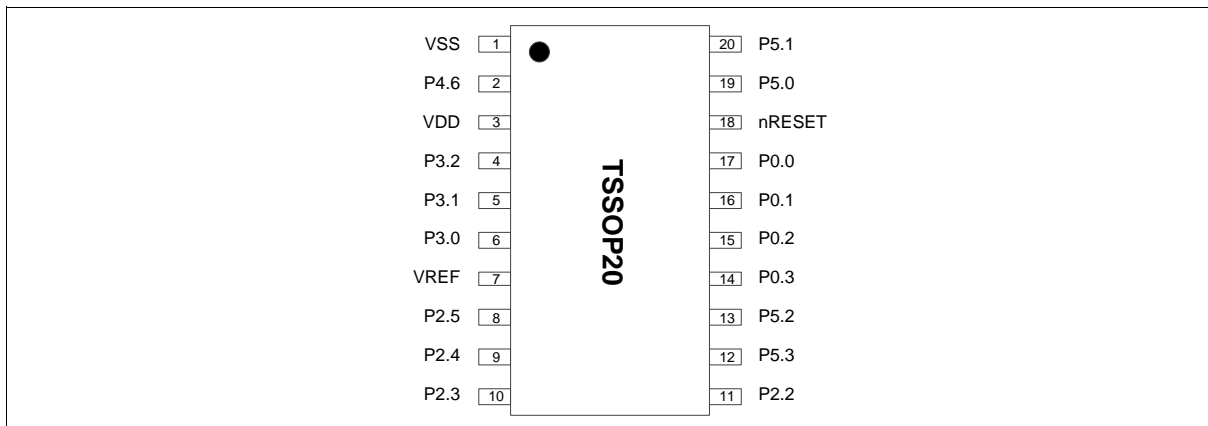


Figure 4.1-10 ML51FB9AE Pin Assignment

4.1.1.9 SOP20 Package

Corresponding Part Number: ML51OB9AE

ML51OB9AE

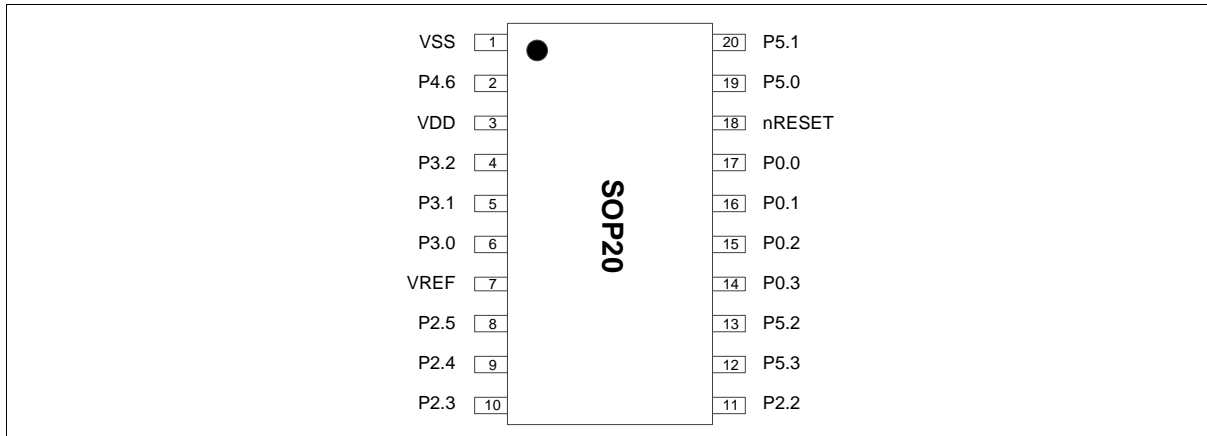


Figure 4.1-11 ML51OB9AE Pin Assignment

4.1.1.10 QFN20 Package

Corresponding Part Number: ML51XB9AE

ML51XB9AE

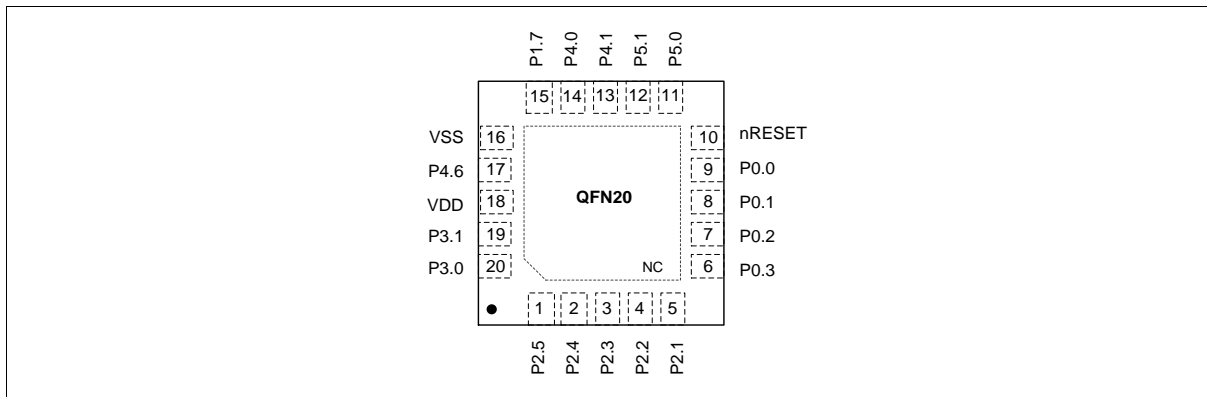


Figure 4.1-12 ML51XB9AE Pin Assignment

4.1.1.11 TSSOP14 Package

Corresponding Part Number: ML51DB9AE

ML51DB9AE

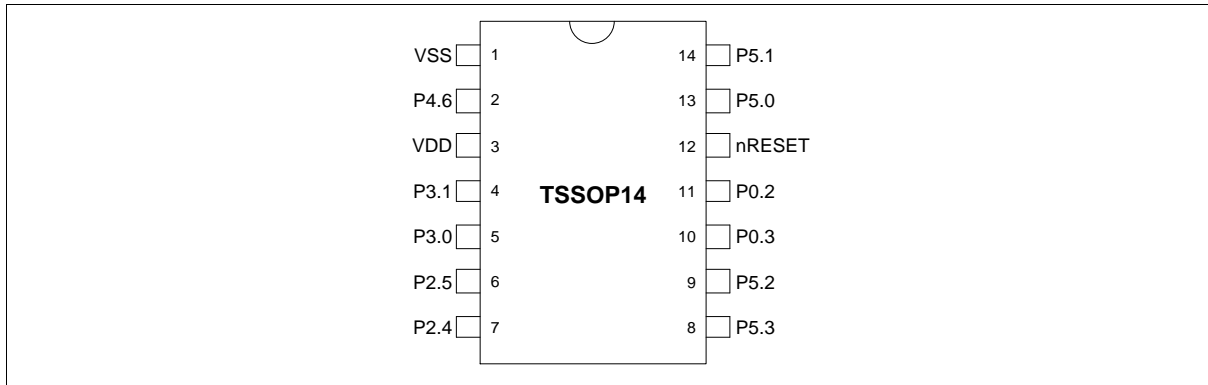


Figure 4.1-13 ML51DB9AE Pin Assignment

4.1.1.12 MSOP10 Package

Corresponding Part Number: ML51BB9AE

ML51BB9AE

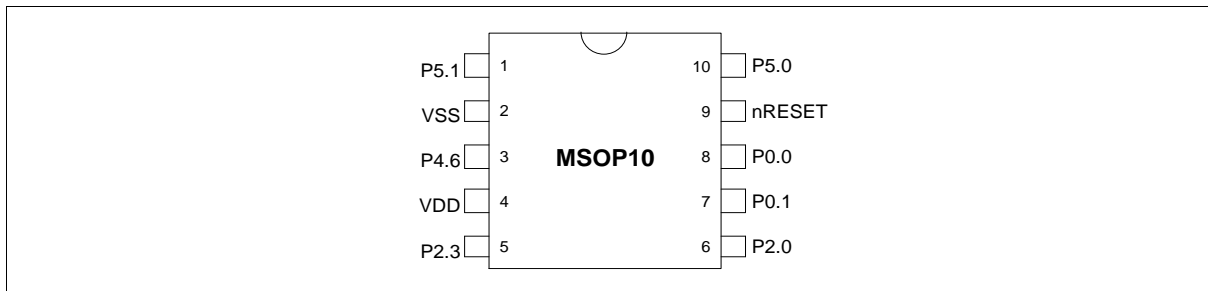


Figure 4.1-14 ML51BB9AE Pin Assignment

4.1.2 ML51/ML54/ML56 Series Multi Function Pin Diagram

4.1.2.1 LQFP64 Package

Corresponding Part Number: ML51SD1AE / ML54SD1AE / ML56SD1AE

ML51SD1AE Pin Function

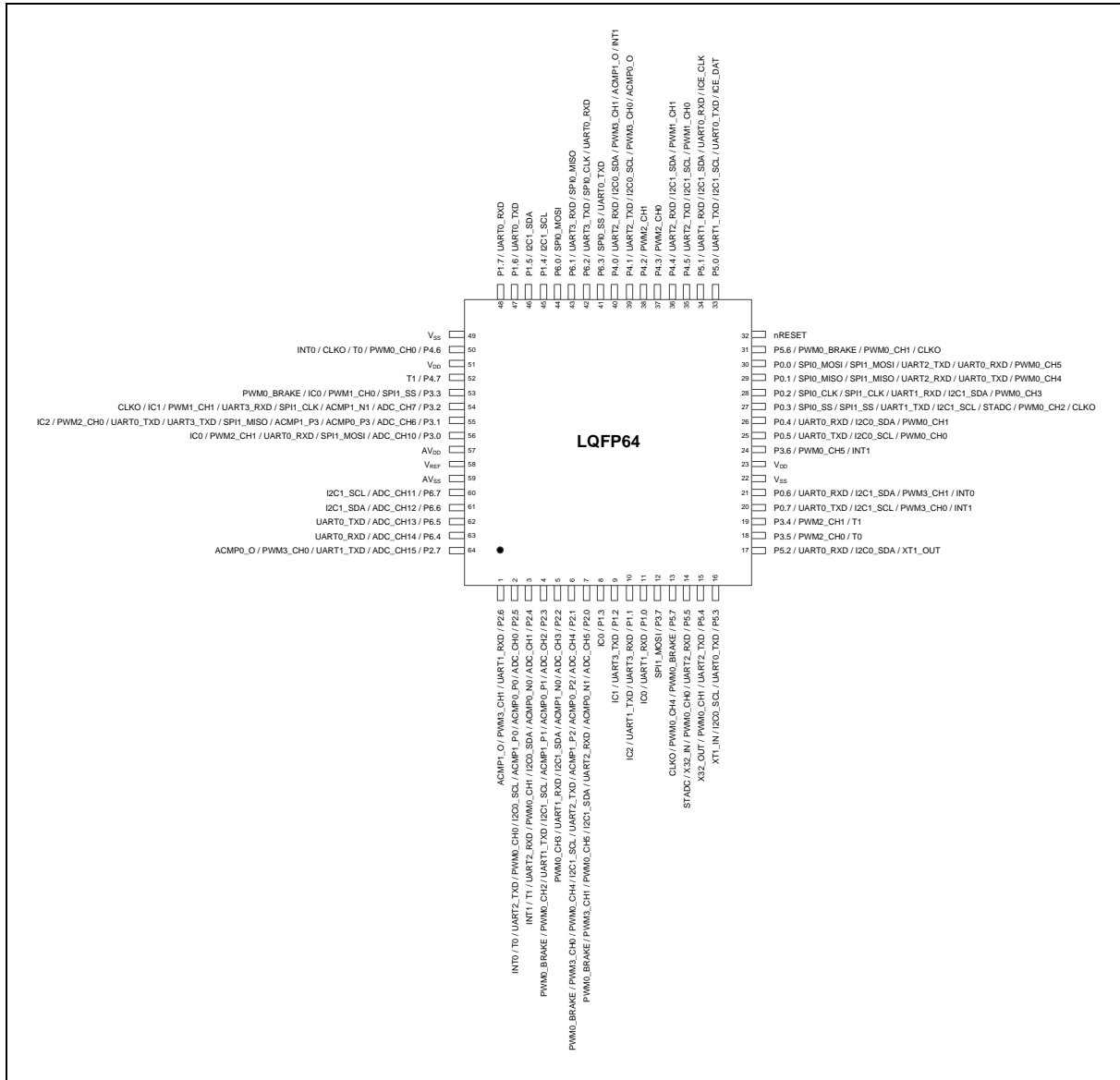


Figure 4.1-15 ML51SD1AE Multi-Function Pin assignment

Pin	ML51SD1AE Pin Function
1	P2.6 / UART1_RXD / PWM3_CH1 / ACMP1_O
2	P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INTO
3	P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
4	P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE

Pin	ML51SD1AE Pin Function
5	P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3
6	P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE
7	P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE
8	P1.3 / IC0
9	P1.2 / UART3_TXD / IC1
10	P1.1 / UART3_RXD / UART1_TXD / IC2
11	P1.0 / UART1_RXD / IC0
12	P3.7 / SPI1_MOSI
13	P5.7 / PWM0_BRAKE / PWM0_CH4 / CLKO
14	P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC
15	P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT
16	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
17	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
18	P3.5 / PWM2_CH0 / T0
19	P3.4 / PWM2_CH1 / T1
20	P0.7 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1
21	P0.6 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0
22	V _{SS}
23	V _{DD}
24	P3.6 / PWM0_CH5 / INT1
25	P0.5 / UART0_TXD / I2C0_SCL / PWM0_CH0
26	P0.4 / UART0_RXD / I2C0_SDA / PWM0_CH1
27	P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLKO
28	P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
29	P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4
30	P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5
31	P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO
32	nRESET
33	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
34	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
35	P4.5 / UART2_TXD / I2C1_SCL / PWM1_CH0
36	P4.4 / UART2_RXD / I2C1_SDA / PWM1_CH1

Pin	ML51SD1AE Pin Function
37	P4.3 / PWM2_CH0
38	P4.2 / PWM2_CH1
39	P4.1 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O
40	P4.0 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1
41	P6.3 / SPI0_SS / UART0_TXD
42	P6.2 / UART3_TXD / SPI0_CLK / UART0_RXD
43	P6.1 / UART3_RXD / SPI0_MISO
44	P6.0 / SPI0_MOSI
45	P1.4 / I2C1_SCL
46	P1.5 / I2C1_SDA
47	P1.6 / UART0_TXD
48	P1.7 / UART0_RXD
49	V _{SS}
50	P4.6 / PWM0_CH0 / T0 / CLKO / INT0
51	V _{DD}
52	P4.7 / T1
53	P3.3 / SPI1_SS / PWM1_CH0 / IC0 / PWM0_BRAKE
54	P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO
55	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2
56	P3.0 / ADC_CH10 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0
57	AV _{DD}
58	V _{REF}
59	AV _{SS}
60	P6.7 / ADC_CH11 / I2C1_SCL
61	P6.6 / ADC_CH12 / I2C1_SDA
62	P6.5 / ADC_CH13 / UART0_TXD
63	P6.4 / ADC_CH14 / UART0_RXD
64	P2.7 / ADC_CH15 / UART1_TXD / PWM3_CH0 / ACMP0_O

ML54SD1AE Pin Function

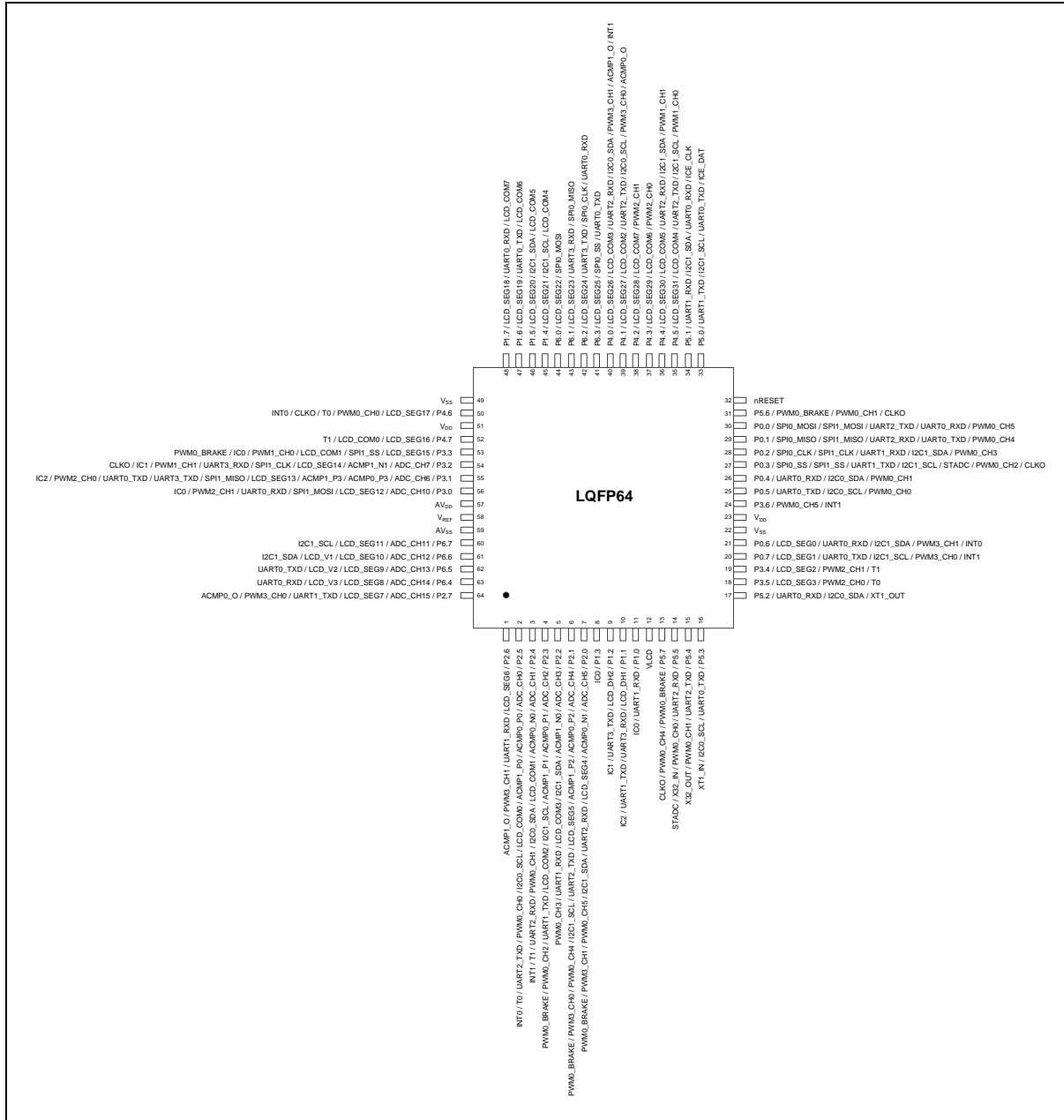


Figure 4.1-16 ML54SD1AE Multi-Function Pin assignment

Pin	ML54SD1AE Pin Function
1	P2.6 / LCD_SEG6 / UART1_RXD / PWM3_CH1 / ACMP1_O
2	P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / LCD_COM0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
3	P2.4 / ADC_CH1 / ACMP0_N0 / LCD_COM1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
4	P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / LCD_COM2 / UART1_TXD / PWM0_CH2 / PWM0_BRAKE

Pin	ML54SD1AE Pin Function
5	P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / LCD_COM3 / UART1_RXD / PWM0_CH3
6	P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / LCD_SEG5 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE
7	P2.0 / ADC_CH5 / ACMP0_N1 / LCD_SEG4 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE
8	P1.3 / IC0
9	P1.2 / LCD_DH2 / UART3_TXD / IC1
10	P1.1 / LCD_DH1 / UART3_RXD / UART1_TXD / IC2
11	P1.0 / UART1_RXD / IC0
12	VLCD
13	P5.7 / PWM0_BRAKE / PWM0_CH4 / CLKO
14	P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC
15	P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT
16	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
17	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
18	P3.5 / LCD_SEG3 / PWM2_CH0 / T0
19	P3.4 / LCD_SEG2 / PWM2_CH1 / T1
20	P0.7 / LCD_SEG1 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1
21	P0.6 / LCD_SEG0 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0
22	V _{SS}
23	V _{DD}
24	P3.6 / PWM0_CH5 / INT1
25	P0.5 / UART0_TXD / I2C0_SCL / PWM0_CH0
26	P0.4 / UART0_RXD / I2C0_SDA / PWM0_CH1
27	P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLKO
28	P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
29	P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4
30	P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5
31	P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO
32	nRESET
33	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
34	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
35	P4.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD / I2C1_SCL / PWM1_CH0

Pin	ML54SD1AE Pin Function
36	P4.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD / I2C1_SDA / PWM1_CH1
37	P4.3 / LCD_SEG29 / LCD_COM6 / PWM2_CH0
38	P4.2 / LCD_SEG28 / LCD_COM7 / PWM2_CH1
39	P4.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O
40	P4.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1
41	P6.3 / LCD_SEG25 / SPI0_SS / UART0_TXD
42	P6.2 / LCD_SEG24 / UART3_TXD / SPI0_CLK / UART0_RXD
43	P6.1 / LCD_SEG23 / UART3_RXD / SPI0_MISO
44	P6.0 / LCD_SEG22 / SPI0_MOSI
45	P1.4 / LCD_SEG21 / I2C1_SCL / LCD_COM4
46	P1.5 / LCD_SEG20 / I2C1_SDA / LCD_COM5
47	P1.6 / LCD_SEG19 / UART0_TXD / LCD_COM6
48	P1.7 / LCD_SEG18 / UART0_RXD / LCD_COM7
49	V _{SS}
50	P4.6 / LCD_SEG17 / PWM0_CH0 / T0 / CLKO / INT0
51	V _{DD}
52	P4.7 / LCD_SEG16 / LCD_COM0 / T1
53	P3.3 / LCD_SEG15 / SPI1_SS / LCD_COM1 / PWM1_CH0 / IC0 / PWM0_BRAKE
54	P3.2 / ADC_CH7 / ACMP1_N1 / LCD_SEG14 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO
55	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / LCD_SEG13 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2
56	P3.0 / ADC_CH10 / LCD_SEG12 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0
57	AV _{DD}
58	V _{REF}
59	AV _{SS}
60	P6.7 / ADC_CH11 / LCD_SEG11 / I2C1_SCL
61	P6.6 / ADC_CH12 / LCD_SEG10 / LCD_V1 / I2C1_SDA
62	P6.5 / ADC_CH13 / LCD_SEG9 / LCD_V2 / UART0_TXD
63	P6.4 / ADC_CH14 / LCD_SEG8 / LCD_V3 / UART0_RXD
64	P2.7 / ADC_CH15 / LCD_SEG7 / UART1_TXD / PWM3_CH0 / ACMP0_O

ML56SD1AE Pin Function

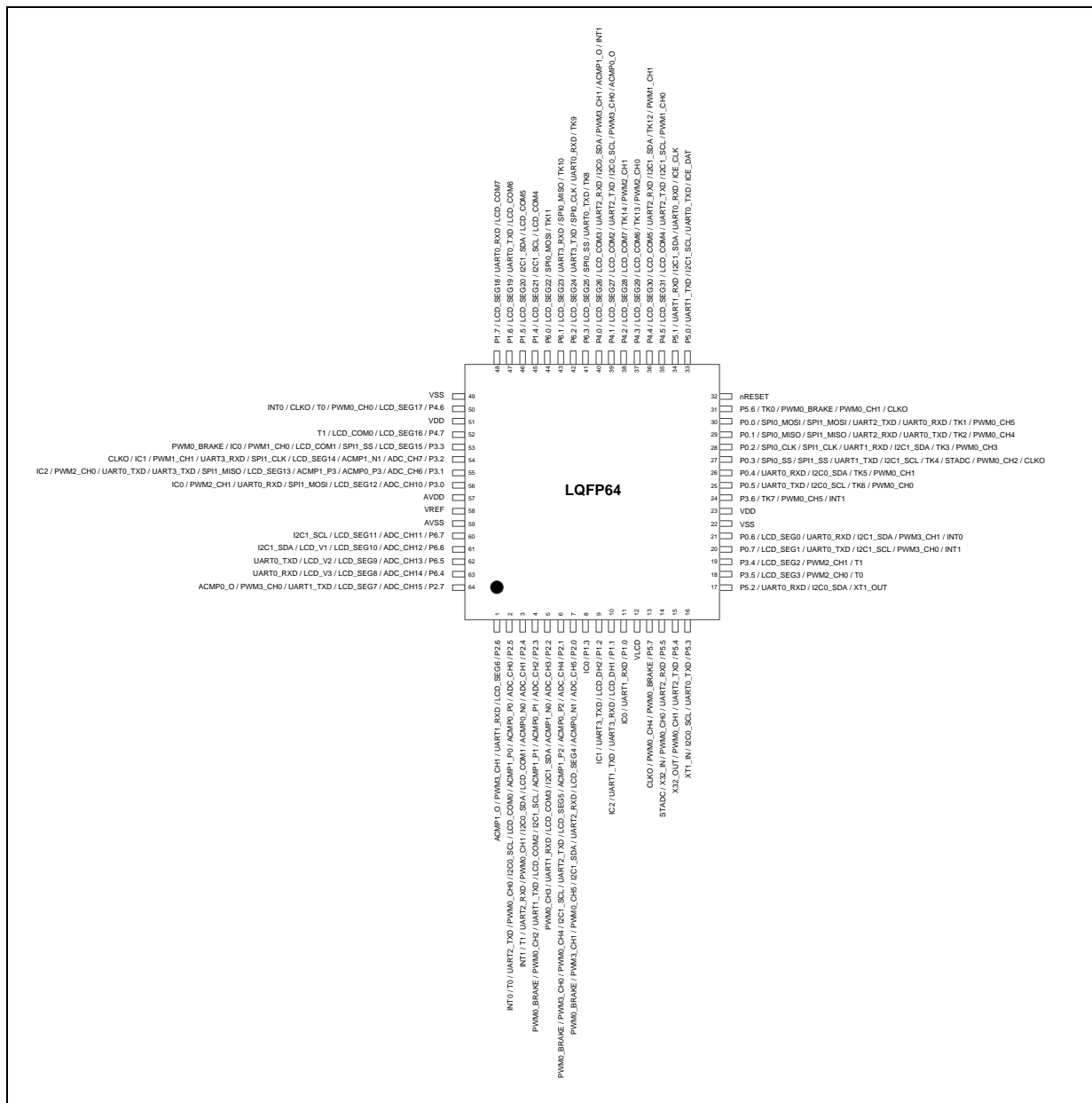


Figure 4.1-17 ML56SD1AE Multi-Function Pin assignment

Pin	ML56SD1AE Pin Function
1	P2.6/LCD_SEG6/UART1_RXD/PWM3_CH1/ACMP1_O
2	P2.5/ADC_CH0/ACMP0_P0/ACMP1_P0/LCD_COM0/I2C0_SCL/PWM0_CH0/UART2_TXD/T0/INT0
3	P2.4/ADC_CH1/ACMP0_N0/LCD_COM1/I2C0_SDA/PWM0_CH1/UART2_RXD/T1/INT1
4	P2.3/ADC_CH2/ACMP0_P1/ACMP1_P1/I2C1_SCL/LCD_COM2/UART1_TXD/PWM0_CH2/PWM0_BRAKE
5	P2.2/ADC_CH3/ACMP1_N0/I2C1_SDA/LCD_COM3/UART1_RXD/PWM0_CH3
6	P2.1/ADC_CH4/ACMP0_P2/ACMP1_P2/LCD_SEG5/UART2_TXD/I2C1_SCL/PWM0_CH4/PWM3_CH0/PWM0_BRAK

Pin	ML56SD1AE Pin Function
	E
7	P2.0/ADC_CH5/ACMP0_N1/LCD_SEG4/UART2_RXD/I2C1_SDA/PWM0_CH5/PWM3_CH1/PWM0_BRAKE
8	P1.3/IC0
9	P1.2/LCD_DH2/UART3_TXD/IC1
10	P1.1/LCD_DH1/UART3_RXD/UART1_TXD/IC2
11	P1.0/UART1_RXD/IC0
12	VLCD
13	P5.7/PWM0_BRAKE/PWM0_CH4/CLKO
14	P5.5/UART2_RXD/PWM0_CH0/X32_IN/STADC
15	P5.4/UART2_TXD/PWM0_CH1/X32_OUT
16	P5.3/UART0_TXD/I2C0_SCL/XT1_IN
17	P5.2/UART0_RXD/I2C0_SDA/XT1_OUT
18	P3.5/LCD_SEG3/PWM2_CH0/T0
19	P3.4/LCD_SEG2/PWM2_CH1/T1
20	P0.7/LCD_SEG1/UART0_TXD/I2C1_SCL/PWM3_CH0/INT1
21	P0.6/LCD_SEG0/UART0_RXD/I2C1_SDA/PWM3_CH1/INT0
22	VSS
23	VDD
24	P3.6/TK7/PWM0_CH5/INT1
25	P0.5/UART0_TXD/I2C0_SCL/TK6/PWM0_CH0
26	P0.4/UART0_RXD/I2C0_SDA/TK5/PWM0_CH1
27	P0.3/SPI0_SS/SPI1_SS/UART1_TXD/I2C1_SCL/TK4/STADC/PWM0_CH2/CLKO
28	P0.2/SPI0_CLK/SPI1_CLK/UART1_RXD/I2C1_SDA/TK3/PWM0_CH3
29	P0.1/SPI0_MISO/SPI1_MISO/UART2_RXD/UART0_TXD/TK2/PWM0_CH4
30	P0.0/SPI0_MOSI/SPI1_MOSI/UART2_TXD/UART0_RXD/TK1/PWM0_CH5
31	P5.6/TK0/PWM0_BRAKE/PWM0_CH1/CLKO
32	nRESET
33	P5.0/UART1_TXD/I2C1_SCL/UART0_TXD/ICE_DAT
34	P5.1/UART1_RXD/I2C1_SDA/UART0_RXD/ICE_CLK
35	P4.5/LCD_SEG31/LCD_COM4/UART2_TXD/I2C1_SCL/PWM1_CH0
36	P4.4/LCD_SEG30/LCD_COM5/UART2_RXD/I2C1_SDA/TK12/PWM1_CH1
37	P4.3/LCD_SEG29/LCD_COM6/TK13/PWM2_CH0
38	P4.2/LCD_SEG28/LCD_COM7/TK14/PWM2_CH1
39	P4.1/LCD_SEG27/LCD_COM2/UART2_TXD/I2C0_SCL/PWM3_CH0/ACMP0_O
40	P4.0/LCD_SEG26/LCD_COM3/UART2_RXD/I2C0_SDA/PWM3_CH1/ACMP1_O/INT1

Pin	ML56SD1AE Pin Function
41	P6.3/LCD_SEG25/SPI0_SS/UART0_TXD/TK8
42	P6.2/LCD_SEG24/UART3_TXD/SPI0_CLK/UART0_RXD/TK9
43	P6.1/LCD_SEG23/UART3_RXD/SPI0_MISO/TK10
44	P6.0/LCD_SEG22/SPI0_MOSI/TK11
45	P1.4/LCD_SEG21/I2C1_SCL/LCD_COM4
46	P1.5/LCD_SEG20/I2C1_SDA/LCD_COM5
47	P1.6/LCD_SEG19/UART0_TXD/LCD_COM6
48	P1.7/LCD_SEG18/UART0_RXD/LCD_COM7
49	VSS
50	P4.6/LCD_SEG17/PWM0_CH0/T0/CLKO/INT0
51	VDD
52	P4.7/LCD_SEG16/LCD_COM0/T1
53	P3.3/LCD_SEG15/SPI1_SS/LCD_COM1/PWM1_CH0/IC0/PWM0_BRAKE
54	P3.2/ADC_CH7/ACMP1_N1/LCD_SEG14/SPI1_CLK/UART3_RXD/PWM1_CH1/IC1/CLKO
55	P3.1/ADC_CH6/ACMP0_P3/ACMP1_P3/LCD_SEG13/SPI1_MISO/UART3_TXD/UART0_TXD/PWM2_CH0/IC2
56	P3.0/ADC_CH10/LCD_SEG12/SPI1_MOSI/UART0_RXD/PWM2_CH1/IC0
57	AV _{DD}
58	V _{REF}
59	AVSS
60	P6.7/ADC_CH11/LCD_SEG11/I2C1_SCL
61	P6.6/ADC_CH12/LCD_SEG10/LCD_V1/I2C1_SDA
62	P6.5/ADC_CH13/LCD_SEG9/LCD_V2/UART0_TXD
63	P6.4/ADC_CH14/LCD_SEG8/LCD_V3/UART0_RXD
64	P2.7/ADC_CH15/LCD_SEG7/UART1_TXD/PWM3_CH0/ACMP0_O

4.1.2.2 LQFP48 Package

Corresponding Part Number: ML51LD1AE

ML51LD1AE Pin Function

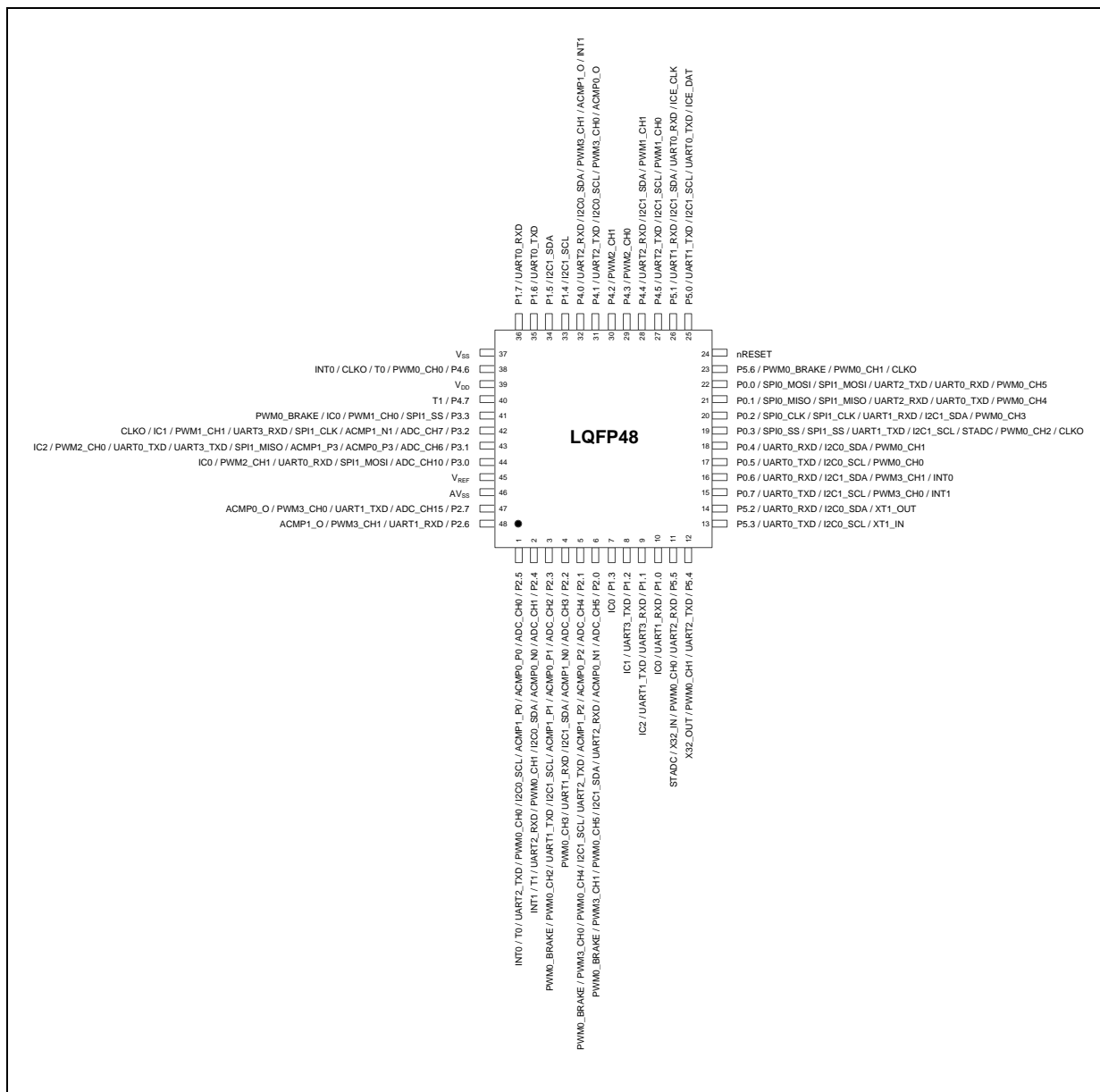


Figure 4.1-18 ML51LD1AE Multi-Function Pin assignment

Pin	ML51LD1AE Pin Function
1	P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INTO
2	P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
3	P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE

Pin	ML51LD1AE Pin Function
4	P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3
5	P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE
6	P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE
7	P1.3 / IC0
8	P1.2 / UART3_TXD / IC1
9	P1.1 / UART3_RXD / UART1_TXD / IC2
10	P1.0 / UART1_RXD / IC0
11	P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC
12	P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT
13	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
14	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
15	P0.7 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1
16	P0.6 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0
17	P0.5 / UART0_TXD / I2C0_SCL / PWM0_CH0
18	P0.4 / UART0_RXD / I2C0_SDA / PWM0_CH1
19	P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLKO
20	P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
21	P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4
22	P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5
23	P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO
24	nRESET
25	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
26	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
27	P4.5 / UART2_TXD / I2C1_SCL / PWM1_CH0
28	P4.4 / UART2_RXD / I2C1_SDA / PWM1_CH1
29	P4.3 / PWM2_CH0
30	P4.2 / PWM2_CH1
31	P4.1 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O
32	P4.0 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1
33	P1.4 / I2C1_SCL
34	P1.5 / I2C1_SDA
35	P1.6 / UART0_TXD

Pin	ML51LD1AE Pin Function
36	P1.7 / UART0_RXD
37	VSS
38	P4.6 / PWM0_CH0 / T0 / CLKO / INT0
39	V _{DD}
40	P4.7 / T1
41	P3.3 / SPI1_SS / PWM1_CH0 / IC0 / PWM0_BRAKE
42	P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO
43	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2
44	P3.0 / ADC_CH10 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0
45	V _{REF}
46	AV _{SS}
47	P2.7 / ADC_CH15 / UART1_TXD / PWM3_CH0 / ACMP0_O
48	P2.6 / UART1_RXD / PWM3_CH1 / ACMP1_O

ML54LD1AE Pin Function

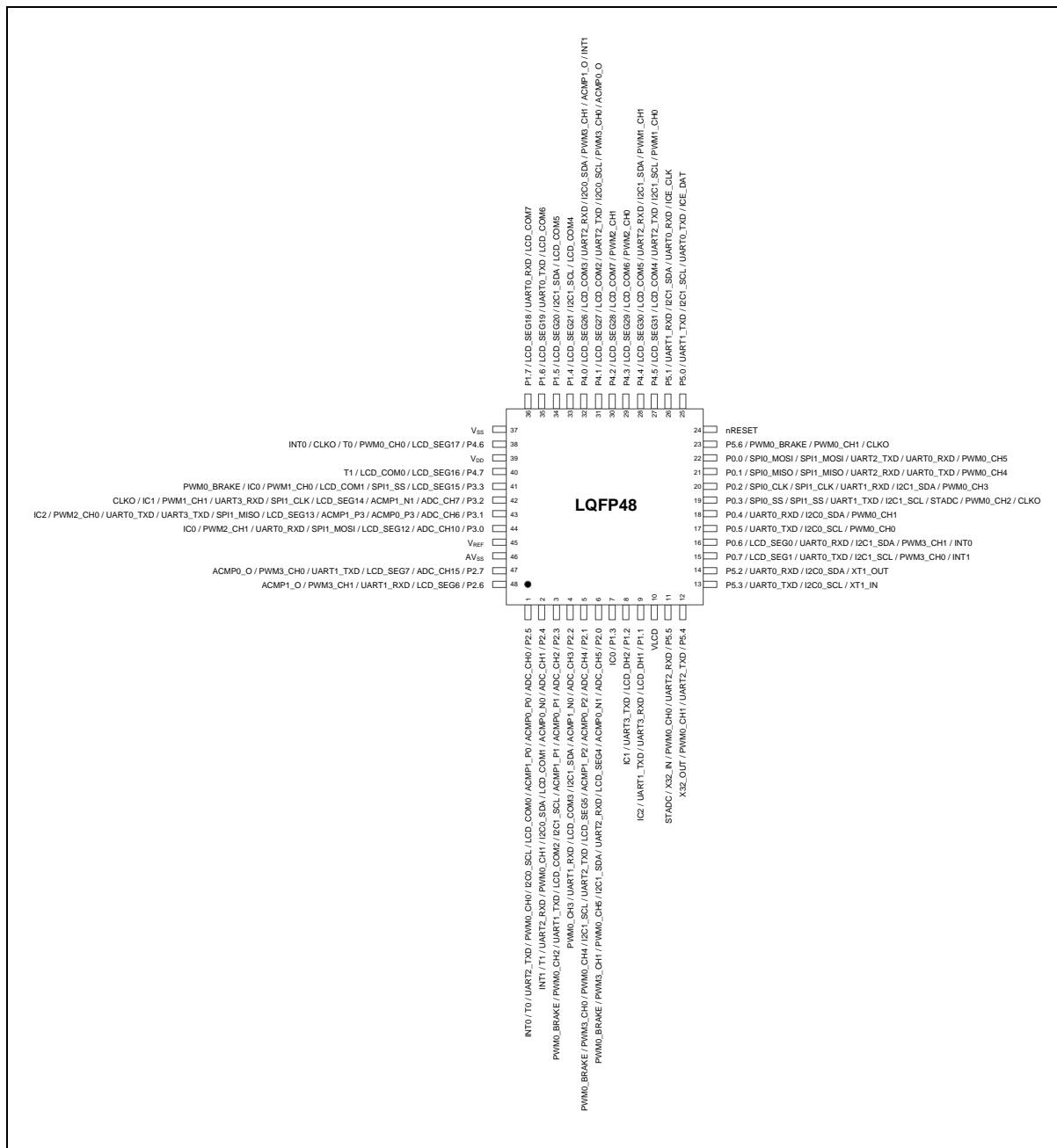


Figure 4.1-19 ML54LD1AE Multi-Function Pin assignment

Pin	ML54LD1AE Pin Function
1	P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / LCD_COM0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INTO
2	P2.4 / ADC_CH1 / ACMP0_N0 / LCD_COM1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
3	P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / LCD_COM2 / UART1_TXD / PWM0_CH2 / PWM0_BRAKE

Pin	ML54LD1AE Pin Function
4	P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / LCD_COM3 / UART1_RXD / PWM0_CH3
5	P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / LCD_SEG5 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE
6	P2.0 / ADC_CH5 / ACMP0_N1 / LCD_SEG4 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE
7	P1.3 / IC0
8	P1.2 / LCD_DH2 / UART3_TXD / IC1
9	P1.1 / LCD_DH1 / UART3_RXD / UART1_TXD / IC2
10	VLCD
11	P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC
12	P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT
13	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
14	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
15	P0.7 / LCD_SEG1 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1
16	P0.6 / LCD_SEG0 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0
17	P0.5 / UART0_TXD / I2C0_SCL / PWM0_CH0
18	P0.4 / UART0_RXD / I2C0_SDA / PWM0_CH1
19	P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLKO
20	P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
21	P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4
22	P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5
23	P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO
24	nRESET
25	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
26	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
27	P4.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD / I2C1_SCL / PWM1_CH0
28	P4.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD / I2C1_SDA / PWM1_CH1
29	P4.3 / LCD_SEG29 / LCD_COM6 / PWM2_CH0
30	P4.2 / LCD_SEG28 / LCD_COM7 / PWM2_CH1
31	P4.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O
32	P4.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1
33	P1.4 / LCD_SEG21 / I2C1_SCL / LCD_COM4
34	P1.5 / LCD_SEG20 / I2C1_SDA / LCD_COM5

Pin	ML54LD1AE Pin Function
35	P1.6 / LCD_SEG19 / UART0_TXD / LCD_COM6
36	P1.7 / LCD_SEG18 / UART0_RXD / LCD_COM7
37	VSS
38	P4.6 / LCD_SEG17 / PWM0_CH0 / T0 / CLKO / INT0
39	V _{DD}
40	P4.7 / LCD_SEG16 / LCD_COM0 / T1
41	P3.3 / LCD_SEG15 / SPI1_SS / LCD_COM1 / PWM1_CH0 / IC0 / PWM0_BRAKE
42	P3.2 / ADC_CH7 / ACMP1_N1 / LCD_SEG14 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO
43	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / LCD_SEG13 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2
44	P3.0 / ADC_CH10 / LCD_SEG12 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0
45	V _{REF}
46	AV _{SS}
47	P2.7 / ADC_CH15 / LCD_SEG7 / UART1_TXD / PWM3_CH0 / ACMP0_O
48	P2.6 / LCD_SEG6 / UART1_RXD / PWM3_CH1 / ACMP1_O

ML56LD1AE Pin Function

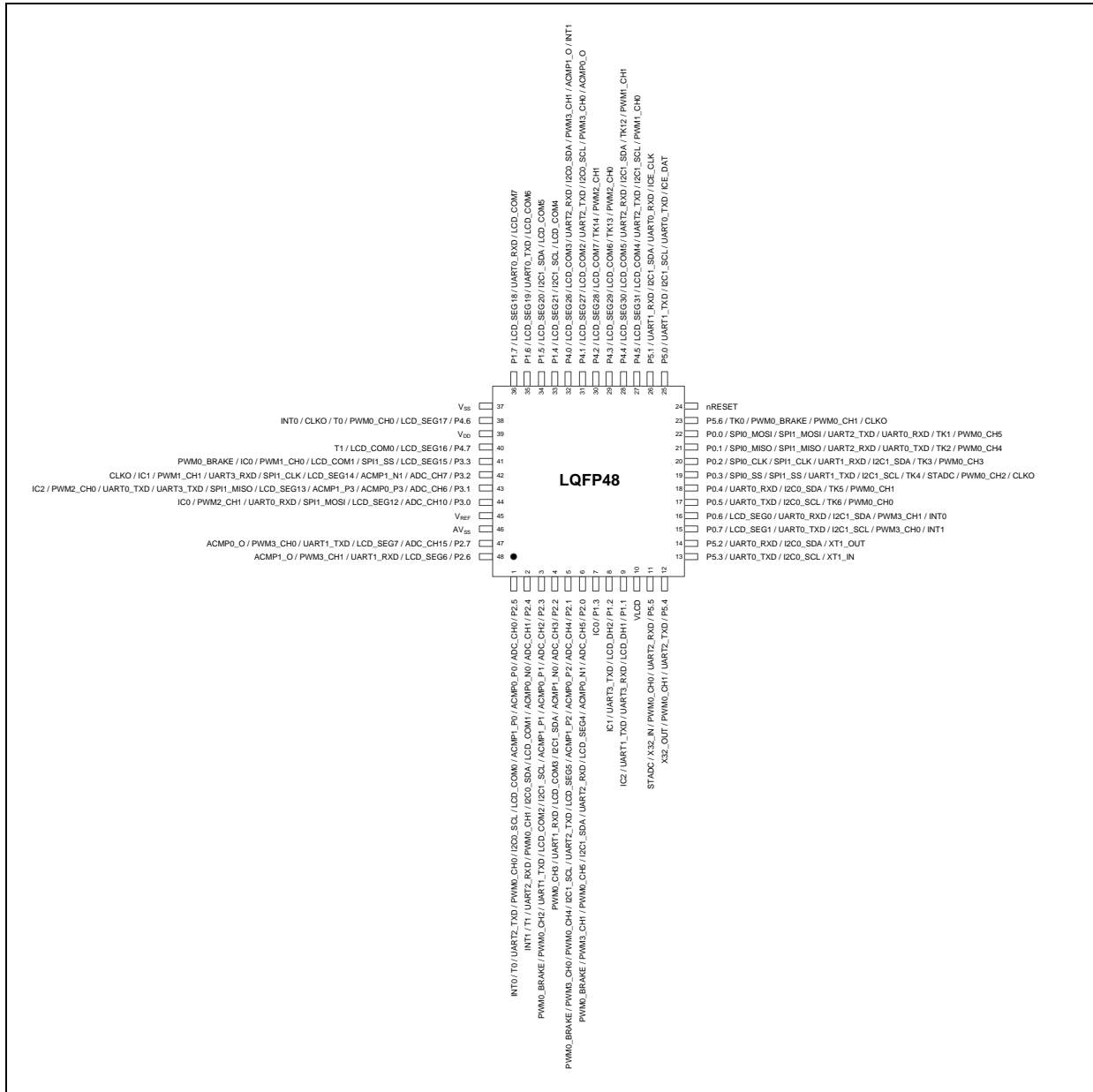


Figure 4.1-20 ML56LD1AE Multi-Function Pin assignment

Pin	ML56LD1AE/ML56LC1AE Pin Function
1	P2.5/ADC_CH0/ACMP0_P0/ACMP1_P0/LCD_COM0/I2C0_SCL/PWM0_CH0/UART2_TXD/T0/INT0
2	P2.4/ADC_CH1/ACMP0_N0/LCD_COM1/I2C0_SDA/PWM0_CH1/UART2_RXD/T1/INT1
3	P2.3/ADC_CH2/ACMP0_P1/ACMP1_P1/I2C1_SCL/LCD_COM2/UART1_TXD/PWM0_CH2/PWM0_BRAKE
4	P2.2/ADC_CH3/ACMP1_N0/I2C1_SDA/LCD_COM3/UART1_RXD/PWM0_CH3
5	P2.1/ADC_CH4/ACMP0_P2/ACMP1_P2/LCD_SEG5/UART2_TXD/I2C1_SCL/PWM0_CH4/PWM3_CH0/PWM0_BRAKE

Pin	ML56LD1AE/ML56LC1AE Pin Function
6	P2.0/ADC_CH5/ACMP0_N1/LCD_SEG4/UART2_RXD/I2C1_SDA/PWM0_CH5/PWM3_CH1/PWM0_BRAKE
7	P1.3/IC0
8	P1.2/LCD_DH2/UART3_TXD/IC1
9	P1.1/LCD_DH1/UART3_RXD/UART1_TXD/IC2
10	VLCD
11	P5.5/UART2_RXD/PWM0_CH0/X32_IN/STADC
12	P5.4/UART2_TXD/PWM0_CH1/X32_OUT
13	P5.3/UART0_TXD/I2C0_SCL/XT1_IN
14	P5.2/UART0_RXD/I2C0_SDA/XT1_OUT
15	P0.7/LCD_SEG1/UART0_TXD/I2C1_SCL/PWM3_CH0/INT1
16	P0.6/LCD_SEG0/UART0_RXD/I2C1_SDA/PWM3_CH1/INT0
17	P0.5/UART0_TXD/I2C0_SCL/TK6/PWM0_CH0
18	P0.4/UART0_RXD/I2C0_SDA/TK5/PWM0_CH1
19	P0.3/SPI0_SS/SPI1_SS/UART1_TXD/I2C1_SCL/TK4/STADC/PWM0_CH2/CLKO
20	P0.2/SPI0_CLK/SPI1_CLK/UART1_RXD/I2C1_SDA/TK3/PWM0_CH3
21	P0.1/SPI0_MISO/SPI1_MISO/UART2_RXD/UART0_TXD/TK2/PWM0_CH4
22	P0.0/SPI0_MOSI/SPI1_MOSI/UART2_TXD/UART0_RXD/TK1/PWM0_CH5
23	P5.6/TK0/PWM0_BRAKE/PWM0_CH1/CLKO
24	nRESET
25	P5.0/UART1_TXD/I2C1_SCL/UART0_TXD/ICE_DAT
26	P5.1/UART1_RXD/I2C1_SDA/UART0_RXD/ICE_CLK
27	P4.5/LCD_SEG31/LCD_COM4/UART2_TXD/I2C1_SCL/PWM1_CH0
28	P4.4/LCD_SEG30/LCD_COM5/UART2_RXD/I2C1_SDA/TK12/PWM1_CH1
29	P4.3/LCD_SEG29/LCD_COM6/TK13/PWM2_CH0
30	P4.2/LCD_SEG28/LCD_COM7/TK14/PWM2_CH1
31	P4.1/LCD_SEG27/LCD_COM2/UART2_TXD/I2C0_SCL/PWM3_CH0/ACMP0_O
32	P4.0/LCD_SEG26/LCD_COM3/UART2_RXD/I2C0_SDA/PWM3_CH1/ACMP1_O/INT1
33	P1.4/LCD_SEG21/I2C1_SCL/LCD_COM4
34	P1.5/LCD_SEG20/I2C1_SDA/LCD_COM5
35	P1.6/LCD_SEG19/UART0_TXD/LCD_COM6
36	P1.7/LCD_SEG18/UART0_RXD/LCD_COM7
37	VSS
38	P4.6/LCD_SEG17/PWM0_CH0/T0/CLKO/INT0
39	VDD

Pin	ML56LD1AE/ML56LC1AE Pin Function
40	P4.7/LCD_SEG16/LCD_COM0/T1
41	P3.3/LCD_SEG15/SPI1_SS/LCD_COM1/PWM1_CH0/IC0/PWM0_BRAKE
42	P3.2/ADC_CH7/ACMP1_N1/LCD_SEG14/SPI1_CLK/UART3_RXD/PWM1_CH1/IC1/CLKO
43	P3.1/ADC_CH6/ACMP0_P3/ACMP1_P3/LCD_SEG13/SPI1_MISO/UART3_TXD/UART0_TXD/PWM2_CH0/IC2
44	P3.0/ADC_CH10/LCD_SEG12/SPI1_MOSI/UART0_RXD/PWM2_CH1/IC0
45	V _{REF}
46	AVSS
47	P2.7/ADC_CH15/LCD_SEG7/UART1_TXD/PWM3_CH0/ACMP0_O
48	P2.6/LCD_SEG6/UART1_RXD/PWM3_CH1/ACMP1_O

4.1.2.3 LQFP44 Package

ML54MD1AE Pin Function

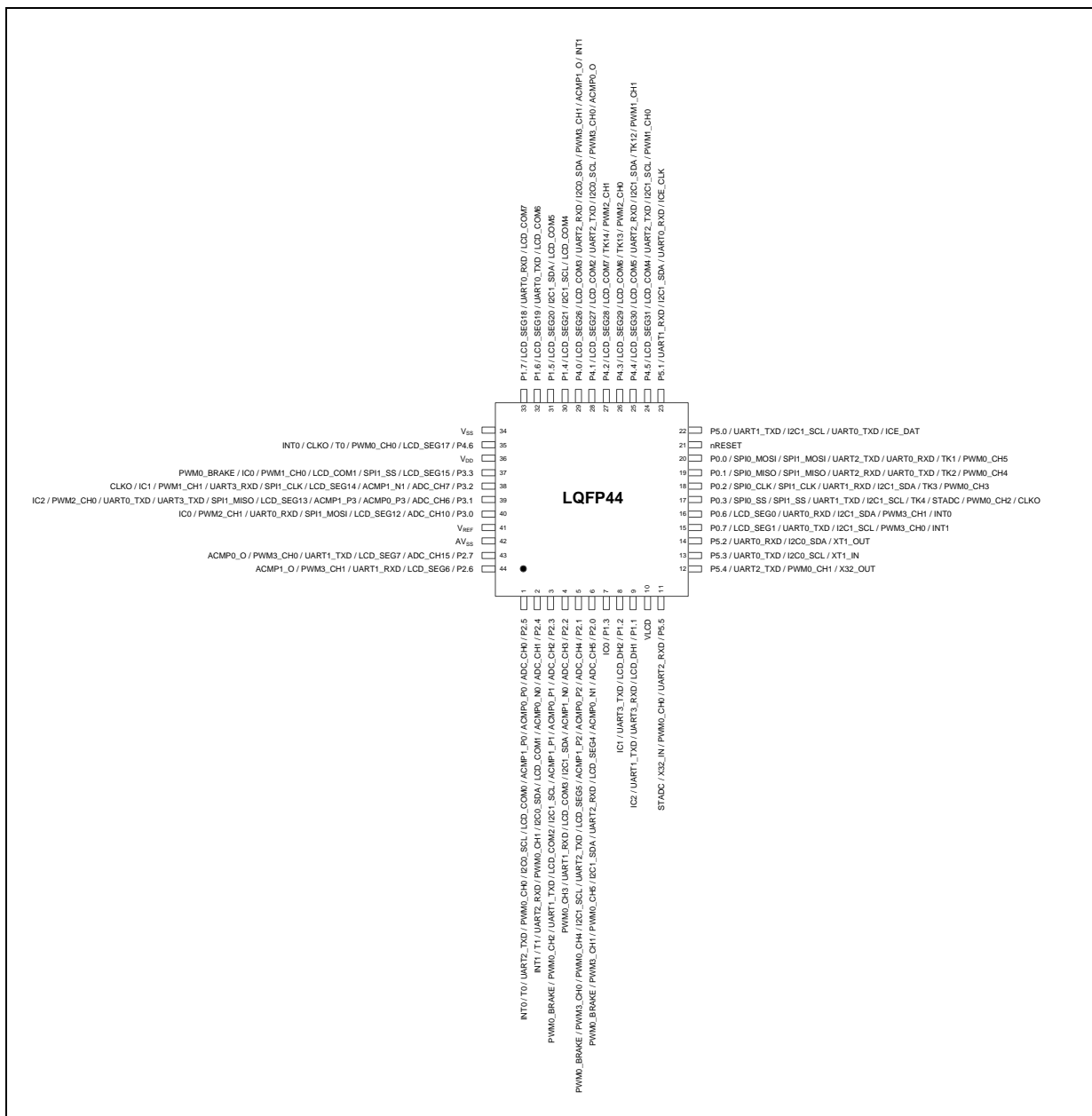


Figure 4.1-21 ML54MD1AE Multi-Function Pin assignment

Pin	ML54MD1AE Pin Function
1	P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / LCD_COM0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
2	P2.4 / ADC_CH1 / ACMP0_N0 / LCD_COM1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
3	P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / LCD_COM2 / UART1_TXD / PWM0_CH2 / PWM0_BRAKE

Pin	ML54MD1AE Pin Function
4	P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / LCD_COM3 / UART1_RXD / PWM0_CH3
5	P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / LCD_SEG5 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM3_CH0 / PWM0_BRAKE
6	P2.0 / ADC_CH5 / ACMP0_N1 / LCD_SEG4 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM3_CH1 / PWM0_BRAKE
7	P1.3 / IC0
8	P1.2 / LCD_DH2 / UART3_TXD / IC1
9	P1.1 / LCD_DH1 / UART3_RXD / UART1_TXD / IC2
10	VLCD
11	P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC
12	P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT
13	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
14	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
15	P0.7 / LCD_SEG1 / UART0_TXD / I2C1_SCL / PWM3_CH0 / INT1
16	P0.6 / LCD_SEG0 / UART0_RXD / I2C1_SDA / PWM3_CH1 / INT0
17	P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLKO
18	P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
19	P0.1 / SPI0_MISO / SPI1_MISO / UART2_RXD / UART0_TXD / PWM0_CH4
20	P0.0 / SPI0_MOSI / SPI1_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5
21	nRESET
22	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
23	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
24	P4.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD / I2C1_SCL / PWM1_CH0
25	P4.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD / I2C1_SDA / PWM1_CH1
26	P4.3 / LCD_SEG29 / LCD_COM6 / PWM2_CH0
27	P4.2 / LCD_SEG28 / LCD_COM7 / PWM2_CH1
28	P4.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / PWM3_CH0 / ACMP0_O
29	P4.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / PWM3_CH1 / ACMP1_O / INT1
30	P1.4 / LCD_SEG21 / I2C1_SCL / LCD_COM4
31	P1.5 / LCD_SEG20 / I2C1_SDA / LCD_COM5
32	P1.6 / LCD_SEG19 / UART0_TXD / LCD_COM6
33	P1.7 / LCD_SEG18 / UART0_RXD / LCD_COM7
34	V _{SS}

Pin	ML54MD1AE Pin Function
35	P4.6 / LCD_SEG17 / PWM0_CH0 / T0 / CLKO / INT0
36	V _{DD}
37	P3.3 / LCD_SEG15 / SPI1_SS / LCD_COM1 / PWM1_CH0 / IC0 / PWM0_BRAKE
38	P3.2 / ADC_CH7 / ACMP1_N1 / LCD_SEG14 / SPI1_CLK / UART3_RXD / PWM1_CH1 / IC1 / CLKO
39	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / LCD_SEG13 / SPI1_MISO / UART3_TXD / UART0_TXD / PWM2_CH0 / IC2
40	P3.0 / ADC_CH10 / LCD_SEG12 / SPI1_MOSI / UART0_RXD / PWM2_CH1 / IC0
41	V _{REF}
42	AV _{SS}
43	P2.7 / ADC_CH15 / LCD_SEG7 / UART1_TXD / PWM3_CH0 / ACMP0_O
44	P2.6 / LCD_SEG6 / UART1_RXD / PWM3_CH1 / ACMP1_O

ML56MD1AE Pin Function

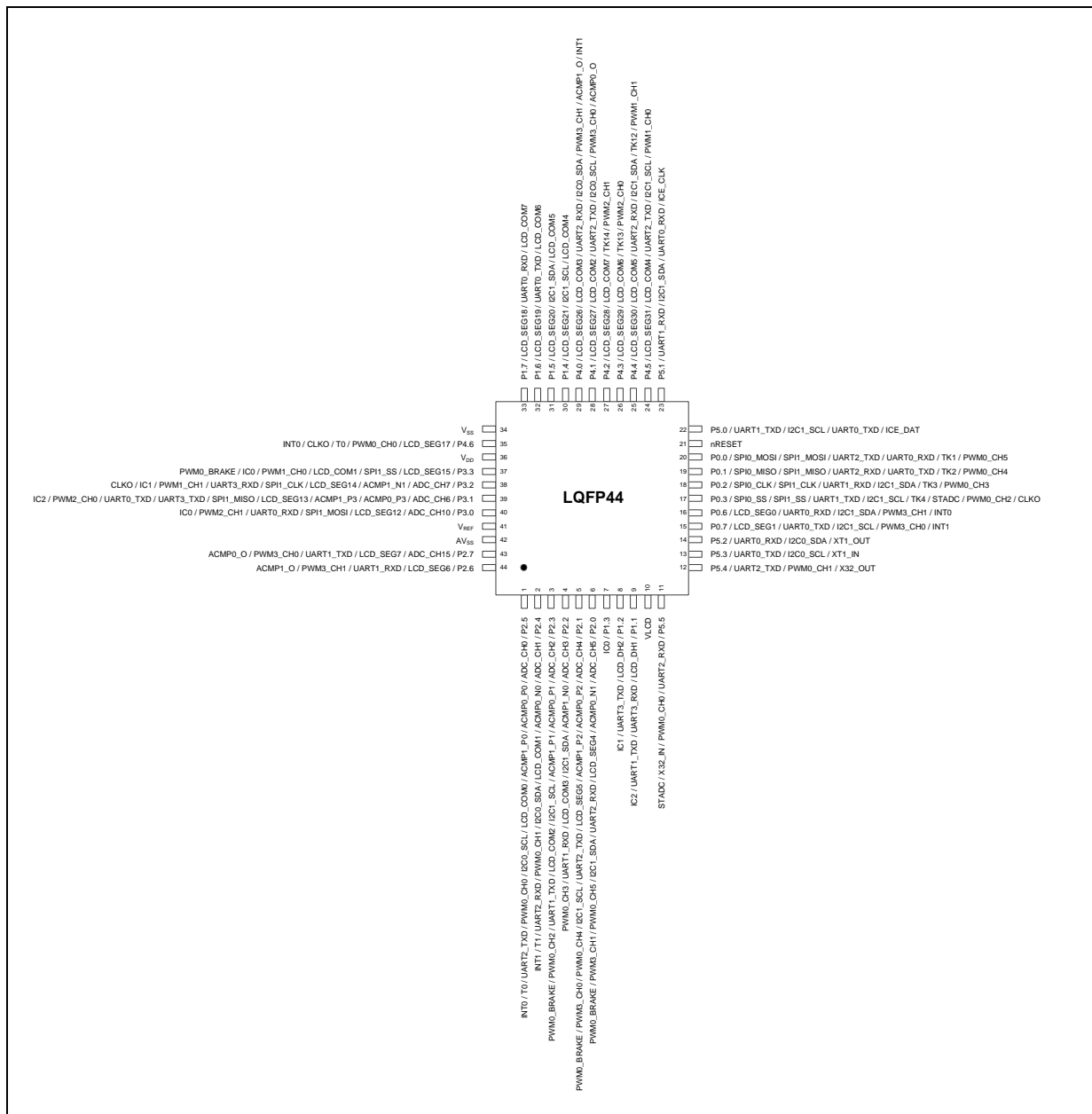


Figure 4.1-22 ML56MD1AE Multi-Function Pin assignment

Pin	ML56MD1AE Pin Function
1	P2.5/ADC_CH0/ACMP0_P0/ACMP1_P0/LCD_COM0/I2C0_SCL/PWM0_CH0/UART2_TXD/T0/INT0
2	P2.4/ADC_CH1/ACMP0_N0/LCD_COM1/I2C0_SDA/PWM0_CH1/UART2_RXD/T1/INT1
3	P2.3/ADC_CH2/ACMP0_P1/ACMP1_P1/I2C1_SCL/LCD_COM2/UART1_TXD/PWM0_CH2/PWM0_BRAKE
4	P2.2/ADC_CH3/ACMP1_N0/I2C1_SDA/LCD_COM3/UART1_RXD/PWM0_CH3
5	P2.1/ADC_CH4/ACMP0_P2/ACMP1_P2/LCD_SEG5/UART2_TXD/I2C1_SCL/PWM0_CH4/PWM3_CH0/PWM0_BRAKE

Pin	ML56MD1AE Pin Function
6	P2.0/ADC_CH5/ACMP0_N1/LCD_SEG4/UART2_RXD/I2C1_SDA/PWM0_CH5/PWM3_CH1/PWM0_BRAKE
7	P1.3/IC0
8	P1.2/LCD_DH2/UART3_TXD/IC1
9	P1.1/LCD_DH1/UART3_RXD/UART1_TXD/IC2
10	VLCD
11	P5.5/UART2_RXD/PWM0_CH0/X32_IN/STADC
12	P5.4/UART2_TXD/PWM0_CH1/X32_OUT
13	P5.3/UART0_TXD/I2C0_SCL/XT1_IN
14	P5.2/UART0_RXD/I2C0_SDA/XT1_OUT
15	P0.7/LCD_SEG1/UART0_TXD/I2C1_SCL/PWM3_CH0/INT1
16	P0.6/LCD_SEG0/UART0_RXD/I2C1_SDA/PWM3_CH1/INT0
17	P0.3/SPI0_SS/SPI1_SS/UART1_TXD/I2C1_SCL/TK4/STADC/PWM0_CH2/CLKO
18	P0.2/SPI0_CLK/SPI1_CLK/UART1_RXD/I2C1_SDA/TK3/PWM0_CH3
19	P0.1/SPI0_MISO/SPI1_MISO/UART2_RXD/UART0_TXD/TK2/PWM0_CH4
20	P0.0/SPI0_MOSI/SPI1_MOSI/UART2_TXD/UART0_RXD/TK1/PWM0_CH5
21	nRESET
22	P5.0/UART1_TXD/I2C1_SCL/UART0_TXD/ICE_DAT
23	P5.1/UART1_RXD/I2C1_SDA/UART0_RXD/ICE_CLK
24	P4.5/LCD_SEG31/LCD_COM4/UART2_TXD/I2C1_SCL/PWM1_CH0
25	P4.4/LCD_SEG30/LCD_COM5/UART2_RXD/I2C1_SDA/TK12/PWM1_CH1
26	P4.3/LCD_SEG29/LCD_COM6/TK13/PWM2_CH0
27	P4.2/LCD_SEG28/LCD_COM7/TK14/PWM2_CH1
28	P4.1/LCD_SEG27/LCD_COM2/UART2_TXD/I2C0_SCL/PWM3_CH0/ACMP0_O
29	P4.0/LCD_SEG26/LCD_COM3/UART2_RXD/I2C0_SDA/PWM3_CH1/ACMP1_O/INT1
30	P1.4/LCD_SEG21/I2C1_SCL/LCD_COM4
31	P1.5/LCD_SEG20/I2C1_SDA/LCD_COM5
32	P1.6/LCD_SEG19/UART0_TXD/LCD_COM6
33	P1.7/LCD_SEG18/UART0_RXD/LCD_COM7
34	VSS
35	P4.6/LCD_SEG17/PWM0_CH0/T0/CLKO/INT0
36	VDD
37	P3.3/LCD_SEG15/SPI1_SS/LCD_COM1/PWM1_CH0/IC0/PWM0_BRAKE
38	P3.2/ADC_CH7/ACMP1_N1/LCD_SEG14/SPI1_CLK/UART3_RXD/PWM1_CH1/IC1/CLKO
39	P3.1/ADC_CH6/ACMP0_P3/ACMP1_P3/LCD_SEG13/SPI1_MISO/UART3_TXD/UART0_TXD/PWM2_CH0/IC2

Pin	ML56MD1AE Pin Function
40	P3.0/ADC_CH10/LCD_SEG12/SPI1_MOSI/UART0_RXD/PWM2_CH1/IC0
41	V _{REF}
42	AVSS
43	P2.7/ADC_CH15/LCD_SEG7/UART1_TXD/PWM3_CH0/ACMP0_O
44	P2.6/LCD_SEG6/UART1_RXD/PWM3_CH1/ACMP1_O

4.1.2.4 QFN33 Package

ML51TD1AE Pin Function

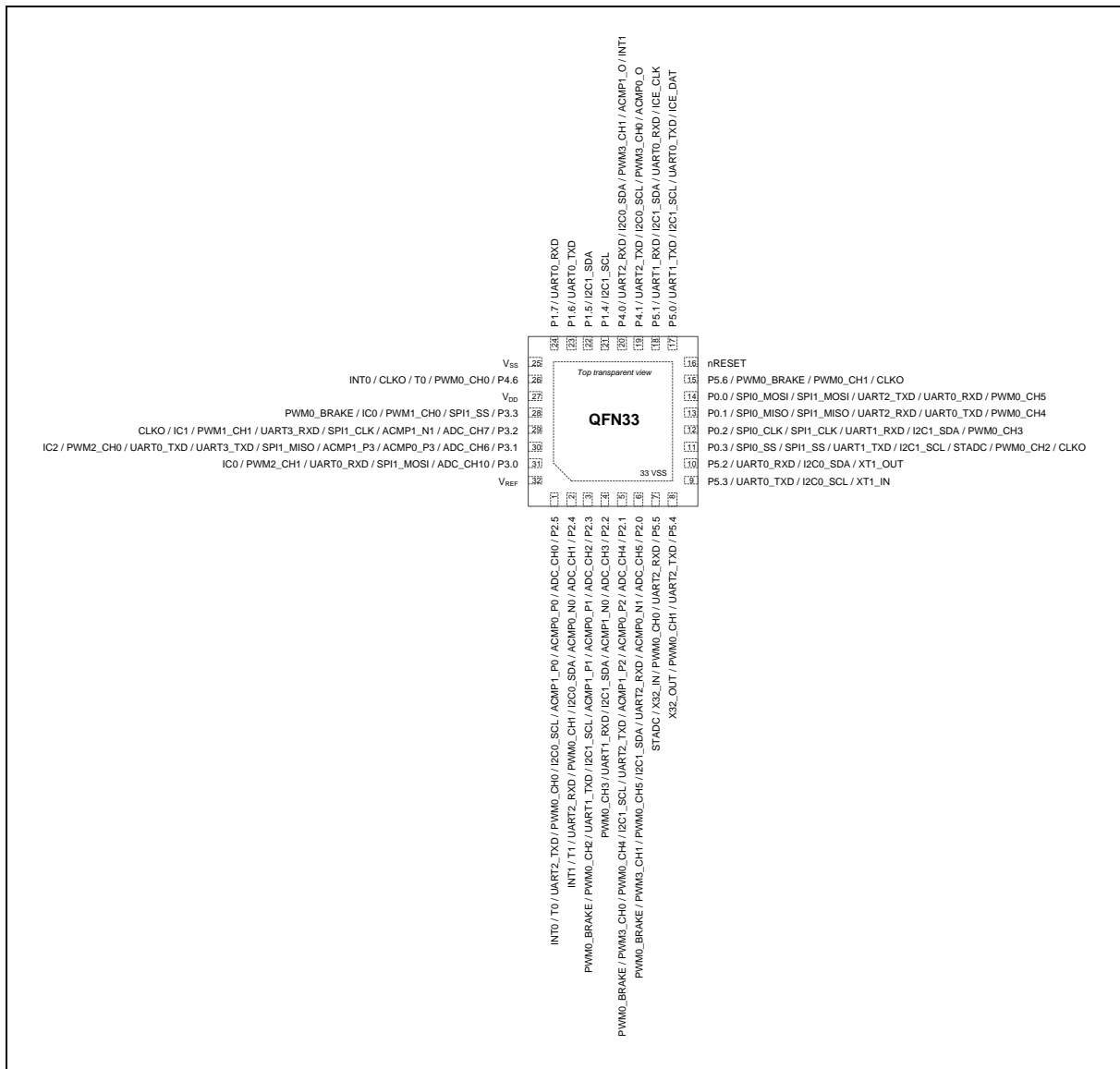


Figure 4.1-23 ML51TD1AE Multi-Function Pin assignment

Pin	ML56TD1AE Pin Function
1	P2.5/ADC_CH0/ACMP0_P0/ACMP1_P0/LCD_COM0/I2C0_SCL/PWM0_CH0/UART2_TXD/T0/INT0
2	P2.4/ADC_CH1/ACMP0_N0/LCD_COM1/I2C0_SDA/PWM0_CH1/UART2_RXD/T1/INT1
3	P2.3/ADC_CH2/ACMP0_P1/ACMP1_P1/I2C1_SCL/LCD_COM2/UART1_TXD/PWM0_CH2/PWM0_BRAKE
4	P2.2/ADC_CH3/ACMP1_N0/I2C1_SDA/LCD_COM3/UART1_RXD/PWM0_CH3
5	P2.1/ADC_CH4/ACMP0_P2/ACMP1_P2/LCD_SEG5/UART2_TXD/I2C1_SCL/PWM0_CH4/PWM3_CH0/PWM0_BRAKE
6	P2.0/ADC_CH5/ACMP0_N1/LCD_SEG4/UART2_RXD/I2C1_SDA/PWM0_CH5/PWM3_CH1/PWM0_BRAKE

Pin	ML56TD1AE Pin Function
7	P5.5/UART2_RXD/PWM0_CH0/X32_IN/STADC
8	P5.4/UART2_TXD/PWM0_CH1/X32_OUT
9	P5.3/UART0_TXD/I2C0_SCL/XT1_IN
10	P5.2/UART0_RXD/I2C0_SDA/XT1_OUT
11	P0.3/SPI0_SS/SPI1_SS/UART1_TXD/I2C1_SCL/TK4/STADC/PWM0_CH2/CLKO
12	P0.2/SPI0_CLK/SPI1_CLK/UART1_RXD/I2C1_SDA/TK3/PWM0_CH3
13	P0.1/SPI0_MISO/SPI1_MISO/UART2_RXD/UART0_TXD/TK2/PWM0_CH4
14	P0.0/SPI0_MOSI/SPI1_MOSI/UART2_TXD/UART0_RXD/TK1/PWM0_CH5
15	P5.6/TK0/PWM0_BRAKE/PWM0_CH1/CLKO
16	nRESET
17	P5.0/UART1_TXD/I2C1_SCL/UART0_TXD/ICE_DAT
18	P5.1/UART1_RXD/I2C1_SDA/UART0_RXD/ICE_CLK
19	P4.1/LCD_SEG27/LCD_COM2/UART2_TXD/I2C0_SCL/PWM3_CH0/ACMP0_O
20	P4.0/LCD_SEG26/LCD_COM3/UART2_RXD/I2C0_SDA/PWM3_CH1/ACMP1_O/INT1
21	P1.4/LCD_SEG21/I2C1_SCL/LCD_COM4
22	P1.5/LCD_SEG20/I2C1_SDA/LCD_COM5
23	P1.6/LCD_SEG19/UART0_TXD/LCD_COM6
24	P1.7/LCD_SEG18/UART0_RXD/LCD_COM7
25	VSS
26	P4.6/LCD_SEG17/PWM0_CH0/T0/CLKO/INT0
27	VDD
28	P3.3/LCD_SEG15/SPI1_SS/LCD_COM1/PWM1_CH0/IC0/PWM0_BRAKE
29	P3.2/ADC_CH7/ACMP1_N1/LCD_SEG14/SPI1_CLK/UART3_RXD/PWM1_CH1/IC1/CLKO
30	P3.1/ADC_CH6/ACMP0_P3/ACMP1_P3/LCD_SEG13/SPI1_MISO/UART3_TXD/UART0_TXD/PWM2_CH0/IC2
31	P3.0/ADC_CH10/LCD_SEG12/SPI1_MOSI/UART0_RXD/PWM2_CH1/IC0
32	V _{REF}
33	VSS

ML51TC0AE / ML51TB9AE Pin Function

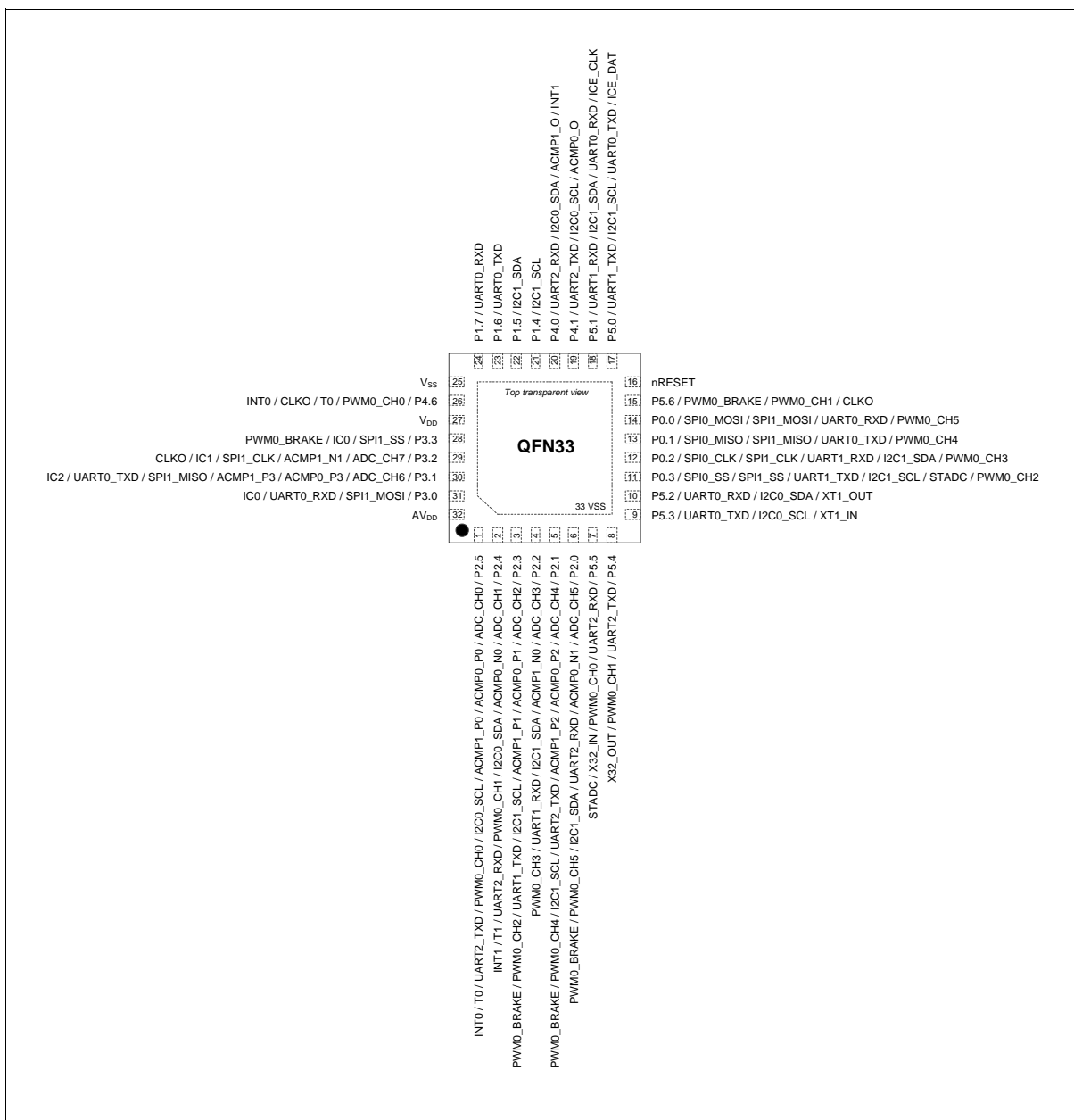


Figure 4.1-24 ML51TC0AE / ML51TB9AE Multi-Function Pin Assignment

Pin	ML51TC0AE / ML51TB9AE Pin Function
1	P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
2	P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
3	P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE
4	P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3
5	P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE

Pin	ML51TC0AE / ML51TB9AE Pin Function
6	P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE
7	P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC
8	P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT
9	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
10	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
11	P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2
12	P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
13	P0.1 / SPI0_MISO / SPI1_MISO / UART0_TXD / PWM0_CH4
14	P0.0 / SPI0_MOSI / SPI1_MOSI / UART0_RXD / PWM0_CH5
15	P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO
16	nRESET
17	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
18	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
19	P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O
20	P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1
21	P1.4 / I2C1_SCL
22	P1.5 / I2C1_SDA
23	P1.6 / UART0_TXD
24	P1.7 / UART0_RXD
25	V _{SS}
26	P4.6 / PWM0_CH0 / T0 / CLKO / INT0
27	V _{DD}
28	P3.3 / SPI1_SS / IC0 / PWM0_BRAKE
29	P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLKO
30	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2
31	P3.0 / SPI1_MOSI / UART0_RXD / IC0
32	AV _{DD}
33	VSS

4.1.2.5 LQFP32 Package

ML51PC0AE / ML51PB9AE Pin Function

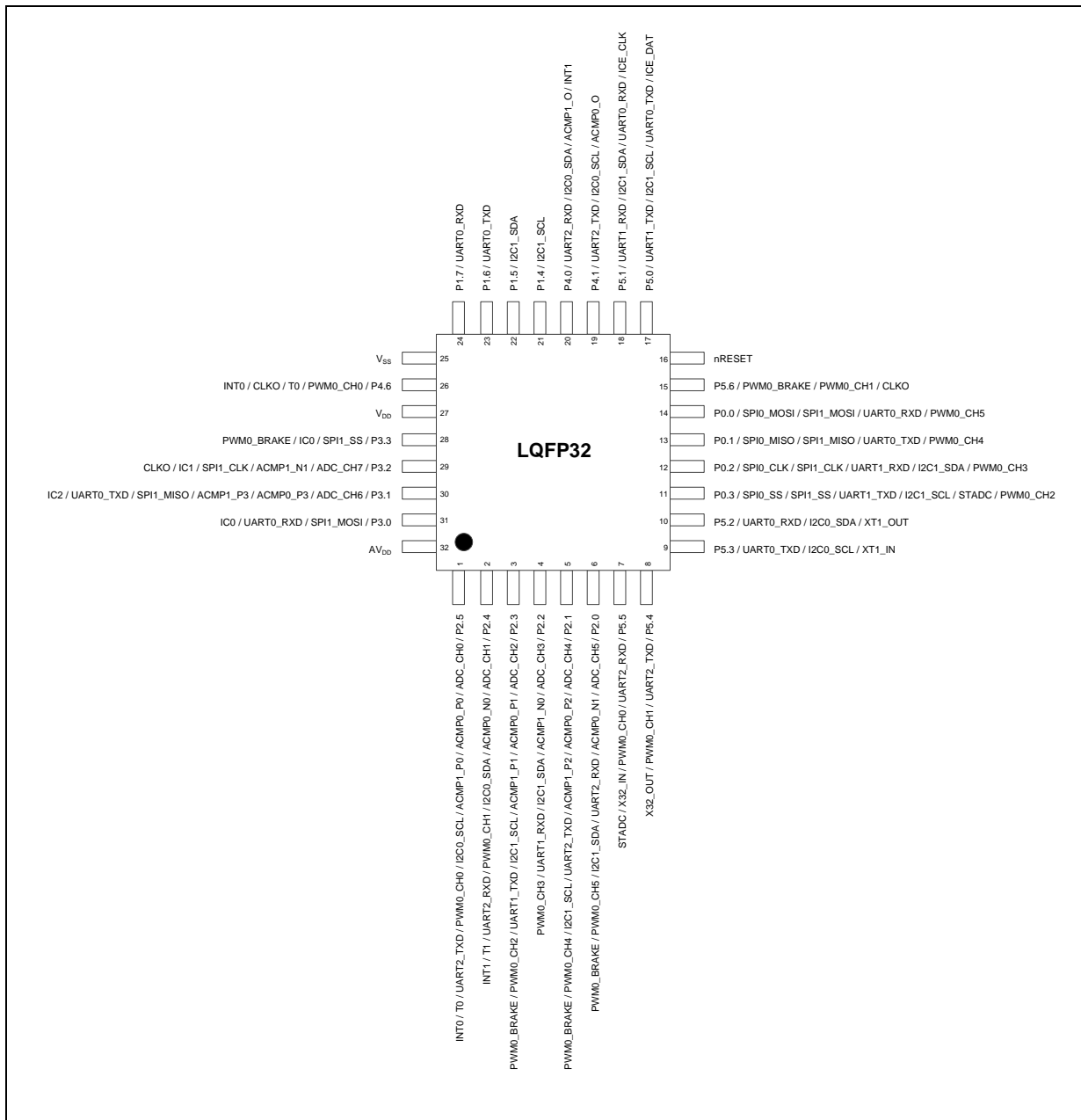


Figure 4.1-25 ML51PC0AE / ML51PB9AE Multi-Function Pin Assignment

Pin	ML51PC0AE Pin Function
1	P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
2	P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
3	P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE

Pin	ML51PC0AE Pin Function
4	P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3
5	P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE
6	P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE
7	P5.5 / UART2_RXD / PWM0_CH0 / X32_IN / STADC
8	P5.4 / UART2_TXD / PWM0_CH1 / X32_OUT
9	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
10	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
11	P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2
12	P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
13	P0.1 / SPI0_MISO / SPI1_MISO / UART0_TXD / PWM0_CH4
14	P0.0 / SPI0_MOSI / SPI1_MOSI / UART0_RXD / PWM0_CH5
15	P5.6 / PWM0_BRAKE / PWM0_CH1 / CLKO
16	nRESET
17	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
18	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
19	P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O
20	P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1
21	P1.4 / I2C1_SCL
22	P1.5 / I2C1_SDA
23	P1.6 / UART0_TXD
24	P1.7 / UART0_RXD
25	V _{SS}
26	P4.6 / PWM0_CH0 / T0 / CLKO / INT0
27	V _{DD}
28	P3.3 / SPI1_SS / IC0 / PWM0_BRAKE
29	P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLKO
30	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2
31	P3.0 / SPI1_MOSI / UART0_RXD / IC0
32	AV _{DD}

4.1.2.6 TSSOP28 Package

ML51EC0AE / ML51EB9AE Pin Function

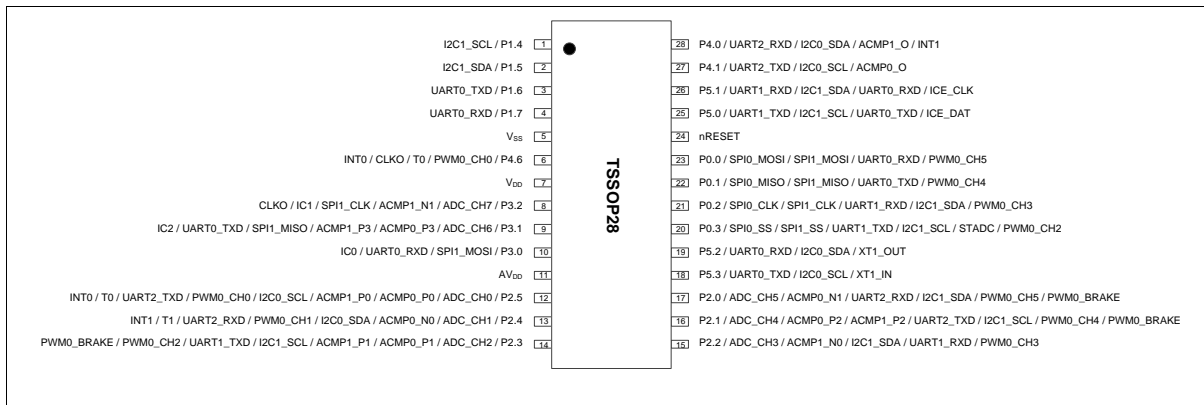


Figure 4.1-26 ML51EC0AE / ML51EB9AE Multi-Function Pin Assignment

Pin	ML51EC0AE / ML51EB9AE Pin Function
1	P1.4 / I2C1_SCL
2	P1.5 / I2C1_SDA
3	P1.6 / UART0_TXD
4	P1.7 / UART0_RXD
5	V _{SS}
6	P4.6 / PWM0_CH0 / T0 / CLK0 / INT0
7	V _{DD}
8	P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLK0
9	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2
10	P3.0 / SPI1_MOSI / UART0_RXD / IC0
11	AV _{DD}
12	P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
13	P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
14	P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE
15	P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3
16	P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE
17	P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE
18	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
19	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
20	P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2

Pin	ML51EC0AE / ML51EB9AE Pin Function
21	P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
22	P0.1 / SPI0_MISO / SPI1_MISO / UART0_TXD / PWM0_CH4
23	P0.0 / SPI0_MOSI / SPI1_MOSI / UART0_RXD / PWM0_CH5
24	nRESET
25	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
26	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
27	P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O
28	P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1

4.1.2.7 SOP28 Package

Corresponding Part Number: ML51UC0AE / ML51UB9AE

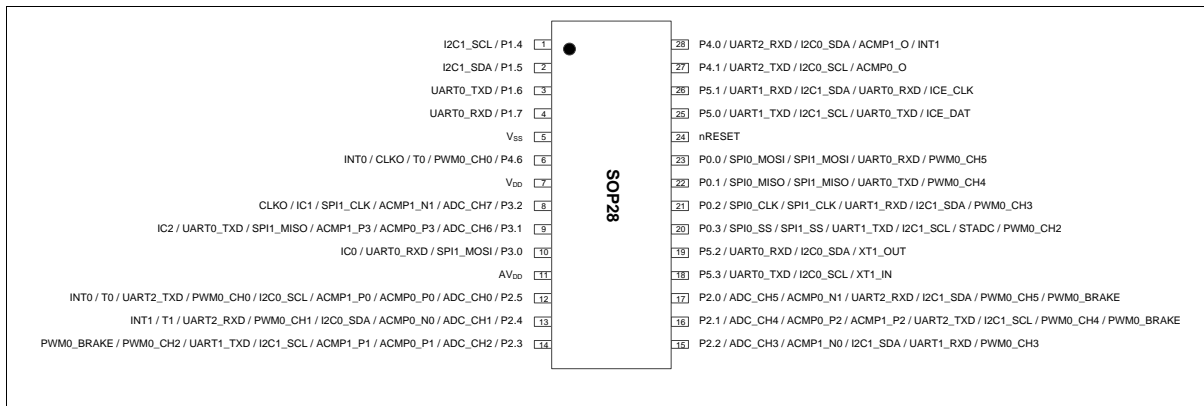


Figure 4.1-27 ML51UC0AE / ML51UB9AE Multi Function Pin Assignment

ML51UC0AE / ML51UB9AE Pin Function

Pin	ML51UC0AE / ML51UB9AE Pin Function
1	P1.4 / I2C1_SCL
2	P1.5 / I2C1_SDA
3	P1.6 / UART0_TXD
4	P1.7 / UART0_RXD
5	V _{SS}
6	P4.6 / PWM0_CH0 / T0 / CLK0 / INT0
7	V _{DD}
8	P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLK0
9	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2
10	P3.0 / SPI1_MOSI / UART0_RXD / IC0
11	AV _{DD}
12	P2.5 / ADC_CH0 / ACMP0_P0 / ACMP1_P0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
13	P2.4 / ADC_CH1 / ACMP0_N0 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
14	P2.3 / ADC_CH2 / ACMP0_P1 / ACMP1_P1 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE
15	P2.2 / ADC_CH3 / ACMP1_N0 / I2C1_SDA / UART1_RXD / PWM0_CH3
16	P2.1 / ADC_CH4 / ACMP0_P2 / ACMP1_P2 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE
17	P2.0 / ADC_CH5 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE
18	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
19	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT

Pin	ML51UC0AE / ML51UB9AE Pin Function
20	P0.3 / SPI0_SS / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2
21	P0.2 / SPI0_CLK / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
22	P0.1 / SPI0_MISO / SPI1_MISO / UART0_TXD / PWM0_CH4
23	P0.0 / SPI0_MOSI / SPI1_MOSI / UART0_RXD / PWM0_CH5
24	nRESET
25	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
26	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
27	P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O
28	P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1

4.1.2.8 TSSOP20 Package

ML51FB9AE Pin Function

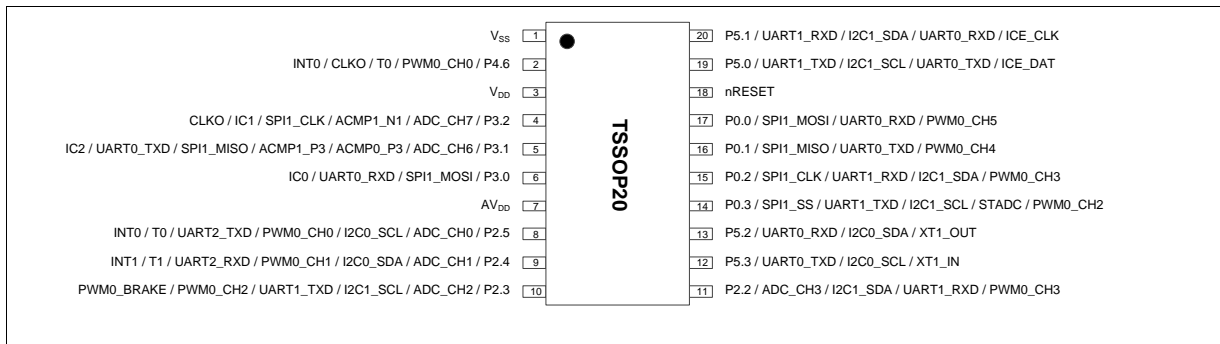


Figure 4.1-28 ML51FB9AE Multi Function Pin Assignment

Pin	ML51FB9AE Pin Function
1	V _{SS}
2	P4.6 / PWM0_CH0 / T0 / CLK0 / INT0
3	V _{DD}
4	P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLK0
5	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2
6	P3.0 / SPI1_MOSI / UART0_RXD / IC0
7	AV _{DD}
8	P2.5 / ADC_CH0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
9	P2.4 / ADC_CH1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
10	P2.3 / ADC_CH2 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE
11	P2.2 / ADC_CH3 / I2C1_SDA / UART1_RXD / PWM0_CH3
12	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
13	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
14	P0.3 / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2
15	P0.2 / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
16	P0.1 / SPI1_MISO / UART0_TXD / PWM0_CH4
17	P0.0 / SPI1_MOSI / UART0_RXD / PWM0_CH5
18	nRESET
19	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
20	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK

4.1.2.9 SOP20 Package

ML51OB9AE Pin Function

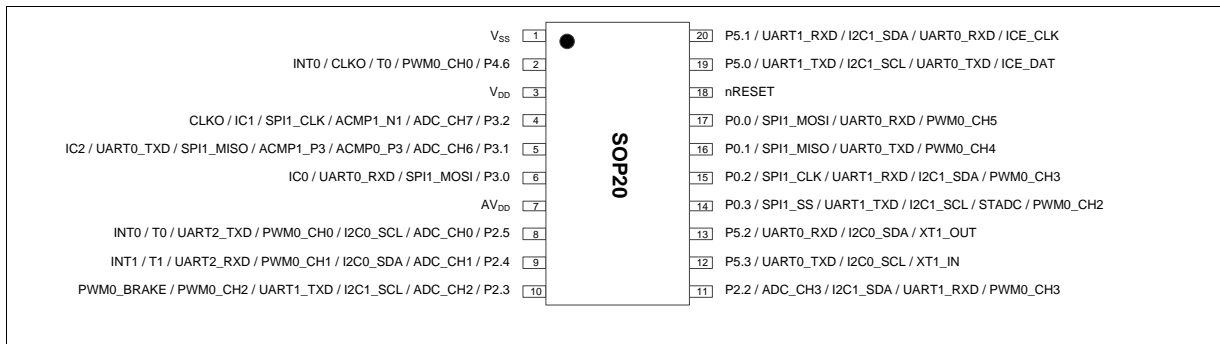


Figure 4.1-29 ML51OB9AE Multi Function Pin Assignment

Pin	ML51OB9AE Pin Function
1	V _{SS}
2	P4.6 / PWM0_CH0 / T0 / CLK0 / INT0
3	V _{DD}
4	P3.2 / ADC_CH7 / ACMP1_N1 / SPI1_CLK / IC1 / CLK0
5	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2
6	P3.0 / SPI1_MOSI / UART0_RXD / IC0
7	AV _{DD}
8	P2.5 / ADC_CH0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
9	P2.4 / ADC_CH1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
10	P2.3 / ADC_CH2 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE
11	P2.2 / ADC_CH3 / I2C1_SDA / UART1_RXD / PWM0_CH3
12	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
13	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
14	P0.3 / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2
15	P0.2 / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
16	P0.1 / SPI1_MISO / UART0_TXD / PWM0_CH4
17	P0.0 / SPI1_MOSI / UART0_RXD / PWM0_CH5
18	nRESET
19	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
20	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK

4.1.2.10 QFN20 Package

ML51XB9AE Pin Function

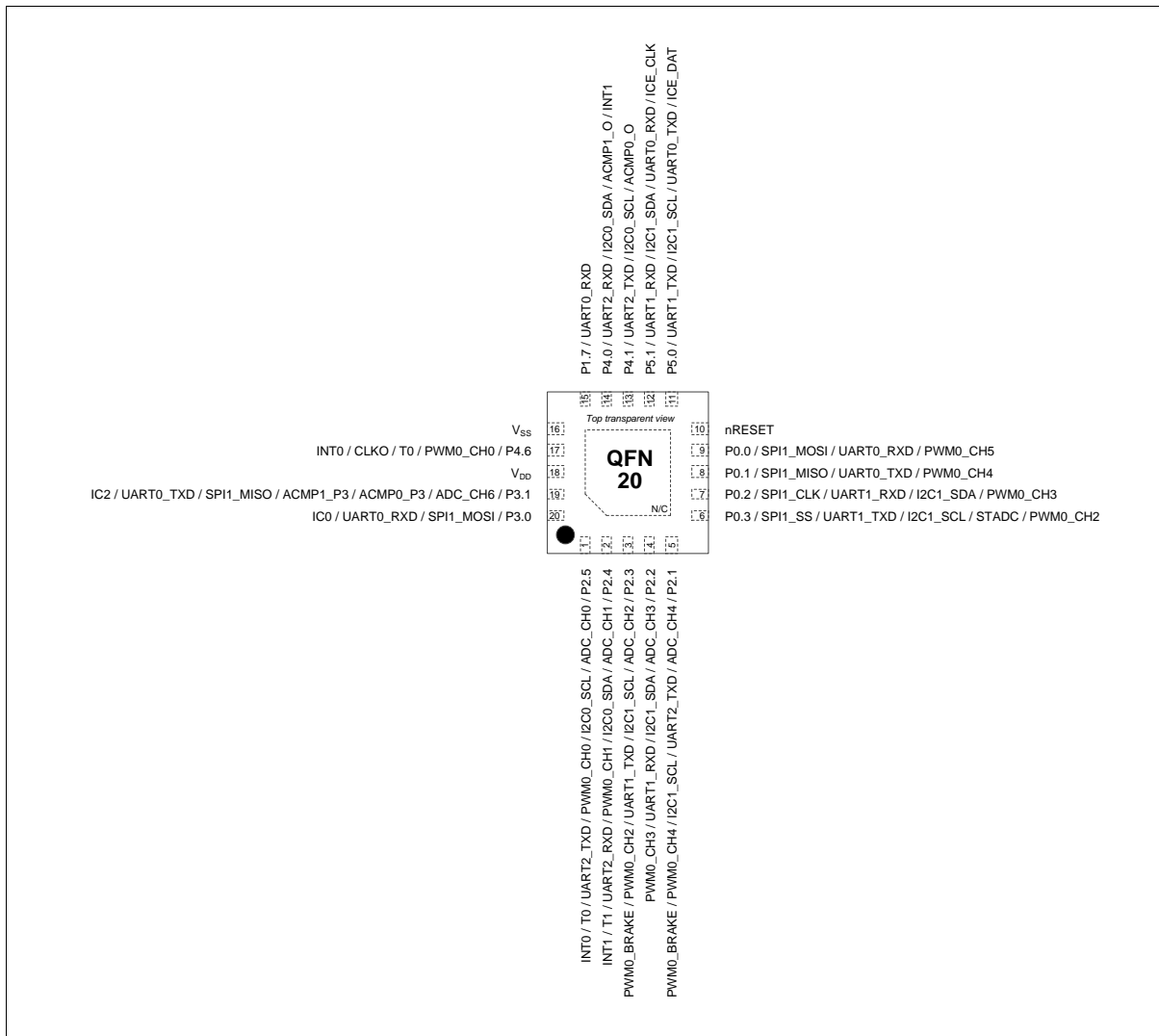


Figure 4.1-30 ML51XB9AE Multi Function Pin Assignment

Pin	ML51XB9AE Pin Function
1	P2.5 / ADC_CH0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
2	P2.4 / ADC_CH1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
3	P2.3 / ADC_CH2 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE
4	P2.2 / ADC_CH3 / I2C1_SDA / UART1_RXD / PWM0_CH3
5	P2.1 / ADC_CH4 / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE
6	P0.3 / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2
7	P0.2 / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3

Pin	ML51XB9AE Pin Function
8	P0.1 / SPI1_MISO / UART0_TXD / PWM0_CH4
9	P0.0 / SPI1_MOSI / UART0_RXD / PWM0_CH5
10	nRESET
11	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
12	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
13	P4.1 / UART2_TXD / I2C0_SCL / ACMP0_O
14	P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1
15	P1.7 / UART0_RXD
16	V _{SS}
17	P4.6 / PWM0_CH0 / T0 / CLKO / INT0
18	V _{DD}
19	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2
20	P3.0 / SPI1_MOSI / UART0_RXD / IC0

4.1.2.11 TSSOP14 Package

ML51DB9AE Pin Function

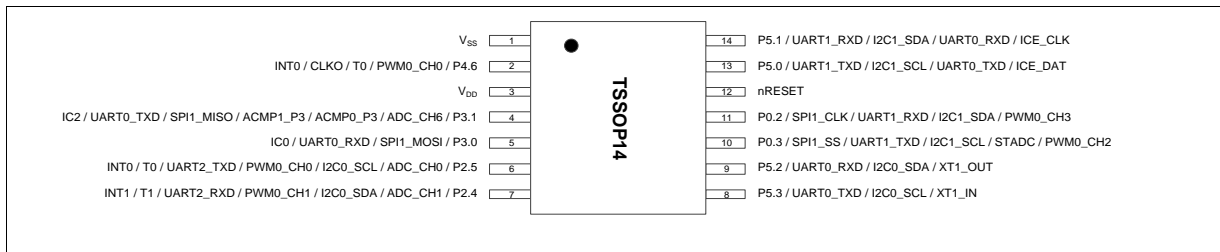


Figure 4.1-31 ML51DB9AE Multi Function Pin Assignment

Pin	ML51DB9AE Pin Function
1	V _{SS}
2	P4.6 / PWM0_CH0 / T0 / CLKO / INT0
3	V _{DD}
4	P3.1 / ADC_CH6 / ACMP0_P3 / ACMP1_P3 / SPI1_MISO / UART0_TXD / IC2
5	P3.0 / SPI1_MOSI / UART0_RXD / IC0
6	P2.5 / ADC_CH0 / I2C0_SCL / PWM0_CH0 / UART2_TXD / T0 / INT0
7	P2.4 / ADC_CH1 / I2C0_SDA / PWM0_CH1 / UART2_RXD / T1 / INT1
8	P5.3 / UART0_TXD / I2C0_SCL / XT1_IN
9	P5.2 / UART0_RXD / I2C0_SDA / XT1_OUT
10	P0.3 / SPI1_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2
11	P0.2 / SPI1_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3
12	nRESET
13	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
14	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK

4.1.2.12 MSOP10 Package

ML51BB9AE Pin Function

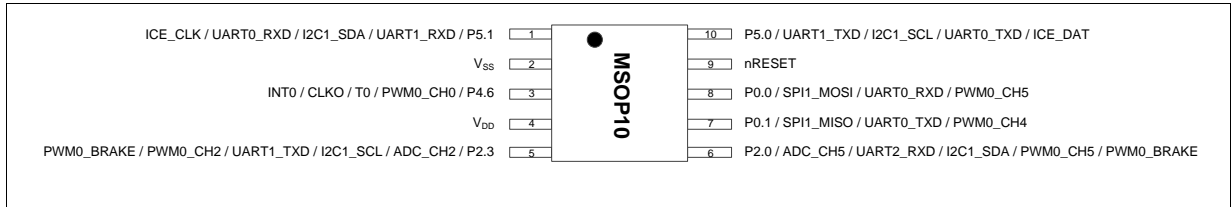


Figure 4.1-32 ML51BB9AE Pin Assignment

Pin	ML51BB9AE Pin Function
1	P5.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
2	V _{SS}
3	P4.6 / PWM0_CH0 / T0 / CLK0 / INT0
4	V _{DD}
5	P2.3 / ADC_CH2 / I2C1_SCL / UART1_TXD / PWM0_CH2 / PWM0_BRAKE
6	P2.0 / ADC_CH5 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE
7	P0.1 / SPI1_MISO / UART0_TXD / PWM0_CH4
8	P0.0 / SPI1_MOSI / UART0_RXD / PWM0_CH5
9	nRESET
10	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT

4.2 Pin Description

4.2.1 ML51/ML54/ML56 Series Pin Mapping

Pin Number	ML54/ML56			ML51							
	64	48	44	64	48	33/32	28	20	QFN20	14	10
P2.6	1	48	44	1	48						
P2.5	2	1	1	2	1	1	12	8	1	6	
P2.4	3	2	2	3	2	2	13	9	2	7	
P2.3	4	3	3	4	3	3	14	10	3		5
P2.2	5	4	4	5	4	4	15	11	4		
P2.1	6	5	5	6	5	5	16		5		
P2.0	7	6	6	7	6	6	17				6
P1.3	8	7	7	8	7						
P1.2	9	8	8	9	8						
P1.1	10	9	9	10	9						
P1.0	11			11	10						
VLCD	12	10	10								
P3.7				12							
P5.7	13			13							
P5.5	14	11	11	14	11	7					
P5.4	15	12	12	15	12	8					
P5.3	16	13	13	16	13	9	18	12		8	
P5.2	17	14	14	17	14	10	19	13		9	
P3.5	18			18							
P3.4	19			19							
P0.7	20	15	15	20	15						
P0.6	21	16	16	21	16						
VSS	22			22		33					
VDD	23			23							
P3.6	24			24							
P0.5	25	17		25	17						
P0.4	26	18		26	18						
P0.3	27	19	17	27	19	11	20	14	6	10	
P0.2	28	20	18	28	20	12	21	15	7	11	
P0.1	29	21	19	29	21	13	22	16	8		7
P0.0	30	22	20	30	22	14	23	17	9		8
P5.6	31	23		31	23	15					
nRESET	32	24	21	32	24	16	24	18	10	12	9

Pin Number	ML54/ML56			ML51							
	64	48	44	64	48	33/32	28	20	QFN20	14	10
P5.0	33	25	22	33	25	17	25	19	11	13	10
P5.1	34	26	23	34	26	18	26	20	12	14	1
P4.5	35	27	24	35	27						
P4.4	36	28	25	36	28						
P4.3	37	29	26	37	29						
P4.2	38	30	27	38	30						
P4.1	39	31	28	39	31	19	27		13		
P4.0	40	32	29	40	32	20	28		14		
P6.3	41			41							
P6.2	42			42							
P6.1	43			43							
P6.0	44			44							
P1.4	45	33	30	45	33	21	1				
P1.5	46	34	31	46	34	22	2				
P1.6	47	35	32	47	35	23	3				
P1.7	48	36	33	48	36	24	4		15		
VSS	49	37	34	49	37	25	5	1	16	1	2
P4.6	50	38	35	50	38	26	6	2	17	2	3
VDD	51	39	36	51	39	27	7	3	18	3	4
P4.7	52	40		52	40						
P3.3	53	41	37	53	41	28					
P3.2	54	42	38	54	42	29	8	4			
P3.1	55	43	39	55	43	30	9	5	19	4	
P3.0	56	44	40	56	44	31	10	6	20	5	
AVDD	57	39	36	57	39	27	7				
VREF	58	45	41	58	45	32	11	7			
AVSS	59	46	42	59	46				16		
P6.7	60			60							
P6.6	61			61							
P6.5	62			62							
P6.4	63			63							
P2.7	64	47	43	64	47						

4.2.2 ML51/ML54/ML56 Series Pin Function Description

As default all GPIO type is defined as input mode. User should setting the GPIO Mode by PxMx register.

A: Analog suggest disable digial function O: output, I: input, I/O: bi-direction (Quasi)

Group	Pin Name	Type	Description
ACMP0	ACMP0_N0	A	Analog comparator 0 negative input 0 pin.
	ACMP0_N1		Analog comparator 0 negative input 1 pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1		Analog comparator 0 positive input 1 pin.
	ACMP0_P2		Analog comparator 0 positive input 2 pin.
	ACMP0_P3		Analog comparator 0 positive input 3 pin.
ACMP1	ACMP1_N0	A	Analog comparator 1 negative input 0 pin.
	ACMP1_N1		Analog comparator 1 negative input 1 pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1		Analog comparator 1 positive input 1 pin.
	ACMP1_P2		Analog comparator 1 positive input 2 pin.
	ACMP1_P3		Analog comparator 1 positive input 3 pin.
ADC	ADC_CH0	A	ADC_ channel analog input.
	ADC_CH1		ADC_ channel analog input.
	ADC_CH2		ADC_ channel analog input.
	ADC_CH3		ADC_ channel analog input.
	ADC_CH4		ADC_ channel analog input.
	ADC_CH5		ADC_ channel analog input.
	ADC_CH6		ADC_ channel analog input.
	ADC_CH7		ADC_ channel analog input.
	ADC_CH10		ADC_ channel analog input.
	ADC_CH11		ADC_ channel analog input.
	ADC_CH12		ADC_ channel analog input.
	ADC_CH13		ADC_ channel analog input.
	ADC_CH14		ADC_ channel analog input.
	ADC_CH15		ADC_ channel analog input.
	CLKO		CLKO
I2C0	I2C0_SCL	I/O	I2C0 clock pin.

Group	Pin Name	Type	Description
	I2C0_SDA	I/O	I2C0 data input/output pin.
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
IC0	IC0	I/O	Input Capture channel 0
IC1	IC1	I/O	Input Capture channel 1
IC2	IC2	I/O	Input Capture channel 2
ICE	ICE_CLK	I	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin
	ICE_DAT	O	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
LCD	LCD_COM0	O	LCD Common 0 output.
	LCD_COM1	O	LCD Common 1 output.
	LCD_COM2	O	LCD Common 2 output.
	LCD_COM3	O	LCD Common 3 output.
	LCD_COM4	O	LCD Common 4 output.
	LCD_COM5	O	LCD Common 5 output.
	LCD_COM6	O	LCD Common 6 output.
	LCD_COM7	O	LCD Common 7 output.
	LCD_DH1	O	LCD external capacitor pin of charge pump circuit.
	LCD_DH2	O	LCD external capacitor pin of charge pump circuit.
	LCD_SEG0	O	LCD segment 0 output
	LCD_SEG1	O	LCD segment 1 output
	LCD_SEG2	O	LCD segment 2 output
	LCD_SEG3	O	LCD segment 3 output
	LCD_SEG4	O	LCD segment 4 output
	LCD_SEG5	O	LCD segment 5 output
	LCD_SEG6	O	LCD segment 6 output
	LCD_SEG7	O	LCD segment 7 output
LCD_SEG8	O	LCD segment 8 output	
LCD_SEG9	O	LCD segment 9 output	
LCD_SEG10	O	LCD segment 10 output	
LCD_SEG11	O	LCD segment 11 output	

Group	Pin Name	Type	Description
	LCD_SEG12	O	LCD segment 12 output
	LCD_SEG13	O	LCD segment 13 output
	LCD_SEG14	O	LCD segment 14 output
	LCD_SEG15	O	LCD segment 15 output
	LCD_SEG16	O	LCD segment 16 output
	LCD_SEG17	O	LCD segment 17 output
	LCD_SEG18	O	LCD segment 18 output
	LCD_SEG19	O	LCD segment 19 output
	LCD_SEG20	O	LCD segment 20 output
	LCD_SEG21	O	LCD segment 21 output
	LCD_SEG22	O	LCD segment 22 output
	LCD_SEG23	O	LCD segment 23 output
	LCD_SEG24	O	LCD segment 24 output
	LCD_SEG25	O	LCD segment 25 output
	LCD_SEG26	O	LCD segment 26 output
	LCD_SEG27	O	LCD segment 27 output
	LCD_SEG28	O	LCD segment 28 output
	LCD_SEG29	O	LCD segment 29 output
	LCD_SEG30	O	LCD segment 30 output
	LCD_SEG31	O	LCD segment 31 output
	LCD_V1	I	Input pin of the 1 st most positive LCD level.
	LCD_V2	I	Input pin of the 2 nd most positive LCD level.
	LCD_V3	I	Input pin of the 3 rd most positive LCD level.
nRESET	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. Note: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
PWM0	PWM0_BRAKE	I	PWM0 Brake input pin.
	PWM0_CH0	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH1	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH2	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH3	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH4	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	I/O	PWM0 channel 5 output/capture input.
PWM1	PWM1_CH0	I/O	PWM1 channel 0 output/capture input.
	PWM1_CH1	I/O	PWM1 channel 1 output/capture input.

Group	Pin Name	Type	Description
PWM2	PWM2_CH0	I/O	PWM2 channel 0 output/capture input.
	PWM2_CH1	I/O	PWM2 channel 1 output/capture input.
PWM3	PWM3_CH0	I/O	PWM3 channel 0 output/capture input.
	PWM3_CH1	I/O	PWM3 channel 1 output/capture input.
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
SPI1	SPI1_CLK	I/O	SPI1 serial clock pin.
	SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_SS	I/O	SPI1 slave select pin.
STADC	STADC	I	ADC external trigger input.
T0	T0	I/O	External count input to Timer/Counter 0 or its toggle output.
T1	T1	I/O	External count input to Timer/Counter 1 or its toggle output.
TK	TK0	A	Touch Key 0.
	TK1	A	Touch Key 1.
	TK2	A	Touch Key 2.
	TK3	A	Touch Key 3.
	TK4	A	Touch Key 4.
	TK5	A	Touch Key 5.
	TK6	A	Touch Key 6.
	TK7	A	Touch Key 7.
	TK8	A	Touch Key 8.
	TK9	A	Touch Key 9.
	TK10	A	Touch Key 10.
	TK11	A	Touch Key 11.
	TK12	A	Touch Key 12.
	TK13	A	Touch Key 13.
TK14	A	Touch Key 14.	
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.

Group	Pin Name	Type	Description
	UART2_TXD	O	UART2 data transmitter output pin.
UART3	UART3_RXD	I	UART3 data receiver input pin.
	UART3_TXD	O	UART3 data transmitter output pin.
V _{REF}	VREF	A	ADC reference voltage input. Note: This pin needs to be connected with a 1uF capacitor when use internal voltage reference output.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.

5 BLOCK DIAGRAM

5.1 ML51 Series Full Function Block

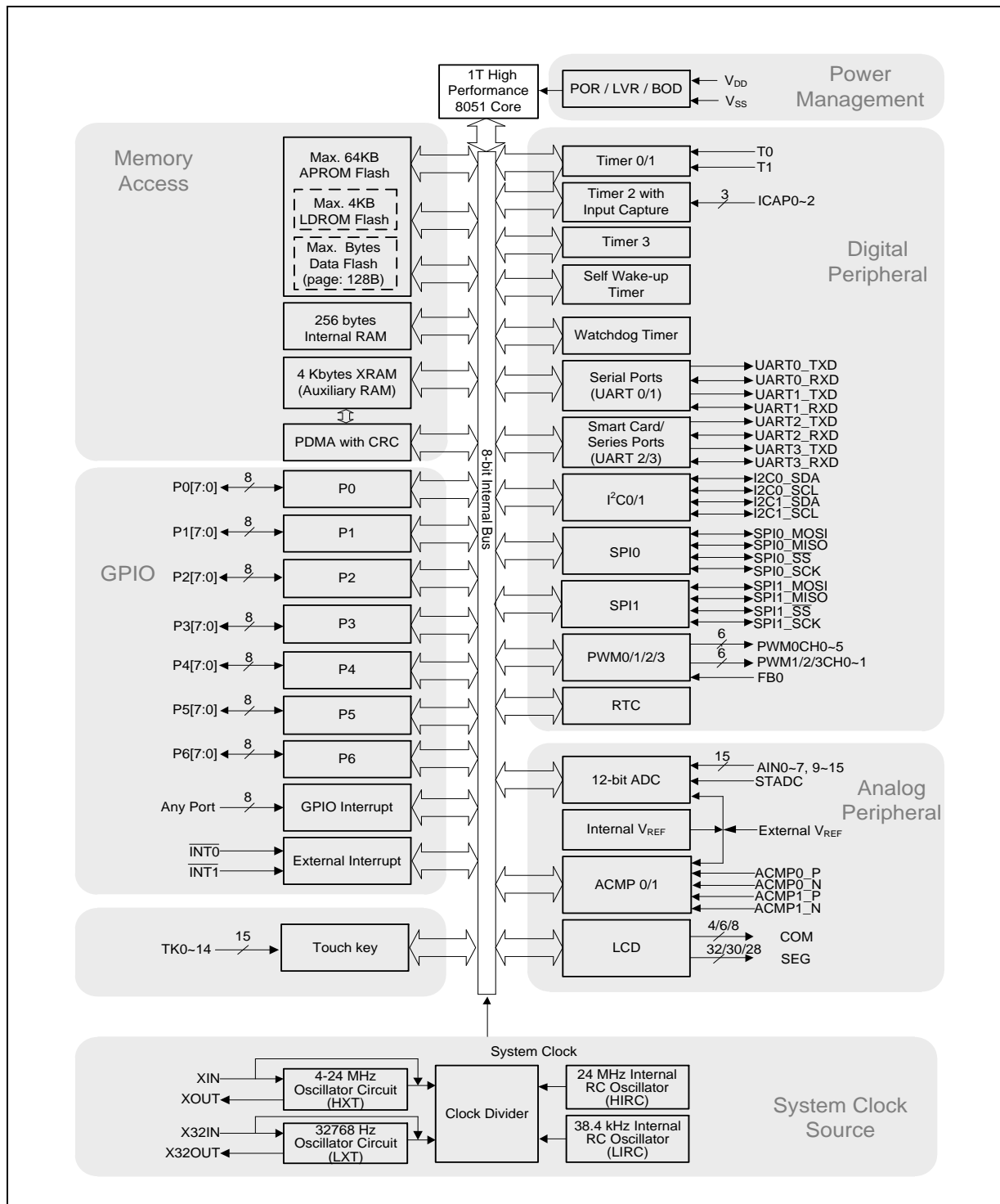


Figure 5.1-1 Functional Block Diagram

6 UTILITIES

6.1 Programmer and Debugger

Nu-Link	Basic full speed USB2.0 hardware debugger/programmer
Nu-Link-Pro	Advance hardware debugger/programmer with programming counter
Nu-Link 2.0	Advance high speed USB2.0 hardware debugger/programmer with multi-functions
Nu-Link-Gang	Off-line hardware programmer supports up to four chips programming for mass-production
ISP	In system programming, a software programming tool support UART/USB
ICP	In Chip Programming, a software programming tool support Nu-Link programmer

6.2 Development Environment

Programming IDE	Keil C51, IAR EWR 8051
Software Package	Board Support Package(BSP), Sample Code,
Development IDE	NuTool-Pin Config

6.3 Development Board

EVB NuMaker	Part Number
NK-ML51SD	ML51TD1AE
	ML51LD1AE
	ML51SD1AE
NK-ML56SD	ML54MD1AE
	ML54LD1AE
	ML54SD1AE
	ML56MD1AE
	ML56LD1AE
	ML56SD1AE

7 PACKAGE DIMENSIONS

7.1 LQFP 64L (7x7x1.4 mm Footprint 2.0 mm)

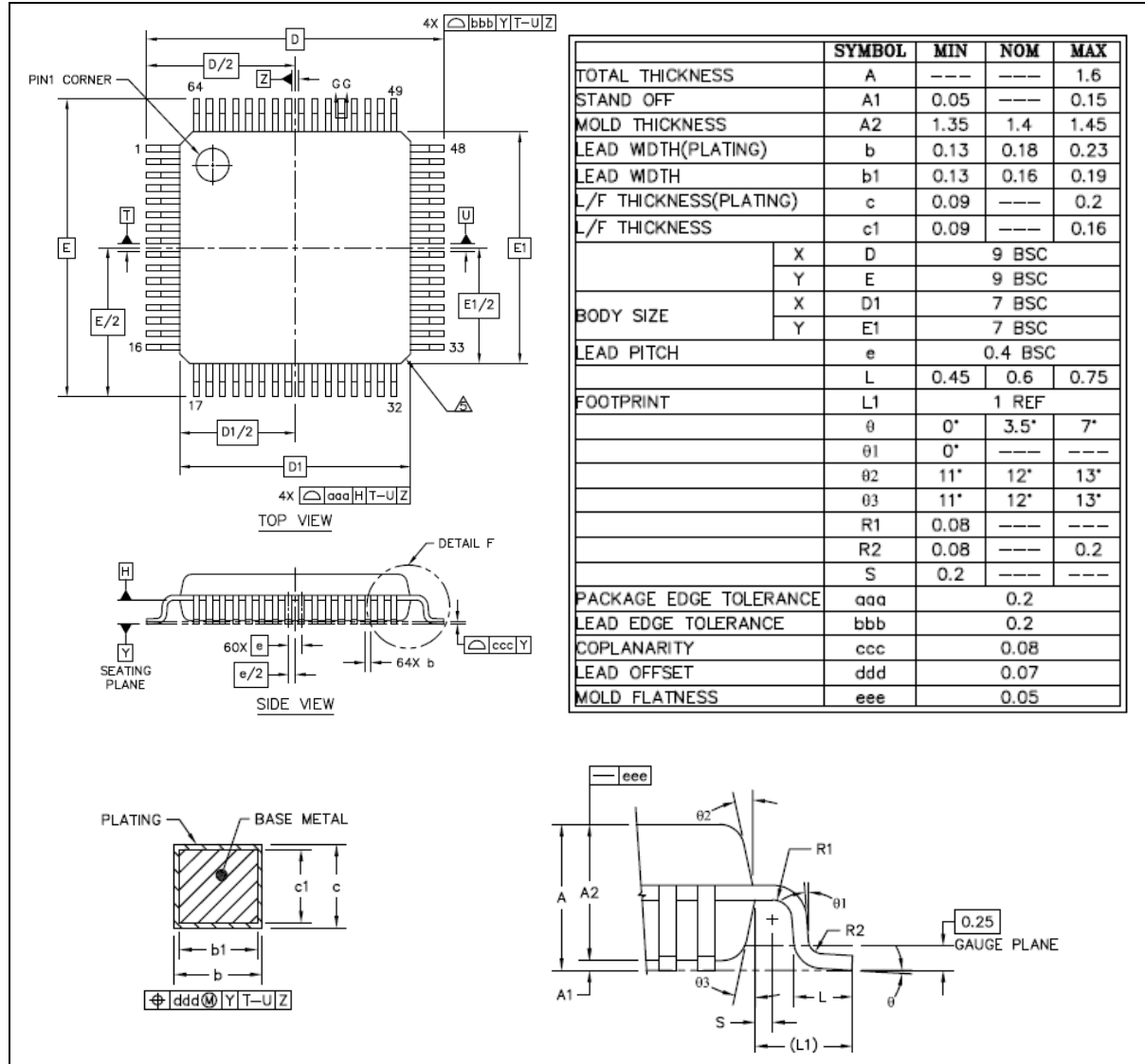


Figure 7.1-1 LQFP 64L Package Dimension

7.2 LQFP 48-pin (7x7x1.4 mm Footprint 2.0mm)

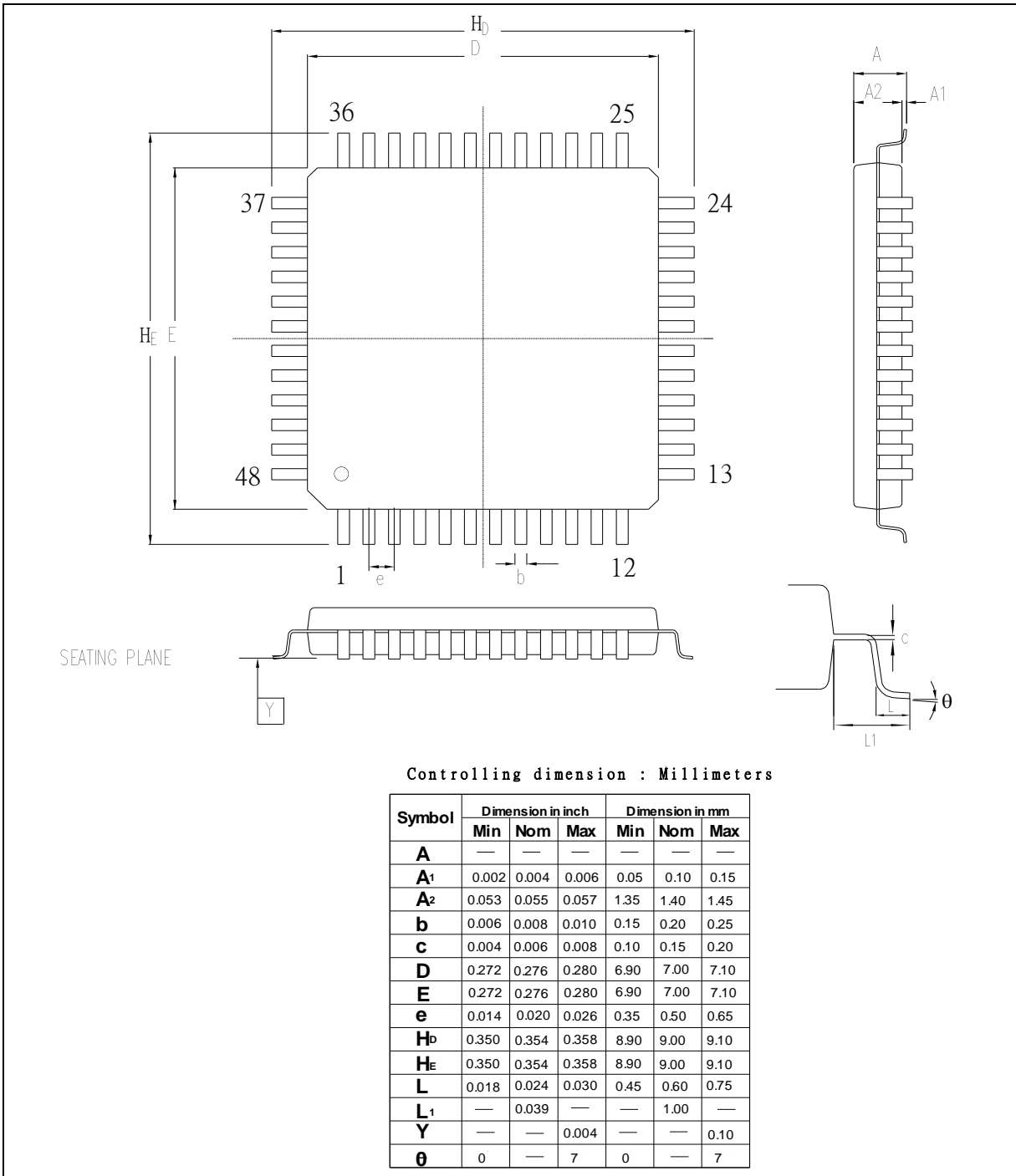


Figure 7.2-1 LQFP48 Package Dimension

7.3 LQFP 44-pin (10x10x1.4mm)

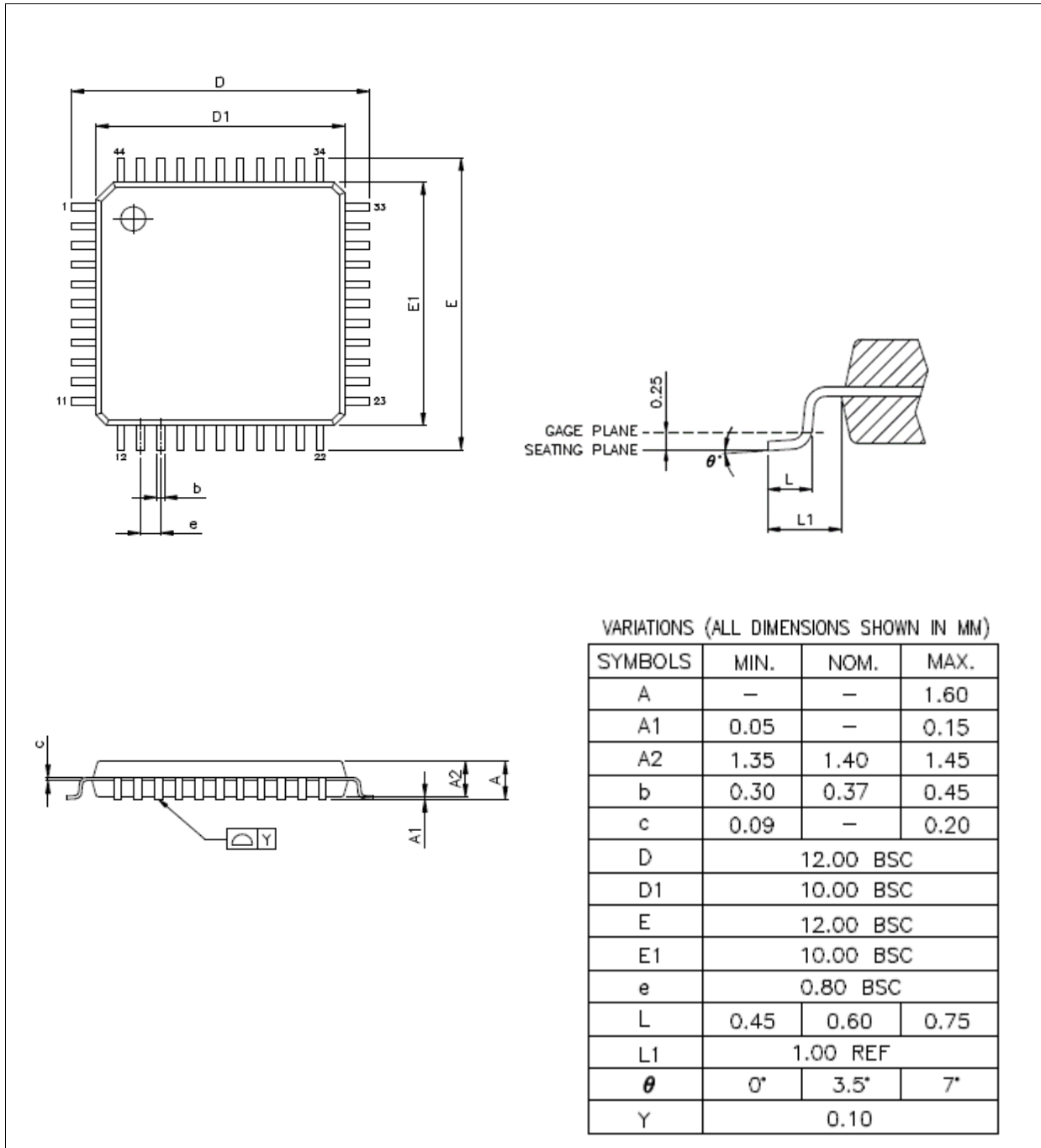


Figure 7.3-1 LFP44 Package Dimension

7.4 QFN 32-pin (4.0 x 4.0 x 0.8 mm)

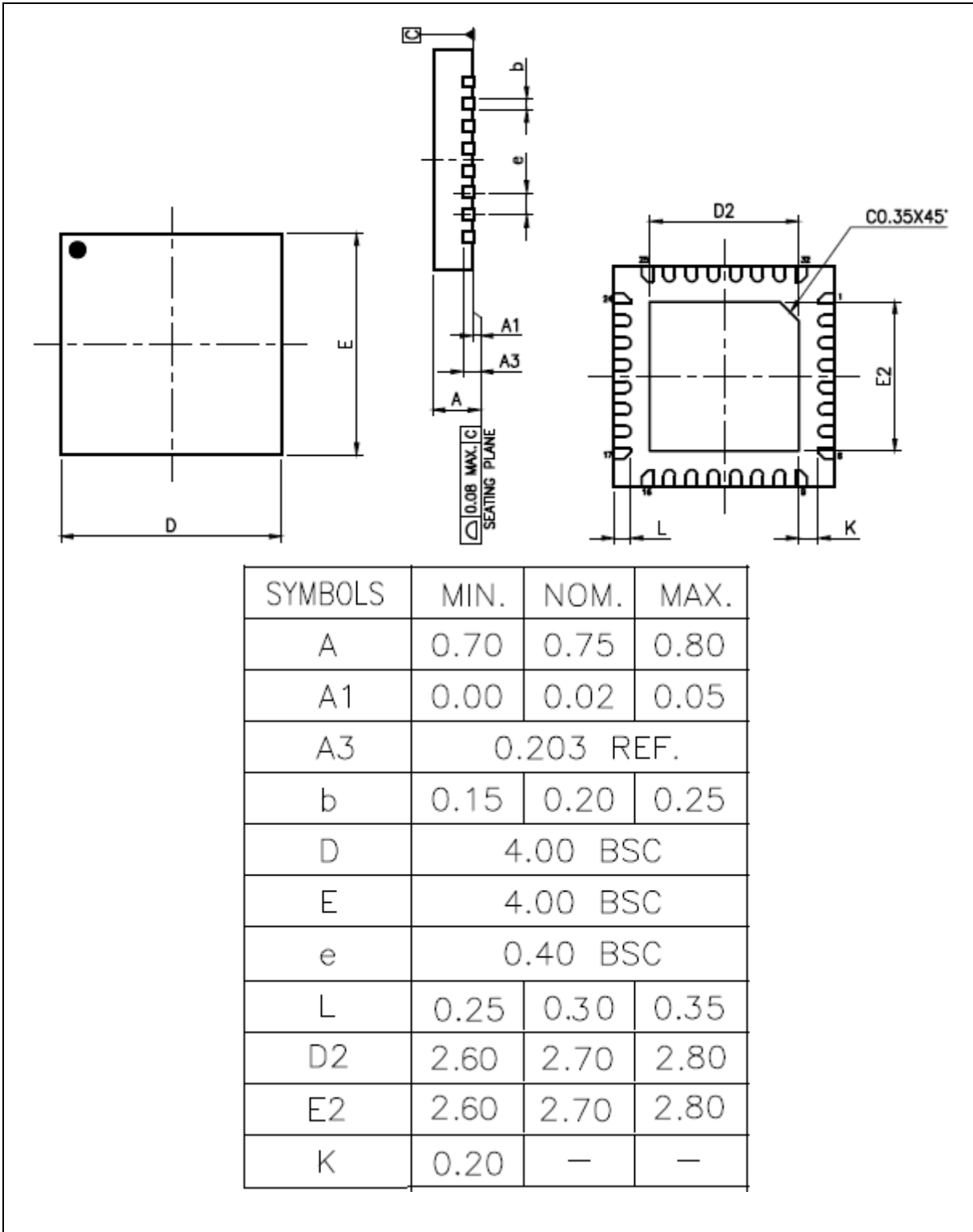


Figure 7.4-1 QFN-32 Package Dimension

7.5 LQFP 32-pin (7.0 x 7.0 x 1.4 mm)

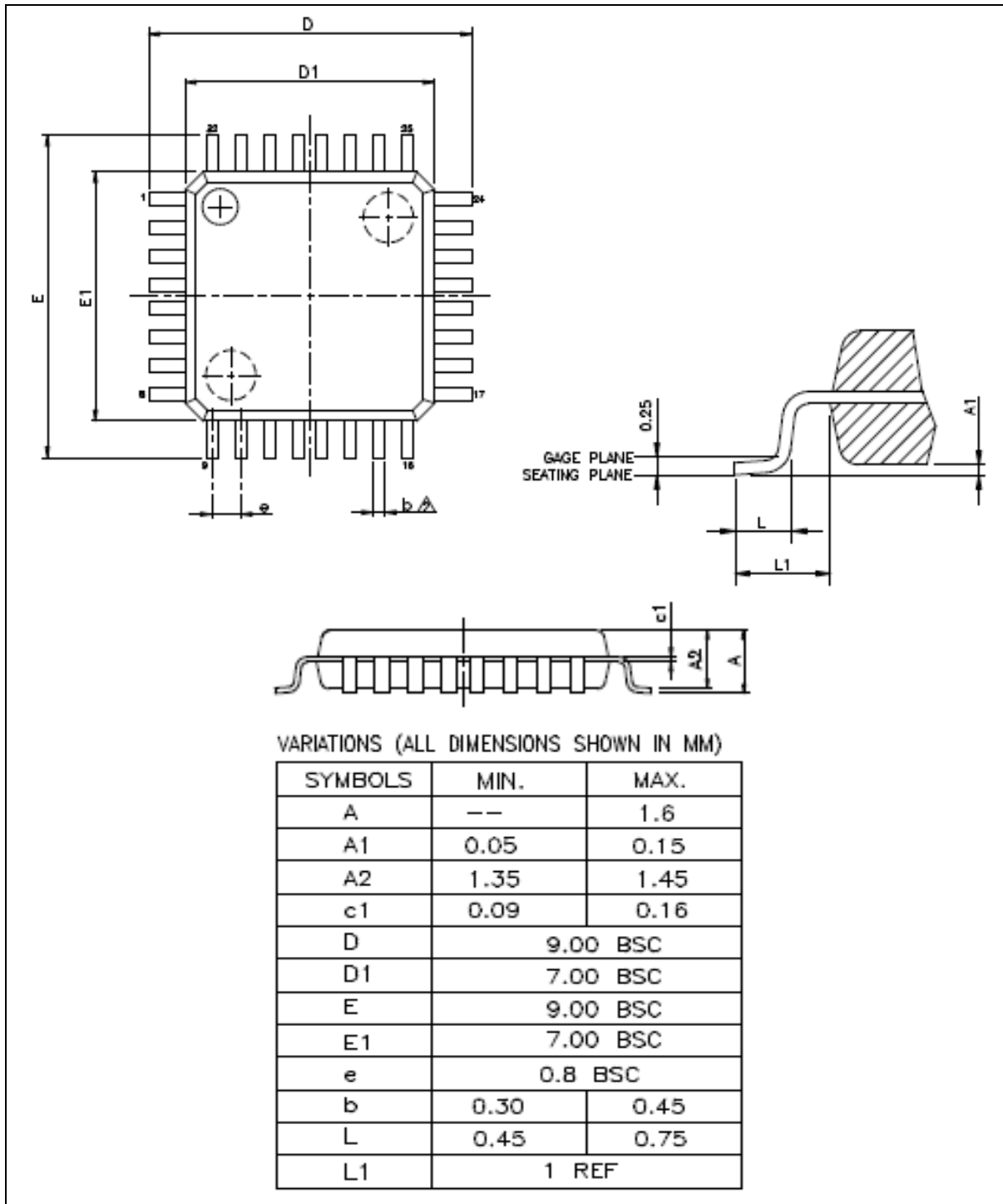


Figure 7.5-1 LQFP-32 Package Dimension

7.6 TSSOP 28-pin (4.4 x 9.7 x 1.0 mm)

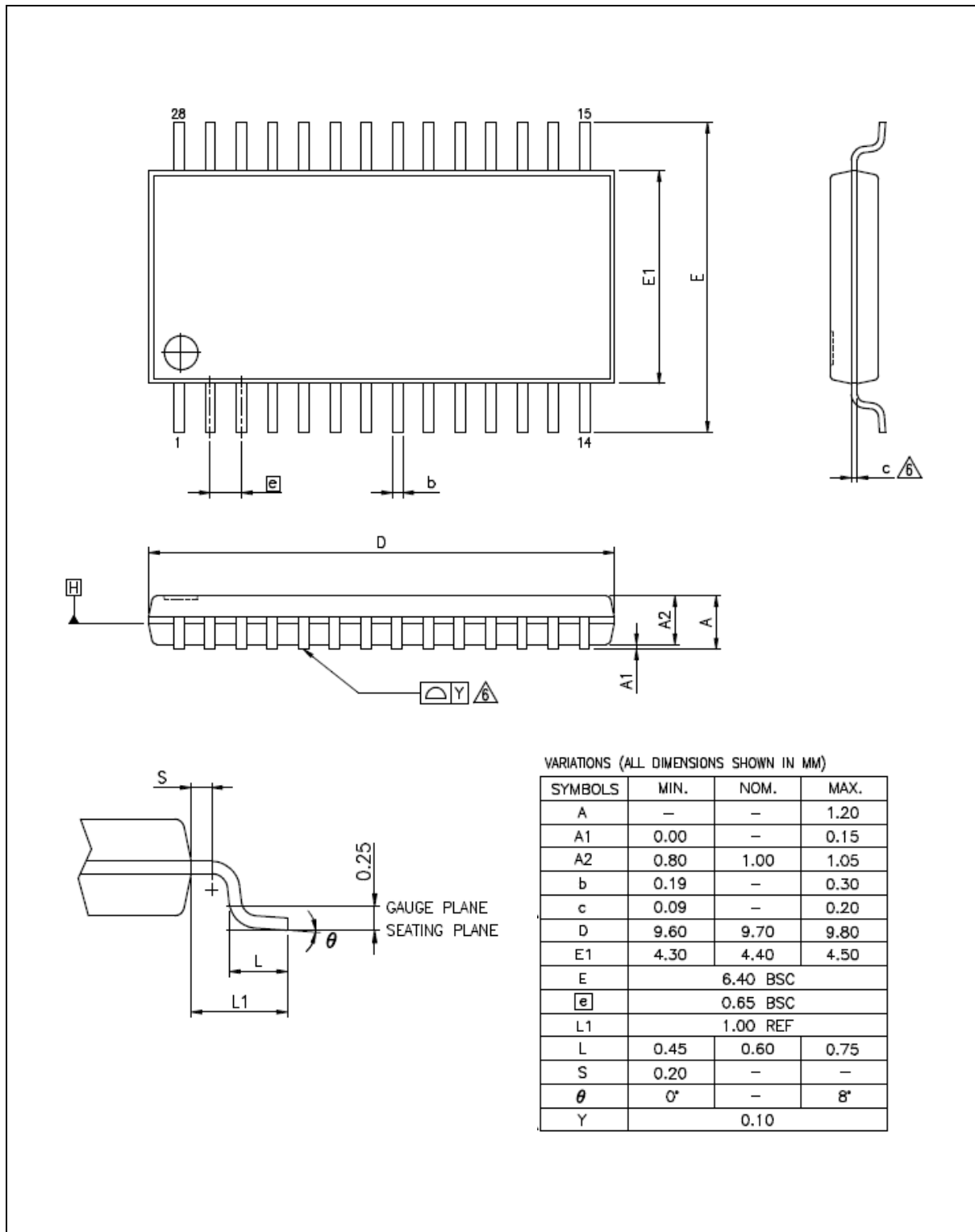


Figure 7.6-1 TSSOP-28 Package Dimension

7.7 SOP 28-pin (300mil)

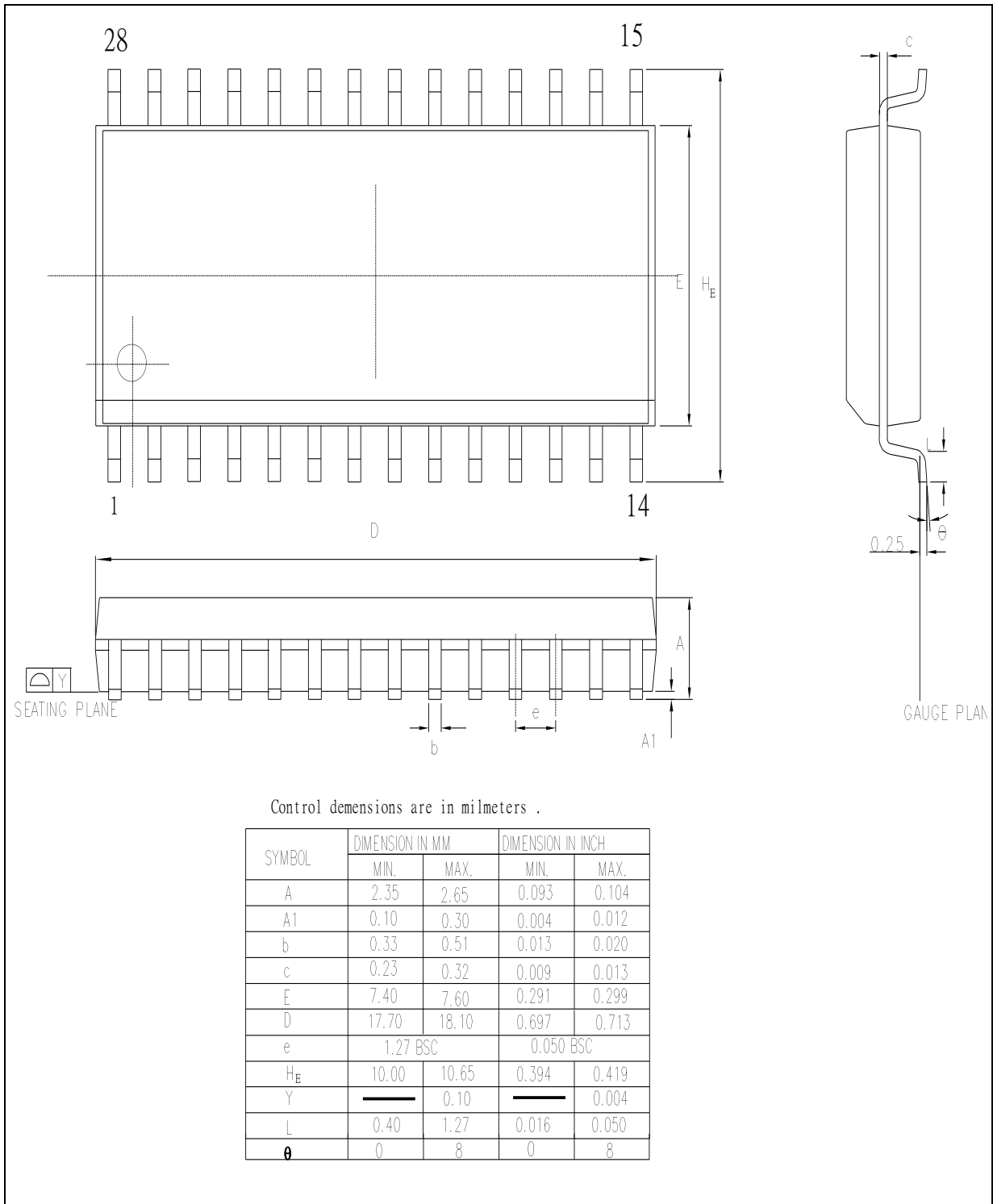


Figure 7.7-1 SOP-28 Package Dimension

7.8 TSSOP 20-pin (4.4 x 6.5 x 0.9 mm)

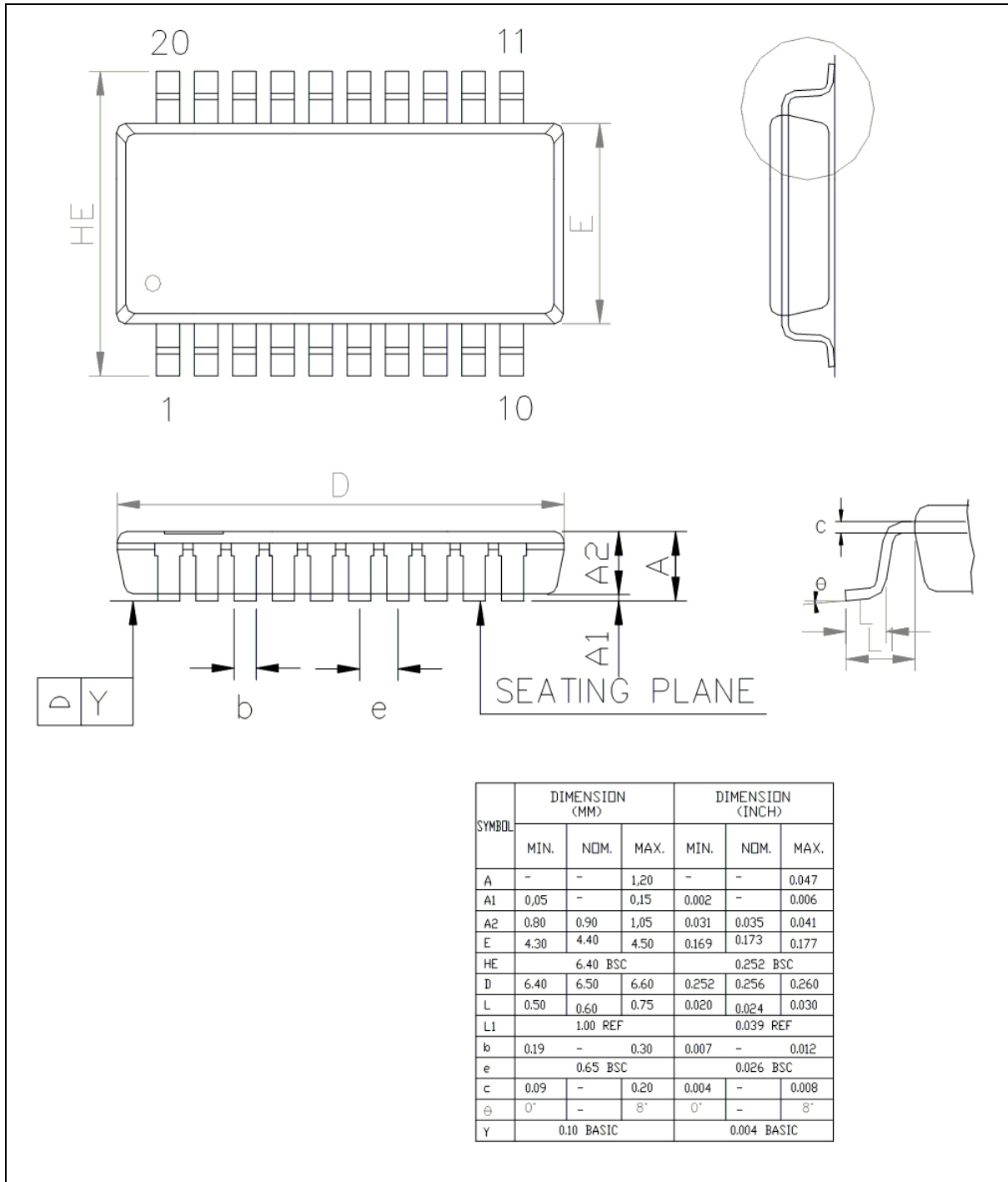


Figure 7.8-1 TSSOP-20 Package Dimension

7.9 SOP 20-pin (300 mil)

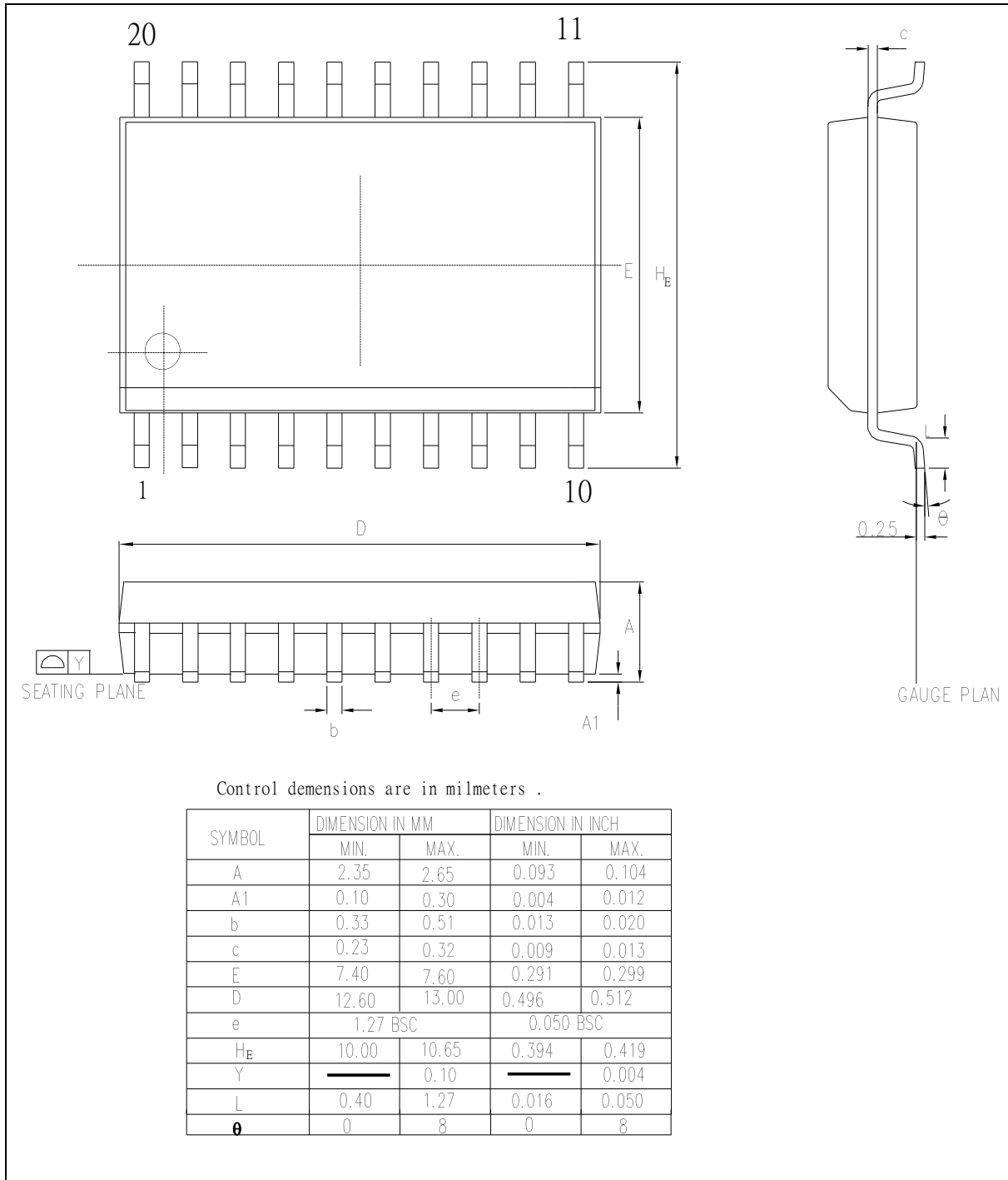


Figure 7.9-1 SOP-20 Package Dimension

7.10 QFN 20-pin (3.0 x 3.0 x 0.8 mm)

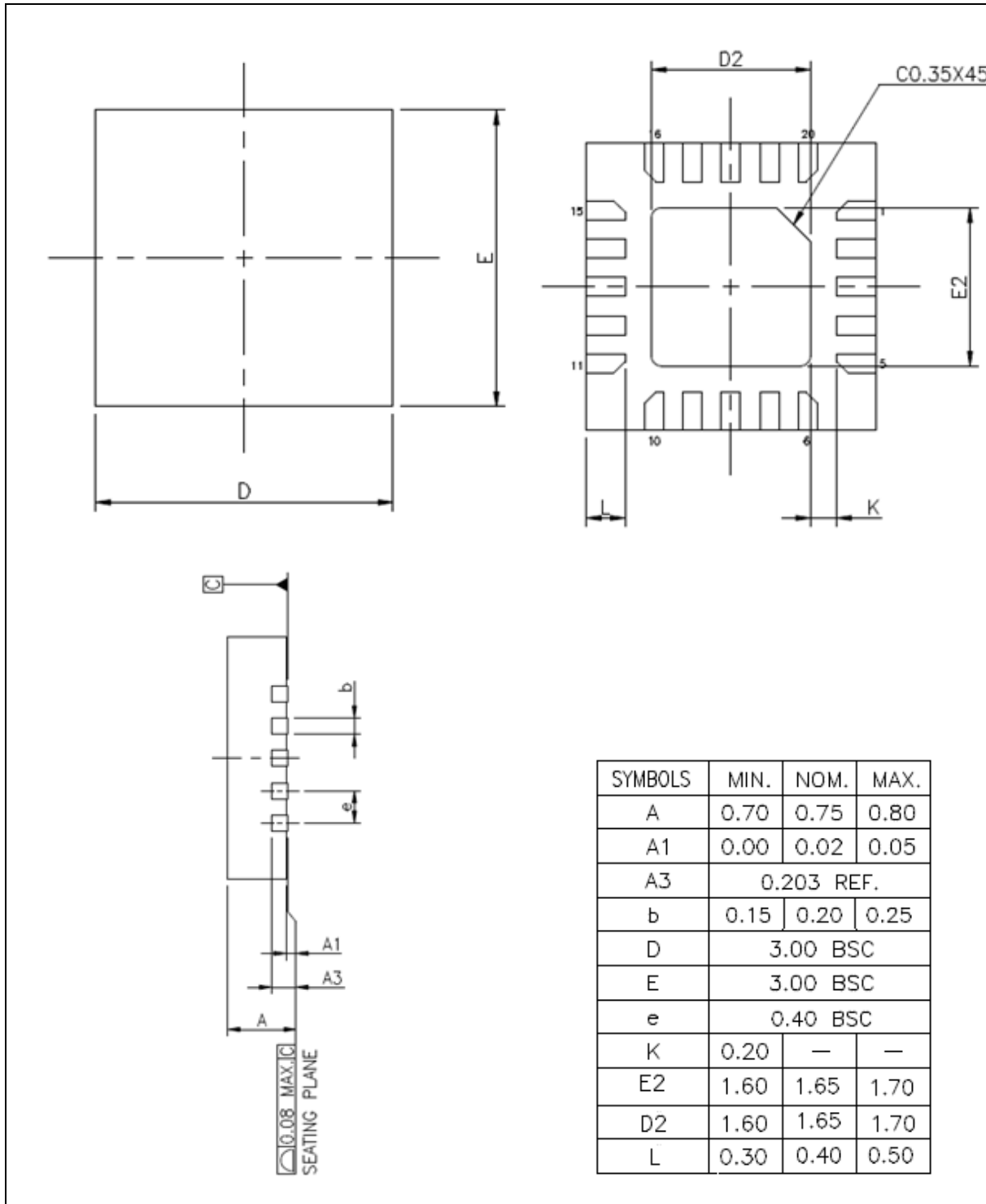


Figure 7.10-1 QFN-20 Package Dimension

7.11 TSSOP 14-pin (4.4 x 5.0 x 0.9 mm)

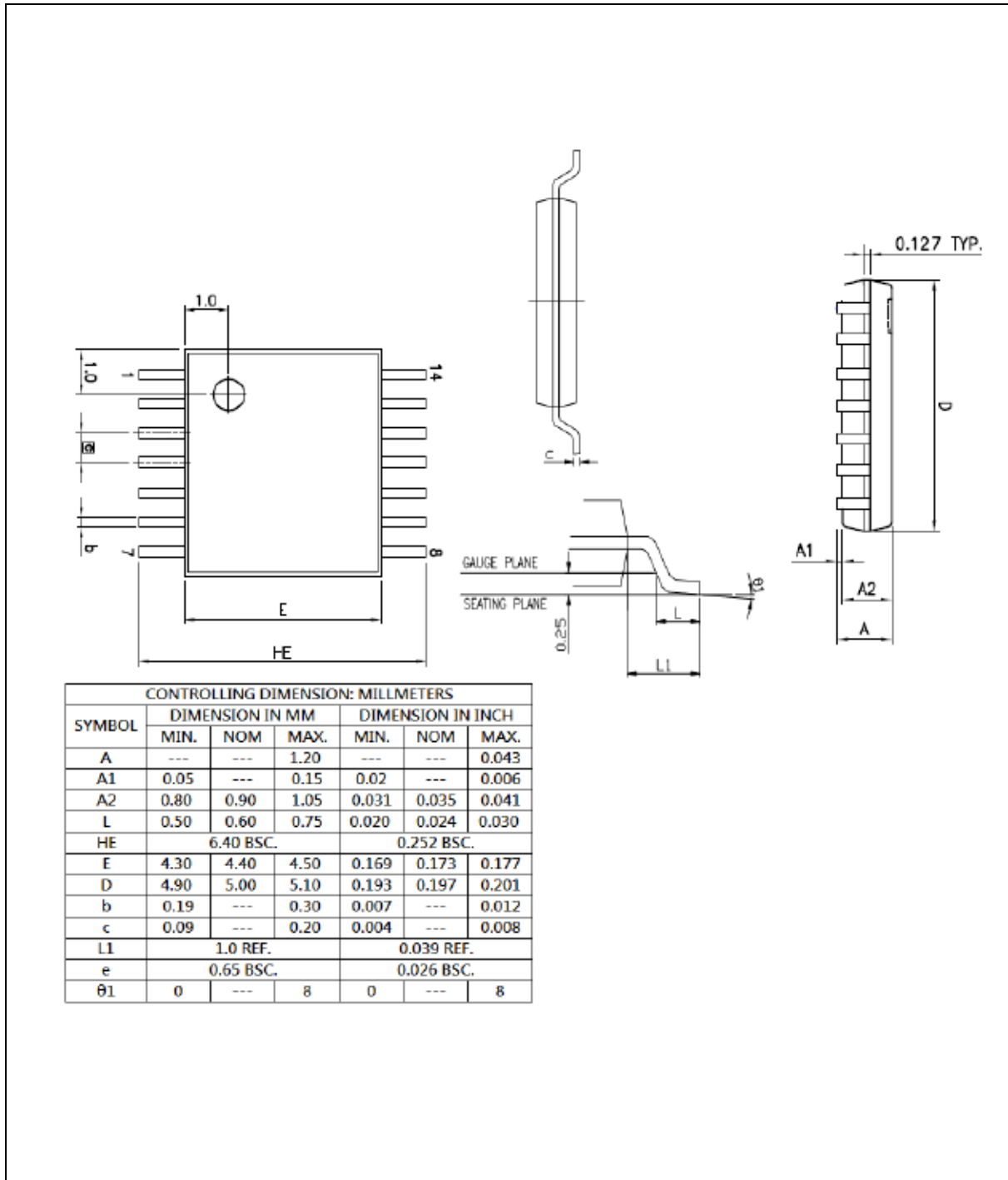


Figure 7.11-1 TSSOP-14 Package Dimension

7.12 MSOP 10-pin (3.0 x 3.0 x 0.85 mm)

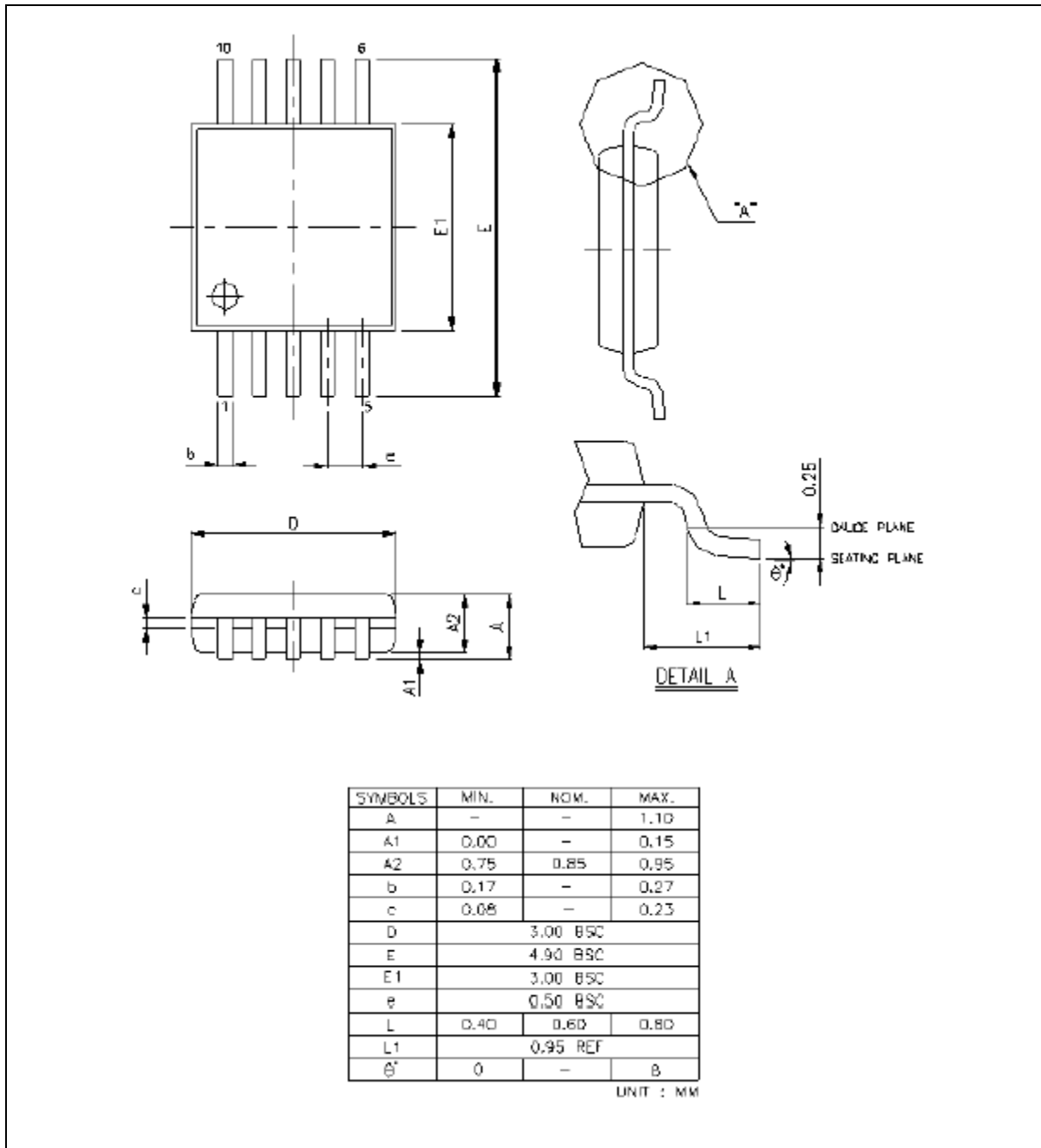


Figure 7.12 -1 MSOP-10 Package Dimension

8 REVISION HISTORY

Date	Revision	Description
2020.04.30	1.00	Initial release.

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

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