

P-channel 40 V, 0.0125 Ω typ., StripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

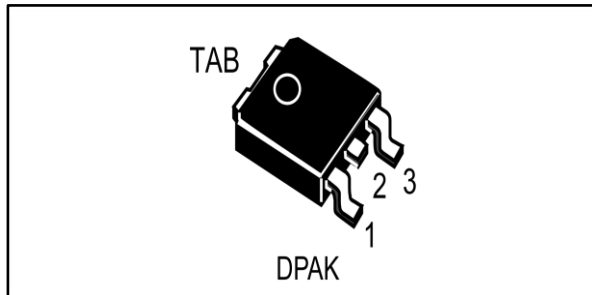
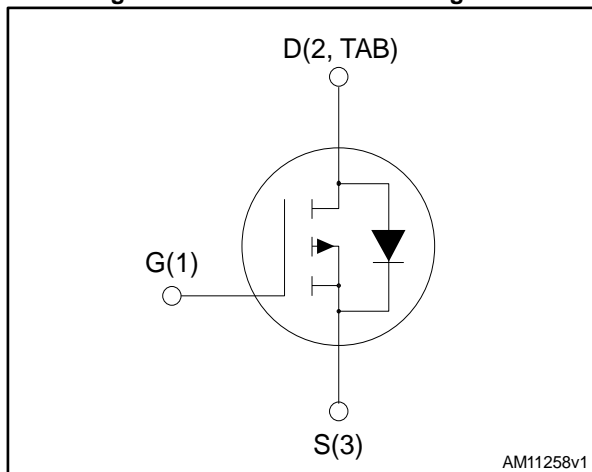


Figure 1: Internal schematic diagram



- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications


- Switching applications

Description

This device is a P-channel Power MOSFET developed using the StripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order codes	Marking	Package	Packaging
STD46P4LLF6	46P4LLF6	DPAK	Tape and reel

 For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max.	I_D
STD46P4LLF6	40 V	0.015 Ω	46 A

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	46	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	32.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	184	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature	175	$^\circ\text{C}$

Notes:

⁽¹⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	2.14	$^\circ\text{C/W}$



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown Voltage	I _D = 250 μA, V _{GS} = 0	40			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 40 V, (V _{GS} = 0)			1	μA
		V _{DS} = 40 V, T _c = 125 °C			10	μA
I _{GSS}	Gate body leakage current	V _{GS} = ± 20 V, (V _{DS} = 0)			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1		2.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 23 A		0.0125	0.015	Ω
		V _{GS} = 4.5 V, I _D = 23 A		0.017	0.02	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f=1 MHz, V _{GS} = 0	-	3525	-	pF
C _{oss}	Output capacitance		-	344	-	pF
C _{rss}	Reverse transfer capacitance		-	238.5	-	pF
Q _g	Total gate charge	V _{DD} = 20 V, I _D = 46 A V _{GS} = 4.5 V	-	34	-	nC
Q _{gs}	Gate-source charge		-	11.3	-	nC
Q _{gd}	Gate-drain charge		-	13.8	-	nC



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 6: Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 23\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$	-	49.4	-	ns
t_r	Rise time		-	60.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	170	-	ns
t_f	Fall time		-	20	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 23\text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 46\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 24\text{ V}$	-	29		ns
Q_{rr}	Reverse recovery charge		-	27.6		nC
I_{RRM}	Reverse recovery current		-	1.9		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

3 Electrical characteristics (curves)

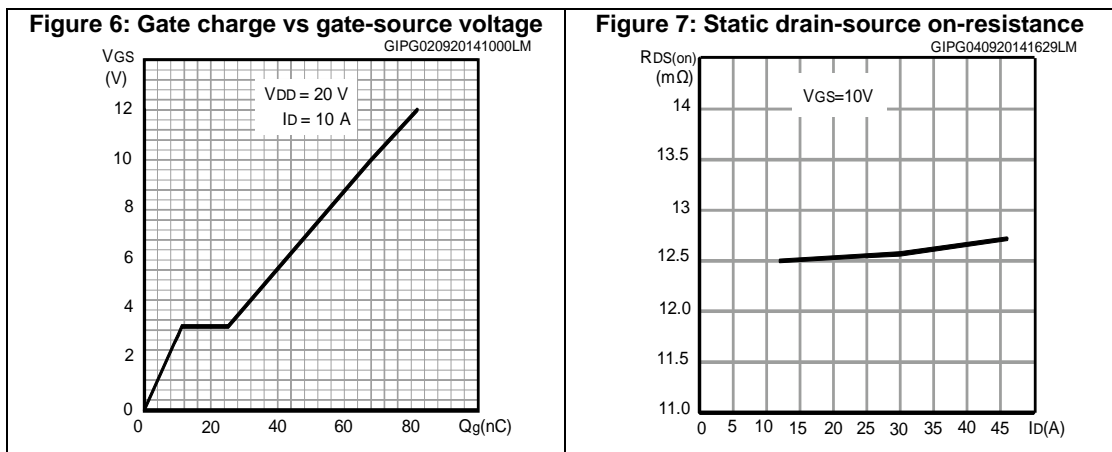
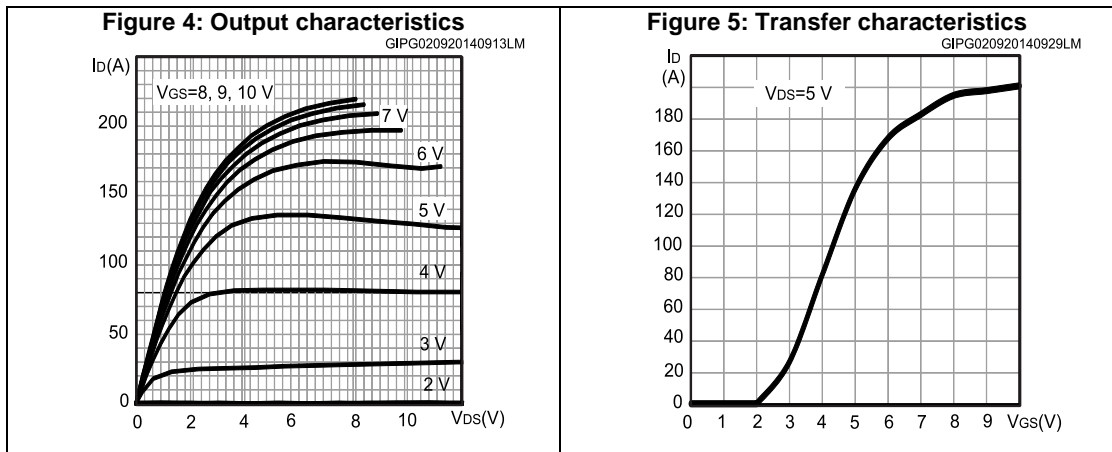
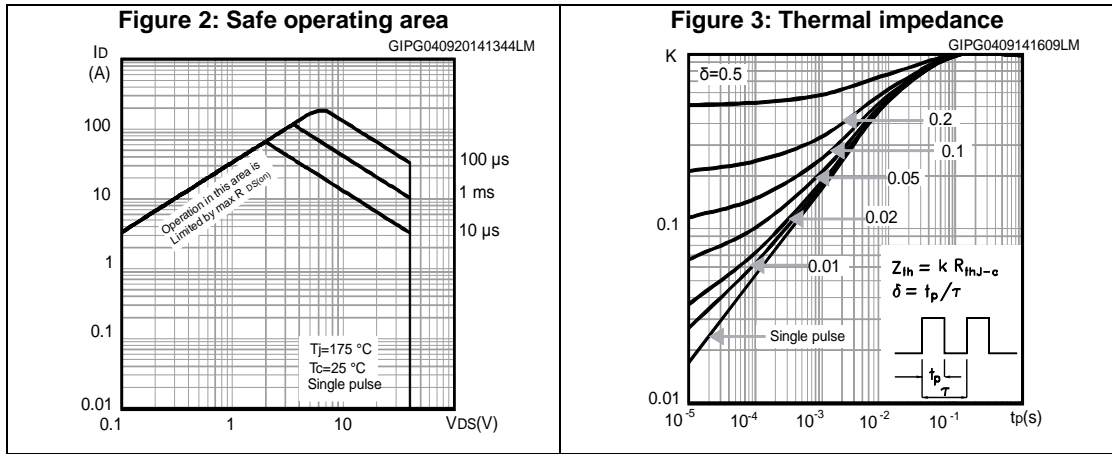


Figure 8: Capacitance variation

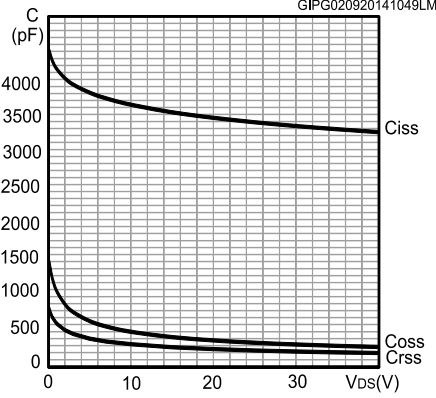


Figure 9: Normalized gate threshold voltage vs temperature

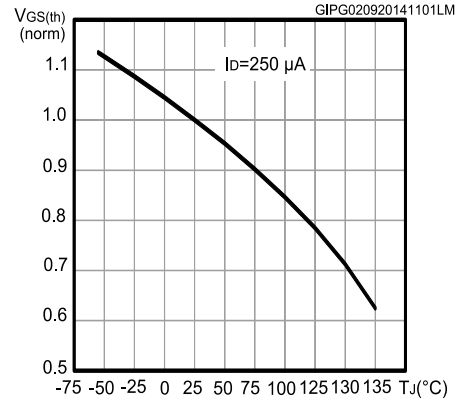


Figure 10: Normalized on-resistance vs temperature

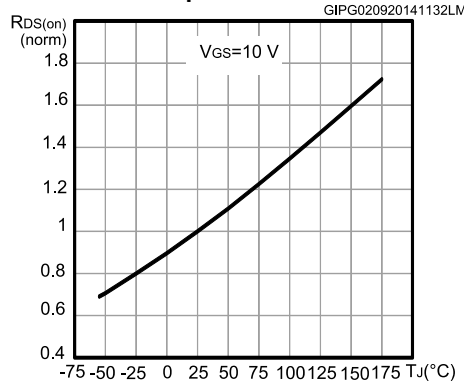


Figure 11: Normalized VBR(DSS) vs temperature

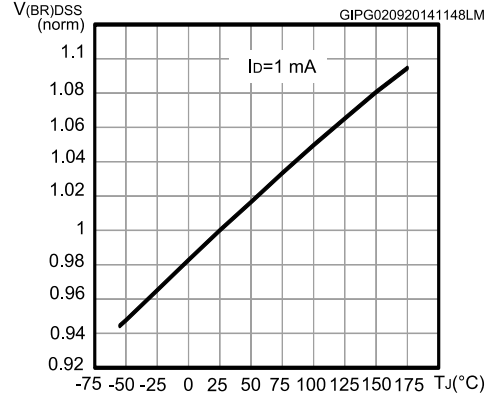
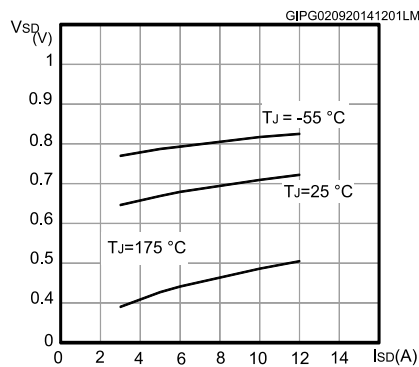
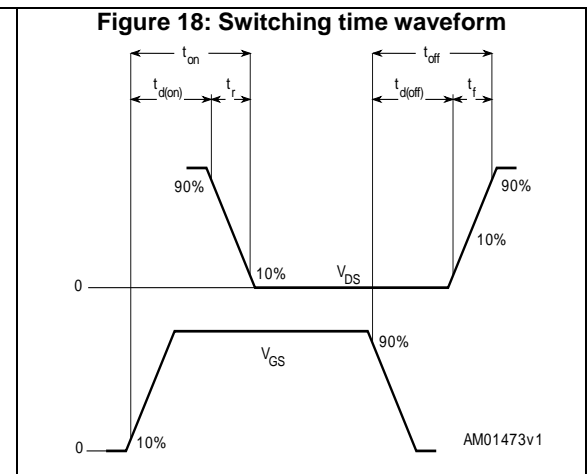
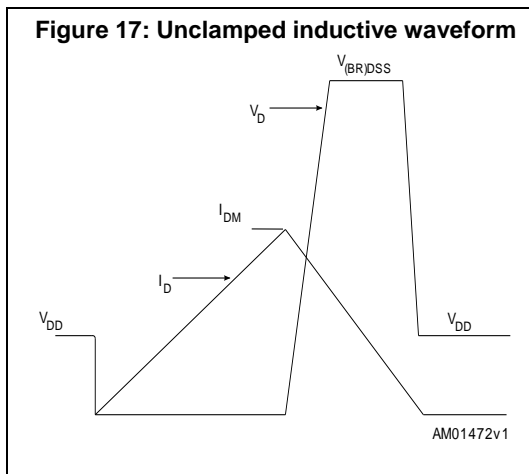
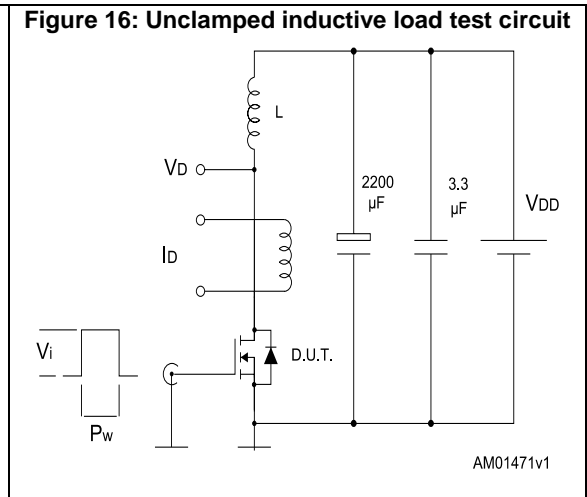
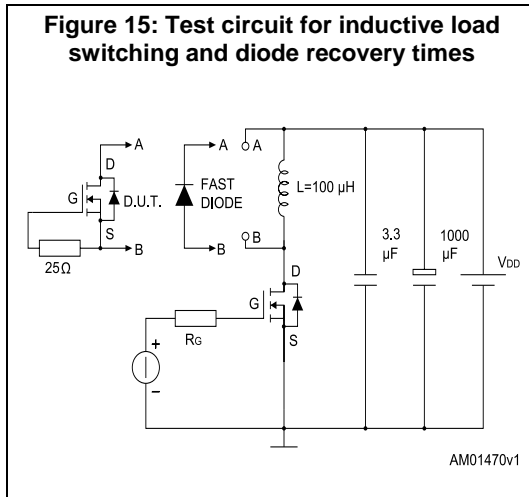
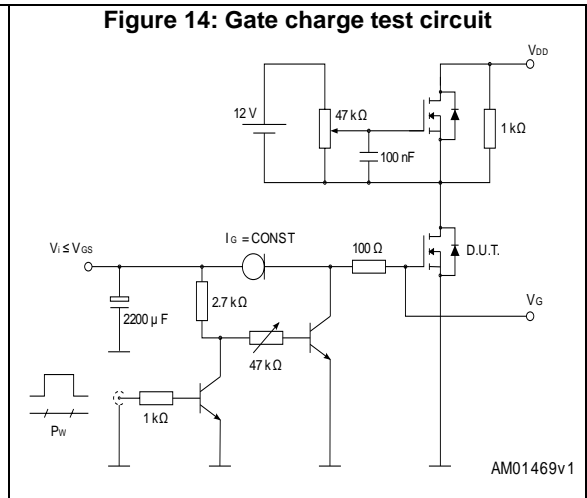
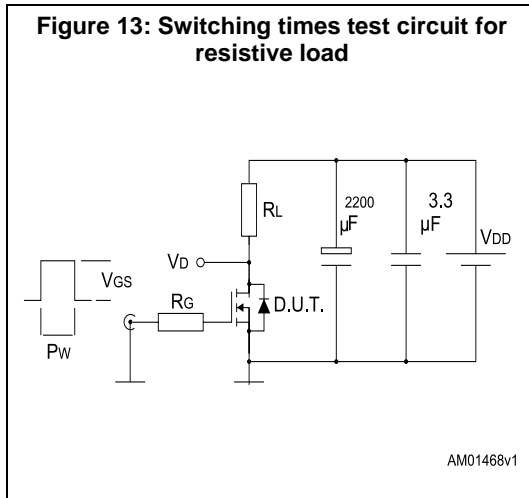


Figure 12: Source-drain diode forward characteristics



4 Test circuits



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

5.1 DPAK (TO-252) rev. Q type A mechanical data

Figure 19: DPAK (TO-252) type A drawings

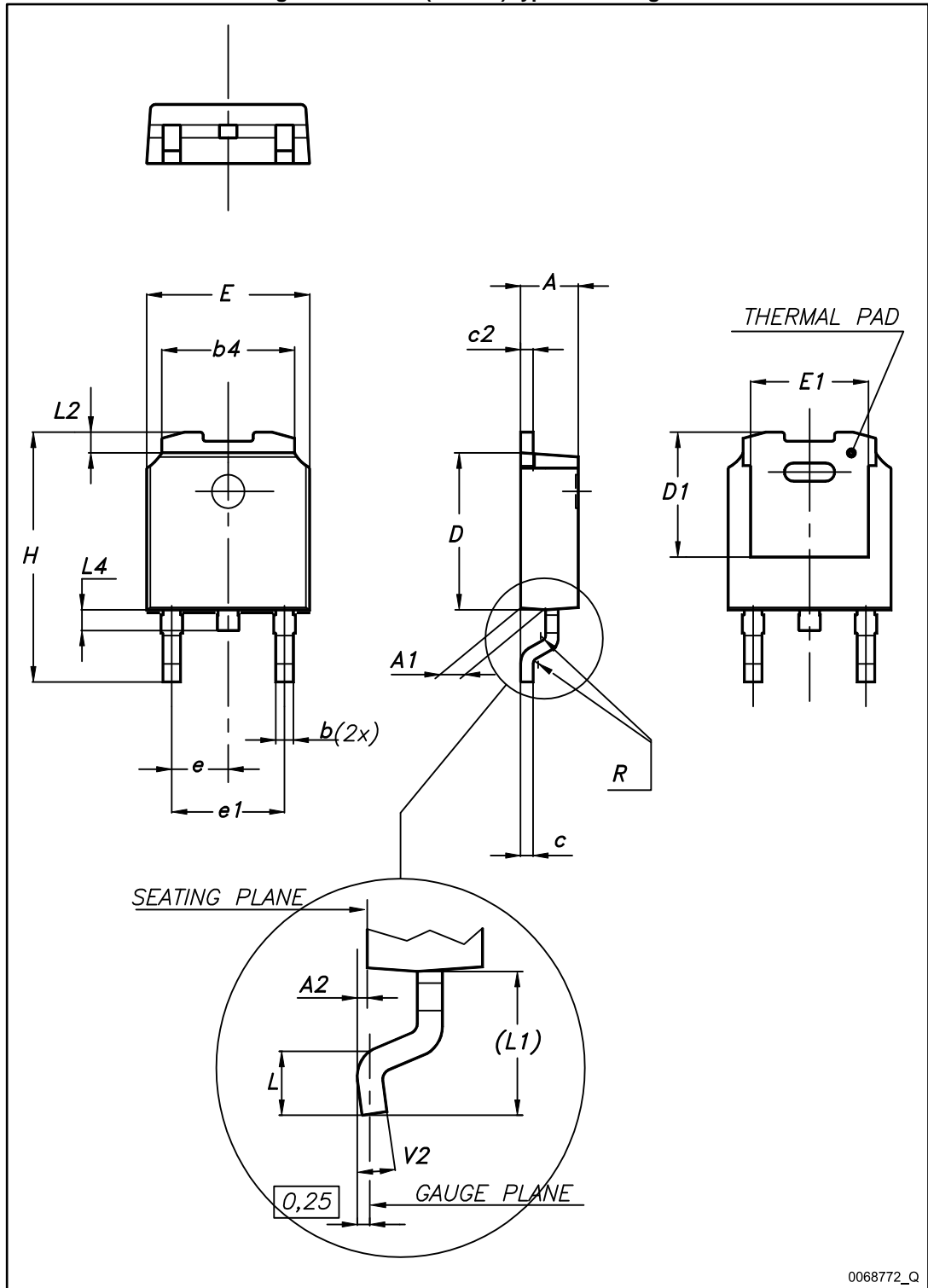
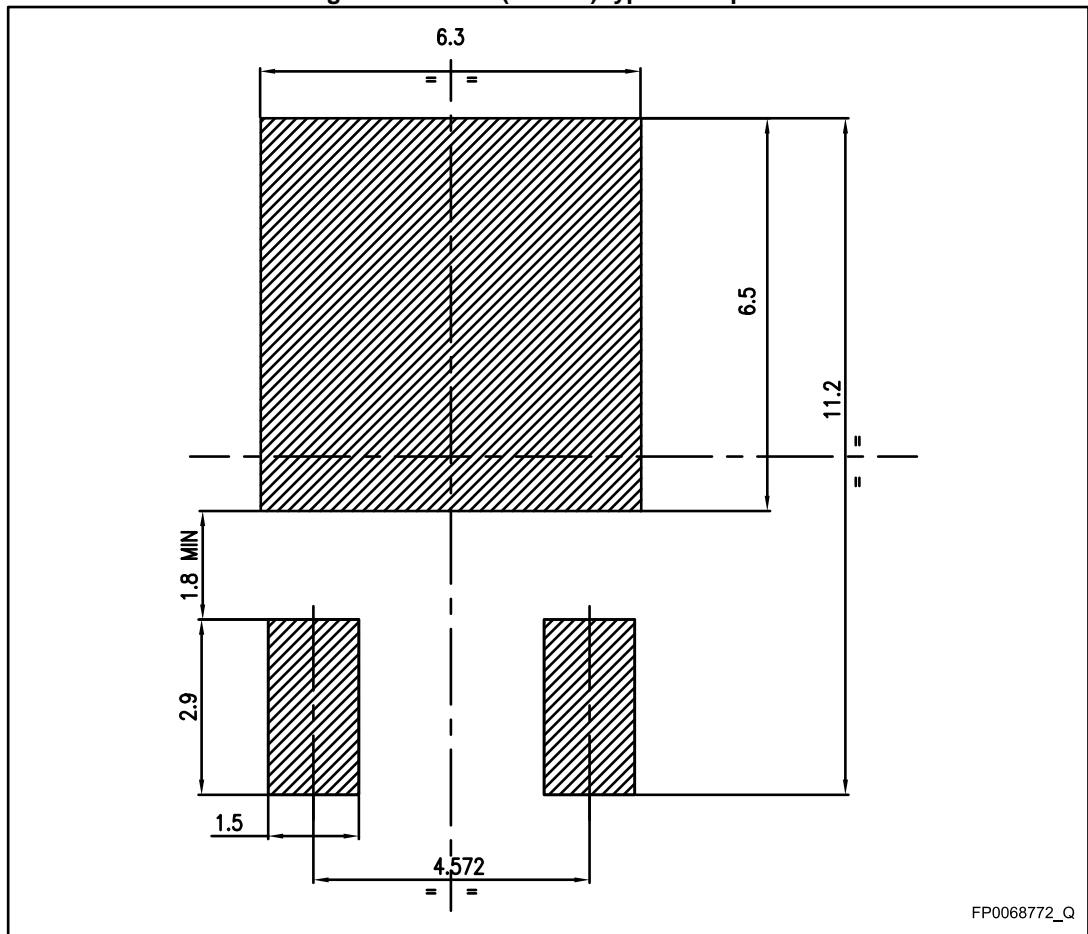


Table 8: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20: DPAK (TO-252) type A footprint



All dimensions are in mm

6 Packaging mechanical data

Figure 21: Tape for DPAK (TO-252)

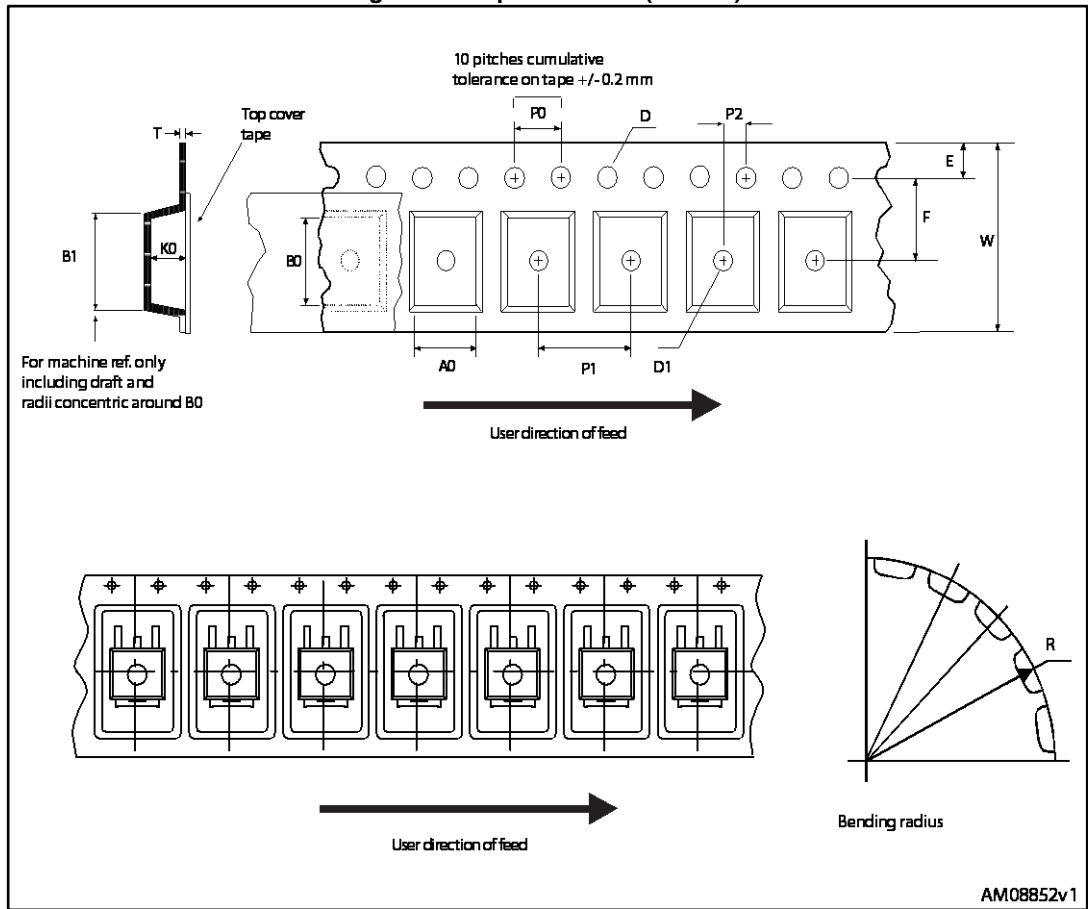


Figure 22: Reel for DPAK (TO-252)

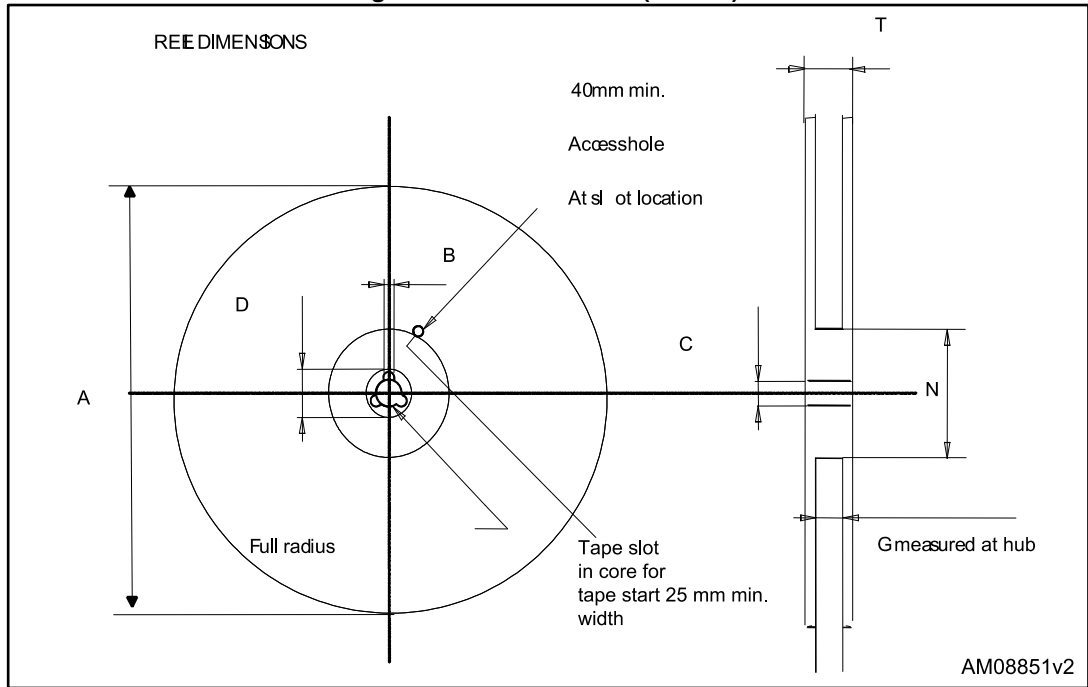


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

7 Revision history

Table 10: Document revision history

Date	Revision	Changes
17-Jan-2014	1	First release
05-Sep-2014	2	Changed the title. Updated <i>Section "Features"</i> and <i>Section "Description"</i> . Updated <i>Table 2: "Absolute maximum ratings"</i> <i>Table 3: "Thermal data"</i> , <i>Table 6: "Switching on/off (inductive load)"</i> , <i>Table 7: "Source-drain diode"</i> .
16-Dec-2014	3	Document status promoted from preliminary data to production data. Minor text changes.

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